Computer Architecture, Fall 2017

Project 2 report
DUE DATE: JANUARY 1, 2018

1 Members & Team Work

- b03902125 郭曉嵐
  - Debugging of *CPU.v*.
  - Handling the stall signal.
- b03902127 林映廷
  - The implementation of the state transition.
  - Setup read/write data of the cache controller.
- b03902129 陳鵬宇
  - Debugging of each sub module.
  - Writing report.

2 Project Implementation

1. First, we review all modules of project1.
2. Copy the code of project1 and add some new *.v* files ("*dcache_top.v*", "*dcache_tag_sram.v*" and "*dcache_data_sram.v*")
3. Finally, modify *CPU.v*, *TestBench.v* and *dcache_top*.

3 Cache Controller in Detail

Compare the Tags

We compare the tags to check if there is a read miss.

```
assign {hit, r_hit_data} = (p1_req && sram_valid && p1_tag == sram_cache_tag[21:0]) ?
       {1'b1, sram_cache_data} : {1'b0, 256'b0};
```

Initialize the 32-bit output data

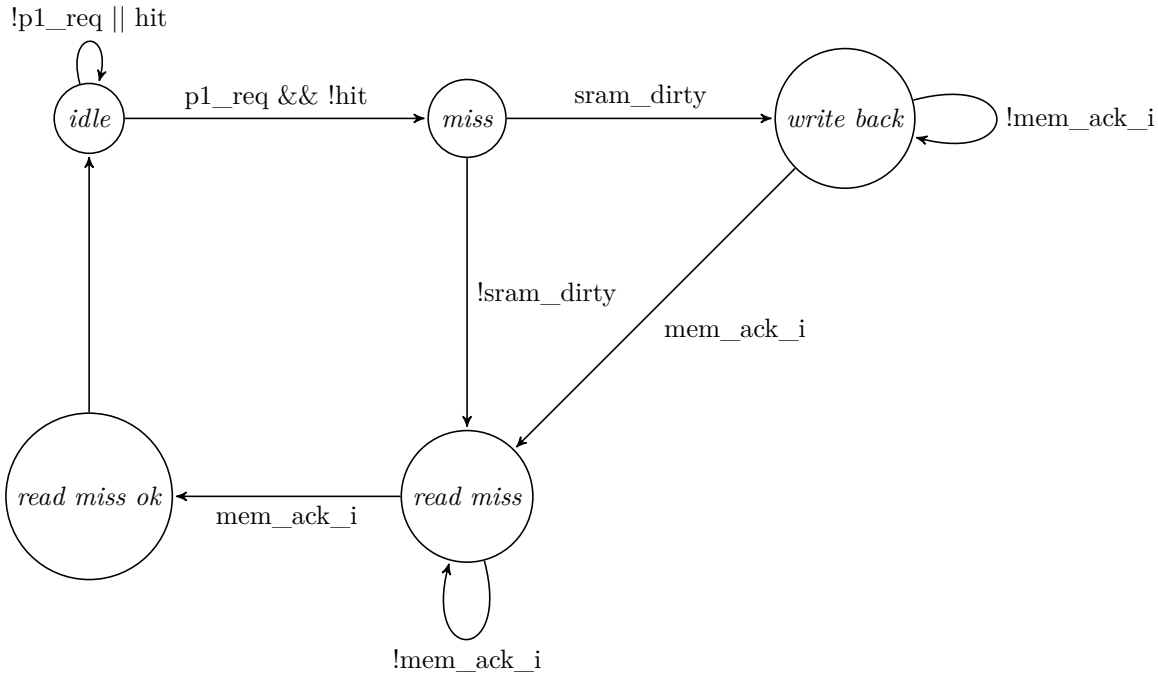
```
always@(p1_offset or r_hit_data) begin
case (p1_offset)
    5'h00: p1_data <= r_hit_data[31:0];
    5'h04: p1_data <= r_hit_data[63:32];
    5'h08: p1_data <= r_hit_data[95:64];
    5'h0c: p1_data <= r_hit_data[127:96];
    5'h10: p1_data <= r_hit_data[159:128];
    5'h14: p1_data <= r_hit_data[191:160];
    5'h18: p1_data <= r_hit_data[223:192];
    5'h1c: p1_data <= r_hit_data[255:224];
```

```
        default p1_data <= 32'd0;
    endcase
    end
```

Initialize the 256-bit output data

```
    always@(p1_offset or r_hit_data or p1_data_i) begin
    case (p1_offset)
        5'h00: w_hit_data <= {r_hit_data[255:32], p1_data_i};
        5'h04: w_hit_data <= {r_hit_data[255:64], p1_data_i, r_hit_data[31:0]};
        5'h08: w_hit_data <= {r_hit_data[255:96], p1_data_i, r_hit_data[63:0]};
        5'h0c: w_hit_data <= {r_hit_data[255:128], p1_data_i, r_hit_data[95:0]};
        5'h10: w_hit_data <= {r_hit_data[255:160], p1_data_i, r_hit_data[127:0]};
        5'h14: w_hit_data <= {r_hit_data[255:192], p1_data_i, r_hit_data[159:0]};
        5'h18: w_hit_data <= {r_hit_data[255:224], p1_data_i, r_hit_data[191:0]};
        5'h1c: w_hit_data <= {p1_data_i, r_hit_data[223:0]};
        default w_hit_data <= 256'b0;
    endcase
    end
```

Revise the signals of the cache



4 Problems and Solution of the Project

To implement L1 cache in so many *.v* files is not easy, we have to carefully connect each input and output in a correct manner. It is also very difficult to debug because there are over *twenty .v* files in the folder. Our eyes really suffered a lot. We inserted the following codes to generate the .vcd file for conveniently debugging:

```
$dumpfile("project.vcd");
$dumpvars
```

By tracing the logic of the .vcd file, it can significantly increase the speed of debugging. Also, printing the values of the ports and pipeline registers works a lot for debugging.