Computer Architecture Homework 1

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1.5 a.

$$\text{CPU time} = \text{Instructions} \times \frac{\text{CPI}}{\text{Clock rate}}$$
$$\text{Instructions per second} = \frac{\text{Clock rate}}{\text{CPI}}$$

- Performance(P1) $= \frac{3\times10^9}{1.5} = 2 \times 10^9$ (instructions/sec)
- Performance(P2) $= \frac{2.5\times10^9}{1.0} = 2.5 \times 10^9$ (instructions/sec)
- Performance(P3) $= \frac{4\times10^9}{2.2} = 1.818 \times 10^9$ (instructions/sec)

As the performance is inversely proportional to the time, the processor with less time performs better. Thus, among the 3 processors, the least time is taken by the processor P_3 resulting in highest performance.

b.

$$\text{CPU time} = \frac{\text{CPU clock cycles}}{\text{Clock rate}}$$
$$\text{Number of cycles} = \text{CPU time} \times \text{Clock rate}$$

- Cycles(P1) $= 10 \times 3 \times 10^9 = 3 \times 10^{10}$
- Cycles(P2) $= 10 \times 2.5 \times 10^9 = 2.5 \times 10^{10}$
- Cycles(P3) $= 10 \times 4 \times 10^9 = 4 \times 10^{10}$

$$\text{Number of instructions} = \frac{\text{CPU clock cycles}}{\text{CPI}}$$

- No.instructions(P1) $= \frac{3\times10^{10}}{1.5} = 2 \times 10^{10}$
- No.instructions(P2) $= \frac{2.5\times10^{10}}{1.0} = 2.5 \times 10^{10}$
- No.instructions(P3) $= \frac{4\times10^{10}}{2.2} = 1.\overline{81} \times 10^{10}$

c.

$$\text{CPU time} = \frac{I \times \text{CPI}}{\text{Clock rate}}$$
$$\text{Clock rate}_{\text{new}} = \frac{I \times \text{CPI}_{\text{new}}}{\text{CPU time}_{\text{new}}} = \frac{I \times (1.2 \times \text{CPI}_{\text{old}})}{0.7 \times \text{CPU time}}$$

- $f(\text{P1}) = \frac{2\times10^{10}\times(1.2\times1.5)}{0.7\times10} \approx 5.14\text{GHz}$
- $f(\text{P2}) = \frac{2.5\times10^{10}\times(1.2\times1.0)}{0.7\times10} \approx 4.28\text{GHz}$
- $f(\text{P3}) = \frac{1.818\times10^{10}\times(1.2\times2.2)}{0.7\times10} \approx 6.85\text{GHz}$

1.6 a.

$$\text{Global CPI} = \sum_i \text{CPI}_i \times \text{the percentage of CPI}_i$$

- Global CPI(P1) $= 1 \cdot 10\% + 2 \cdot 20\% + 3 \cdot 50\% + 3 \cdot 20\% = 2.6$
- Global CPI(P2) $= 2 \cdot 10\% + 2 \cdot 20\% + 2 \cdot 50\% + 2 \cdot 20\% = 2$

b.

$$\text{Clock cycles} = \text{CPI} \times I$$

- Clock cycles(P1) $= 2.6 \times 10^6$
- Clock cycles(P2) $= 2 \times 10^6$

1.8

1.8.1

$$\text{Dynamic power} = 0.5 \times \text{Capacitive load} \times \text{Voltage}^2 \times \text{Clock rate}$$
$$\text{Capacitive load} = \frac{2 \times \text{Dynamic power}}{\text{Voltage}^2 \times \text{Clock rate}}$$

(assuming the static power is negligible)

- Capacitive load(Pentium 4 Prescott processor) = $\frac{2\times 90}{1.25^2 \times 3.6 \times 10^9} = 32 \times 10^{-9} = 32\text{nF}$
- Capacitive load(Core i5 Ivy Bridge) $\frac{2\times 40}{0.9^2 \times 3.4 \times 10^9} \approx 29.05 \times 10^{-9} \approx 29\text{nF}$

1.8.2

$$\text{Total dissipated power} = \text{Dynamic power} + \text{Static power}$$

- Pentium 4 Prescott processor:
  - The ratio of static power to total power = $\frac{10}{10+90} = \frac{1}{10}$
  - The ratio of static power to dynamic power = $\frac{10}{90} = \frac{1}{9}$
- Core i5 Ivy Bridge:
  - The ratio of static power to total power = $\frac{30}{30+40} = \frac{3}{7}$
  - The ratio of static power to dynamic power = $\frac{30}{40} = \frac{3}{4}$

1.8.3

$$P = I \times V$$
$$I_{\text{leak}} = \frac{P_{\text{static}}}{V}$$
$$\text{Total dissipated power} \times 0.9 = 0.5 \times \text{C} \times V_{\text{new}}^2 \times f + V_{\text{new}} \times I_{\text{leak}}$$

- Pentium 4 Prescott processor:
  $I_{\text{leak}} = \frac{10}{1.25} = 8$
  $100 \times 0.9 = 0.5 \times 32 \times 10^{-9} \times V_{\text{new}}^2 \times 3.6 \times 10^9 + V_{\text{new}} \times 8$
  $\rightarrow V_{\text{new}} = 1.18$
- Core i5 Ivy Bridge:
  $I_{\text{leak}} = \frac{30}{0.9} = 33.3$
  $70 \times 0.9 = 0.5 \times 29 \times 10^{-9} \times V_{\text{new}}^2 \times 3.4 \times 10^9 + V_{\text{new}} \times 33.3$
  $\rightarrow V_{\text{new}} = 0.84$