Computer Architecture HW1

Q1

1.5 [4] <§1.6> Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.

a. Which processor has the highest performance expressed in instructions per second?

b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

Q1 Answer

1.5

a. performance of P1 (instructions/sec) $= 3 \times 10^9/1.5 = 2 \times 10^9$
performance of P2 (instructions/sec) $= 2.5 \times 10^9/1.0 = 2.5 \times 10^9$
performance of P3 (instructions/sec) $= 4 \times 10^9/2.2 = 1.8 \times 10^9$

b. cycles(P1) $= 10 \times 3 \times 10^9 = 30 \times 10^9$ s

cycles(P2) $= 10 \times 2.5 \times 10^9 = 25 \times 10^9$ s

cycles(P3) $= 10 \times 4 \times 10^9 = 40 \times 10^9$ s

c. No. instructions(P1) $= 30 \times 10^9/1.5 = 20 \times 10^9$

No. instructions(P2) $= 25 \times 10^9/1 = 25 \times 10^9$

No. instructions(P3) $= 40 \times 10^9/2.2 = 18.18 \times 10^9$

$CPI_{new} = CPI_{old} \times 1.2$, then CPI(P1) = 1.8, CPI(P2) = 1.2, CPI(P3) = 2.6

$f =$ No. instr. $\times$ CPI/time, then

$f(P1) = 20 \times 10^9 \times 1.8/7 = 5.14$ GHz

$f(P2) = 25 \times 10^9 \times 1.2/7 = 4.28$ GHz

$f(P1) = 18.18 \times 10^9 \times 2.6/7 = 6.75$ GHz

Q2

1.6 [20] <§1.6> Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.

Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

a. What is the global CPI for each implementation?

b. Find the clock cycles required in both cases.

Q2 Answer

1.6

a. Class A: 10^5 instr. Class B: 2×10^5 instr. Class C: 5×10^5 instr. Class D: 2×10^5 instr.

Time = No. instr. × CPI/clock rate

Total time P1 $= (10^5 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3)/(2.5 \times 10^9) = 10.4 \times 10^{-4}$ s

Total time P2 $= (10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2)/(3 \times 10^9) = 6.66 \times 10^{-4}$ s

CPI(P1) $= 10.4 \times 10^{-4} \times 2.5 \times 10^9/10^6 = 2.6$

CPI(P2) $= 6.66 \times 10^{-4} \times 3 \times 10^9/10^6 = 2.0$

b. clock cycles(P1) $= 10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 3 = 26 \times 10^5$

clock cycles(P2) $= 10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2 = 20 \times 10^5$

Q3

1.8 The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power.

The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

1.8.1 [5] <§1.7> For each processor find the average capacitive loads.

1.8.2 [5] <§1.7> Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.

1.8.3 [15] <§1.7> If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: power is defined as the product of voltage and current.

Q3 Answer

1.8.1

$$\text{Dynamic Power (DP)} = \frac{1}{2} C \times V^2 \times F \rightarrow C = \frac{2 \times DP}{V^2 \times F}$$

$$\text{Pentium 4} \rightarrow C = \frac{2 \times 90}{1.25^2 \times 3.6 \times 10^9} = 3.2 \times 10^{-8} (F)$$

$$\text{Core i5 Ivy Bridge} \rightarrow C = \frac{2 \times 40}{0.9^2 \times 3.4 \times 10^9} = 2.9 \times 10^{-8} (F)$$

1.8.2

$$\text{Total dissipated power comprised by static} = \frac{Power_{static}}{Power_{static} + Power_{dynamic}}$$

$$\text{Pentium 4} \rightarrow \frac{Power_{static}}{Power_{static} + Power_{dynamic}} = \frac{10}{10+90} = 10\%$$

$$\text{Core i5 Ivy Bridge} \rightarrow \frac{Power_{static}}{Power_{static} + Power_{dynamic}} = \frac{30}{30+40} = 42.9\%$$

$$\text{The ratio of static power to dynamic power} = \frac{Power_{static}}{Power_{dynamic}}$$

$$\text{Pentium 4} \rightarrow \frac{Power_{static}}{Power_{dynamic}} = \frac{10}{90} = 11\%$$

$$\text{Core i5 Ivy Bridge} \rightarrow \frac{Power_{static}}{Power_{dynamic}} = \frac{30}{40} = 75\%$$

1.8.3

$$\frac{NewPower_{static} + NewPower_{dynamic}}{OldPower_{static} + OldPower_{dynamic}} = 0.9 \xrightarrow{Power_{static} = V \times I_{leak},\, Power_{dynamic} = C \times V^2 \times F} \frac{V_{new} \times I_{leak} + C \times V_{new}^2 \times F}{OldPower_{static} + OldPower_{dynamic}} = 0.9$$

$$\xrightarrow{I_{leak} = \frac{OldPower_{static}}{V_{old}}} \frac{V_{new} \times \frac{OldPower_{static}}{V_{old}} + C \times V_{new}^2 \times F}{OldPower_{static} + OldPower_{dynamic}} = 0.9 \rightarrow \text{solve the equation}$$

$$\text{Pentium 4} \rightarrow \frac{V_{new} \times \frac{10}{1.25} + 1.6. \times 10^{-8} \times V_{new}^2 \times 3.6 \times 10^9}{10+90} = 0.9 \rightarrow V_{new} = 1.18 \rightarrow \frac{1.25-1.18}{1.25} = 5.6\%$$

$$\text{Core i5 Ivy Bridge} \rightarrow \frac{V_{new} \times \frac{30}{0.9} + 1.45 \times 10^{-8} \times V_{new}^2 \times 3.4 \times 10^9}{30+40} = 0.9 \rightarrow V_{new} = 0.84 \rightarrow \frac{0.9-0.84}{0.9} = 6.7\%$$