the region.

Operation of FET :

In JFET, the p-n junction b/w gate and source is always kept in reverse biased conditions. Since the current in a reverse biased p-n junction is extremely small, practically zero

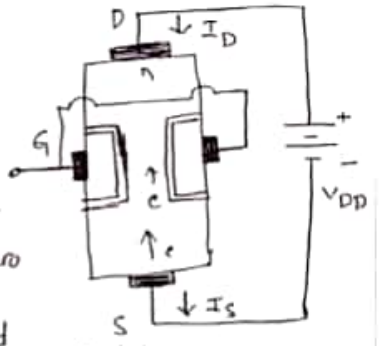
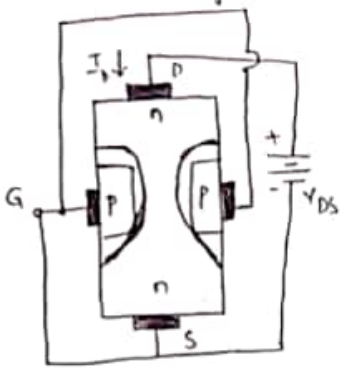


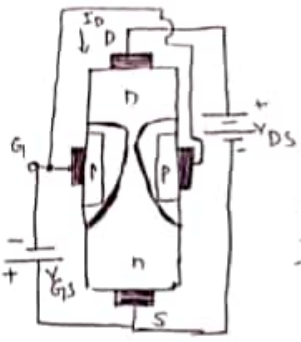
fig: (a) n-channel FET with gate open

From fig (a) the voltage V_{DD} is applied b/w drain and source. Gate terminal is kept open, due to polarities of applied voltage V_{DD} the majority carries i.e., the electrons start flowing

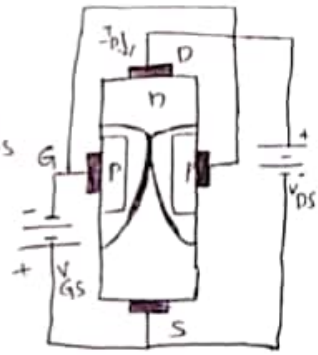
from source to drain. This flow of electrons creates the drain current, I_D. The majority charge carriers moves from source to drain through the space b/w the gate regions. The space is commonly known as channel. The width of this channel can be controlled by varying the gate voltage. To see the effect of gate voltage on channel-width and on drain current I_D, consider the diagram shown below



(a) No bias voltage on gate



(b) small negative gate-source bias



(c) Large negative gate-source bias

fig (a) shows that an n-channel JFET with gate directly connected to the source terminal, when drain voltage is applied (V_{DS}), a drain current I_D flows in the direction shown. Since the n-material is resistive, the drain current causes the voltage drop along the channel. Since gate is heavily doped & the channel is lightly doped, the width of the depletion region will spread in the channel. Thus penetration depends on the reverse bias voltage.

The depletion width across drain is more than the sour because the voltage at drain side is more than voltage at the The depletion region does not have charge carriers, the space b

The depletion width across drain is more than the source because the voltage at drain side is more than voltage at the source side the depletion region does not have charge carriers, the space b/w two depletion regions is available for the conduction of channel. If we extremely applied reverse bias voltage to the gate, the

reverse bias will further increases and hence increases the depletion region which reduces the conducting portion of the channel. As width of the conducting portion of the channel reduces, the no of electrons flowing from source to drain reduces and hence the current flowing from drain to source reduces

If we go on increasing the reverse bias voltage to gate as shown in fig (b) and (c), the depletion regions will increase more and more, and stage will come when the width of depletion region will be equal to the original width of the channel shown in fig (c). This will prevent current flow from drain to source and this will cut off the drain current. The gate to source voltage that produces cut-off is known as "cut-off voltage" and denoted by $V_{GS(off)}$

when the gate is shorted to source (fig (a)), there is minimum reverse bias b/w gate and source p-n junction, making depletion region width minimum and conducting channel width is maximum In this case maximum possible drain current flows which is designated by I_{DSS}. It is clear that the gate to source voltage controls the current flowing through the channel and FET is also called "voltage controlled current source"

Transfer characteristics for n-channel JFET :

For transfer characteristics keep V_{DS} as constant by varying V_{GG}, note down corresponding values of V_{GS} and I_D

V_{DS} = constant		
V_{GG} Vary	V_{GS}	I_D

Transfer characteristics for p-channel JFET:

The transfer characteristics of p channel JFET is identical to transfer characteristics of n-channel JFET except that the polarities of V_{GS} and I_D are reversed.

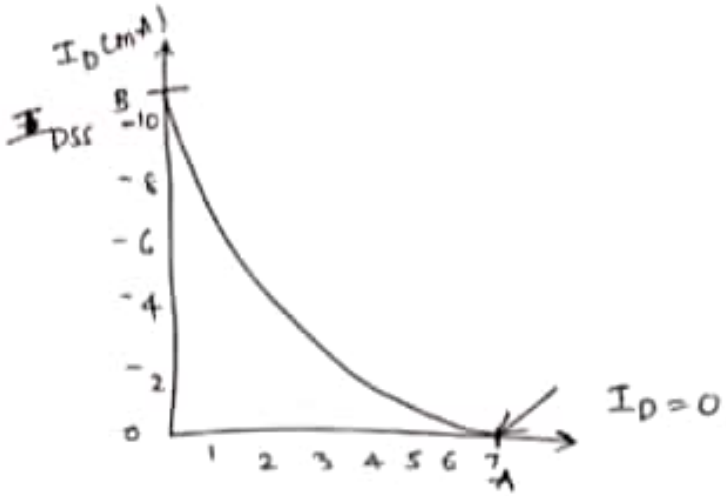
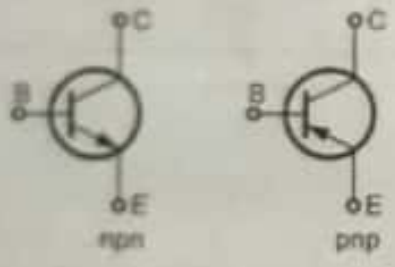
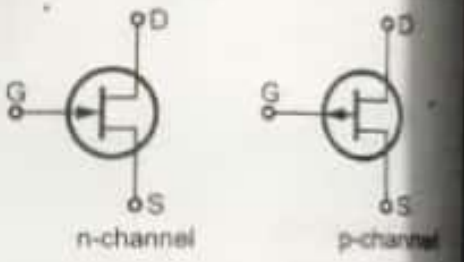


fig: Transfer characteristics of p-channel JFET

7.9 Comparison of BJT and FET

Sr. No.	Parameter	BJT	FET
1.	Control element	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2.	Device type	Current flows due to both, majority and minority carriers and hence **bipolar device.**	Current flows only due to majority carriers and hence **unipolar device.**
3.	Types	n-p-n and p-n-p	n-channel and p-channel.
4.	Symbols		
5.	Configurations	CE, CB, CC	CS, CG, CD
6.	Input resistance	Less compare to JFET.	High compare to BJT.
7.	Size	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in integrated-circuits (IC).

8.	Sensitivity	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9.	Thermal stability	Less	More
10.	Thermal runaway	Exists in BJT, because of cumulative effect of increase in I_C with temperature, resulting increase in temperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D reducing the I_D and hence the temperature of the device.
11.	Relation between input and output	Linear	Non-linear
12.	Ratio of o/p to i/p	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$
13.	Thermal noise	More in BJT as more charge carriers cross junctions.	Much lower in JFET as very few charge carriers cross the junction.
14.	Gain bandwidth product	High	Low

2) B) Relation b/w μ, r_d, and g_m :-

JFET parameters :-

Transconductance $(g_m)_r$

It is defined as change in drain current for a change in gate source with constant drain to source voltage.

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS} \text{ constant}}$$

Transconductance is also called mutual conductance

Drain to source Resistance :-

Drain resistance (r_d) is the AC resistance b/w drain and source terminals when JFET is operating in saturation region.

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} \text{ constant}}$$

Amplification factor (μ) :-

It is defined as change in drain to source terminals for change in gate source with the constant drain current

$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D \text{ constant}}$$

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS} \text{ constant}}$$

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS} \text{ constant}}$$

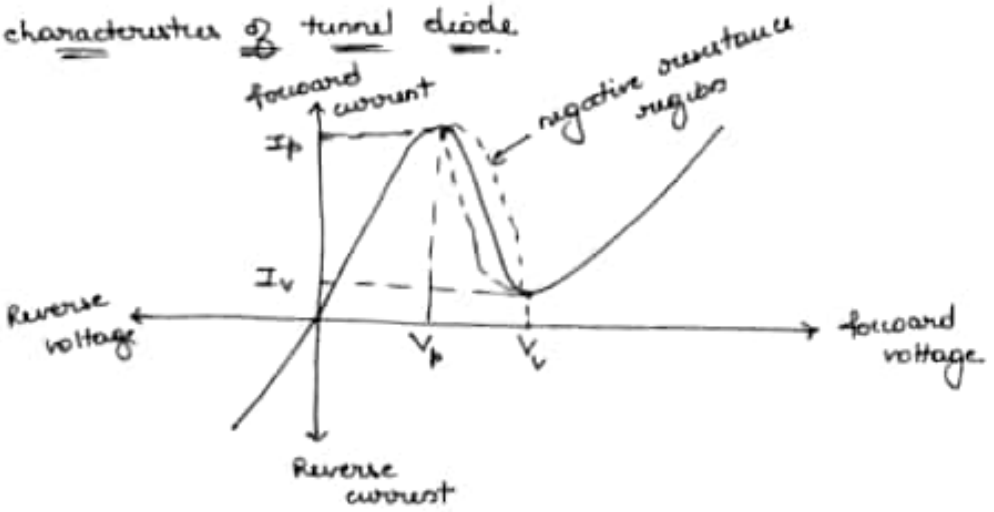
$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D \text{ constant}}$$

$$\therefore \mu = r_d \times g_m$$

$$\frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\cancel{\Delta I_D}} \times \frac{\cancel{\Delta I_D}}{\Delta V_{GS}}$$

$$\frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

→ characteristics of tunnel diode.



The tunnel diode exhibits a negative resistance characteristics between peak current I_p and valley current I_v.

The tunnel diode is excellent conductor in reverse bias conditions.

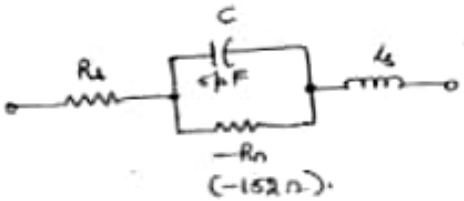
By applying small forward bias voltage to the tunnel diode the current increases and reaches to maximum level. The maximum current for small forward bias voltage is called as "peak current" (I_p). The corresponding voltage to the peak current is called "peak voltage" (V_p)

If the forward bias voltage is increased beyond the peak voltage the current starts decreasing and reaches to minimum level. This minimum value of current is called as "valley current" (I_v). The corresponding voltage to valley current is called as "valley voltage" (V_v).

If forward bias voltage is increased beyond valley voltage it exhibits the same characteristics as ordinary diode.

The symbol and equivalent circuit of tunnel diode is shown below.

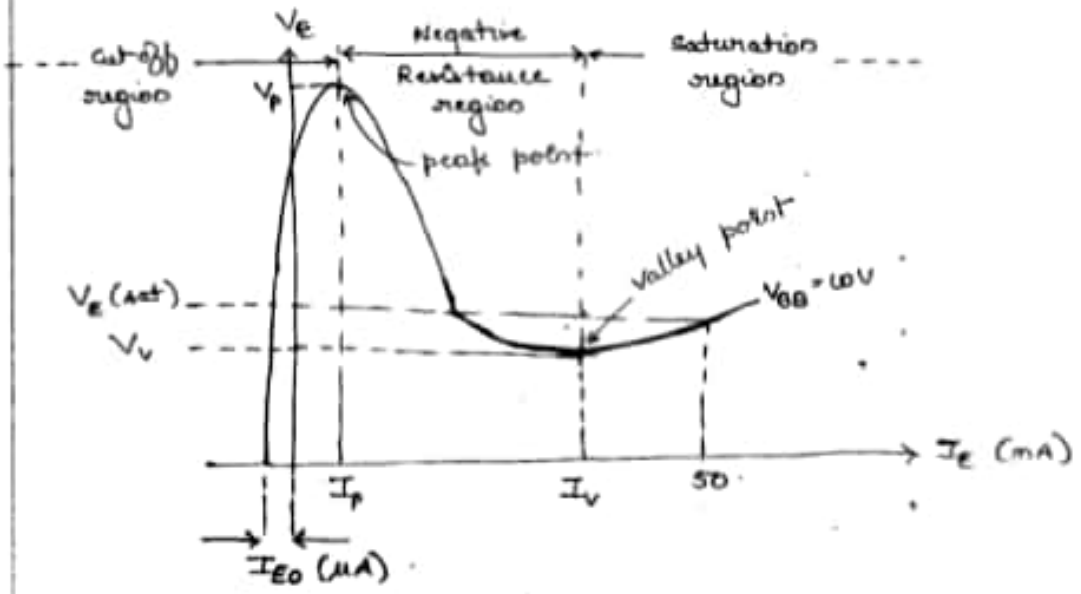
a) Symbol



b) Equivalent Circuit

→ UJT characteristics

The characteristic curve between



Here, upto the peak point (V_p), the diode is reverse biased and hence, the region to the left of the peak point is called **cut-off region**.

At peak point, the peak voltage

$$V_p = \eta V_{BB} + V_0 .$$

The diode starts conduction + holes are injected into n-layer. Hence, resistance decreases thereby decreasing V_E for the increase in I_E. So, there is a **negative reg. resistance region** from peak point V_p to valley point V_v.

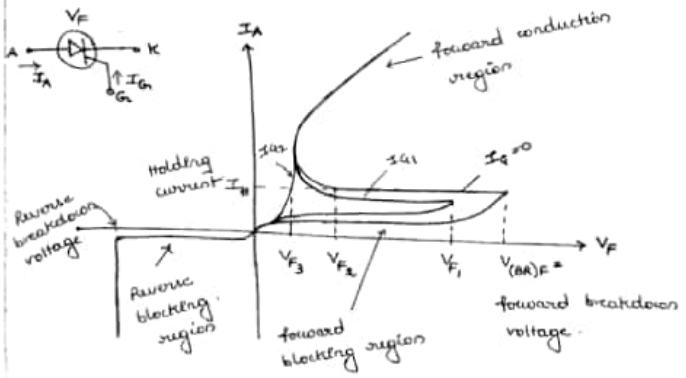
After the valley point, the device is driven into saturation and behaves like a conventional forward biased pn junction diode. The region to the right of the valley point is called **Saturation Region**.

In the valley point, the resistance changes from negative to positive and it remains positive in saturation region.

Due to the negative resistance property, a UJT can be employed in a variety of applications, viz a sawtooth wave generator, pulse generator etc.

→ SCR characteristics:

The characteristics of an SCR are shown for various values of current.



1. Forward breakdown voltage $V_{(BR)F}$*:

It is that voltage above which the SCR enters the conduction region.

The asterisk (*) is a letter that is to be added that is dependent on the condition of the gate terminal as follows:

O = open circuit from G to K

S = short circuit from G to K

R = resistor from G to K

V = fixed bias-voltage from G to K.

2. Holding current, I_H:

It is that current value below which the SCR switches from the conduction state to forward blocking region under stated conditions.

3. Forward & Reverse blocking regions:

These are the regions corresponding to the open circuit condition for the controller rectifier which block the flow of charge (current) from anode to cathode.

4. Reverse breakdown voltage:

It is equivalent to the zener or avalanche region of the fundamental two-layer semiconductor diode.

SCR characteristics are very similar to those of the basic 2-layer semiconductor diode except for the horizontal offshoot before entering the conduction region. It is this horizontal jutting region that gives the gate control over the response of SCR.

For $I_G = 0$, V_F must reach the largest required breakdown voltage ($V_{(BR)F}$*) before the "collapsing" effect will result and the SCR can enter the conduction region corresponding to the "on" state.

If the gate current is increased to I_{G_1}, by applying a bias voltage to the gate terminal, the value of V_F required for the conduction (V_{F_1}) is considerably less. The holding current I_H also drops with increase in I_G.

If gate current is further increased to I_{G_2}, the SCR will fire at very low values of voltages (V_{F_3}) and the characteristics begin to approach those of the basic pn junction diode.

1. *Why thermal runaway is not there in FETs ?*

8.2 Biasing Circuits for FET

Different biasing circuits of FET are :

- Fixed bias circuit
- Self bias circuit
- Voltage divider bias circuit

8.2.1 Fixed-bias Circuit

Fig. 8.2.1 shows the fixed bias circuit for the n-channel JFET. This is the simplest biasing arrangement. To make gate-source junction reverse-biased, a separate supply V_{GG} is connected such that gate is more negative than the source.

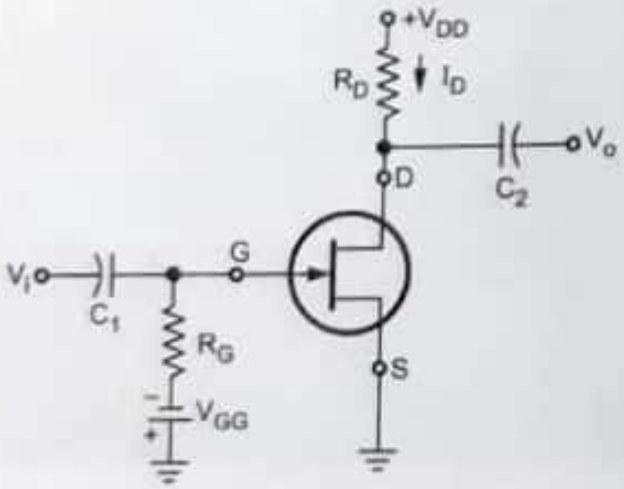


Fig. 8.2.1 Fixed bias circuit for n-channel circuit

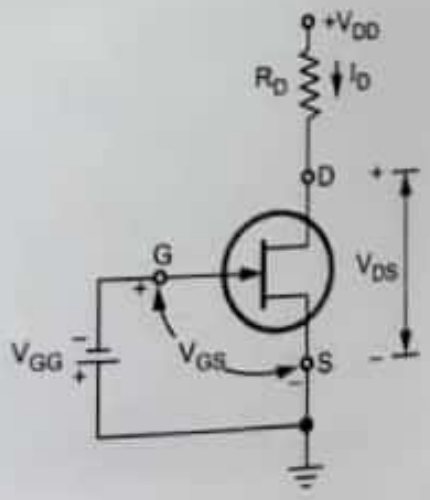


Fig. 8.2.2 Simplified fixed bias circuit

the d.c. analysis coupling capacitors are open circuits. The current through R_G is zero. This permits R_G to replace by short circuit equivalent, simplifying the circuit as shown in the Fig. 8.2.2.

Calculate V_{GS}

for d.c. analysis $I_G = 0$ A and applying KVL to the input circuit we get,

$$V_{GS} = -V_{GG} \quad \ldots (8.2.1)$$

V_{GG} is a fixed d.c. supply, the voltage V_{GS} is fixed in magnitude, and hence the fixed bias circuit.

Calculate I_{DQ}

The drain current I_D can be calculated using equation.

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Calculate V_{DS}

The drain to source voltage of drain circuit can be determined by applying KVL.

$$V_{DD} - I_D R_D - V_{DSQ} = 0$$

$$V_{DSQ} = V_{DD} - I_D R_D \quad \ldots (8.2.2)$$

The main drawback of fixed bias circuit of FET is that it requires two power supplies.

8.2.2 Voltage Divider Bias Circuit

The Fig. 8.2.4 shows n-channel JFET with voltage divider bias. The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased. The source voltage is,

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2. Coupling capacitors C_1 and C_2 and source resistor bypass capacitor C_S are assumed to be open circuit for DC analysis.

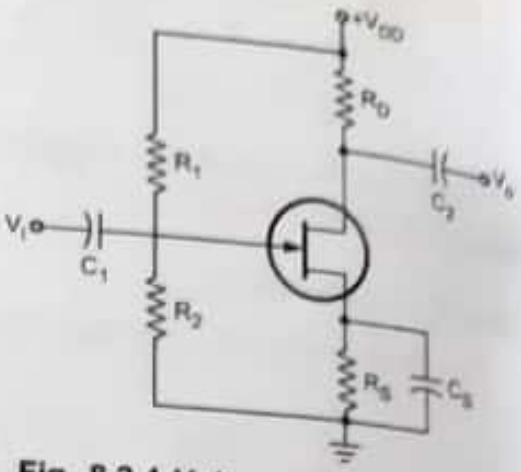


Fig. 8.2.4 Voltage divider bias for n-channel JFET

D.C. analysis :

Step 1 : Calculate V_G

$$V_G = \frac{V_{DD} R_2}{R_1 + R_2} \qquad \because I_G = 0$$

Step 2 : Obtain expression for V_{GS}

Applying KVL to the input circuit we get,

$$V_G - V_{GS} - I_D R_S = 0$$

$$\therefore \quad V_{GS} = V_G - I_D R_S \qquad \ldots (8.2.3)$$

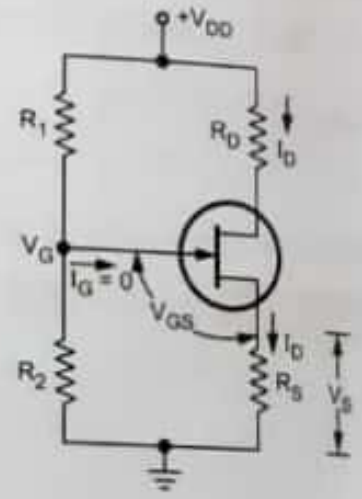


Fig. 8.2.5 Simplified voltage divider circuit for d.c. analysis

Step 3 : Calculate I_{DQ}

The I_{DQ} can be calculated using equation :

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

Step 4 : Calculate V_{DS} and V_{GS}

Applying KVL to the output circuit we get,

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$= V_{DD} - I_D (R_D + R_S) \quad \ldots (8.2.4)$$

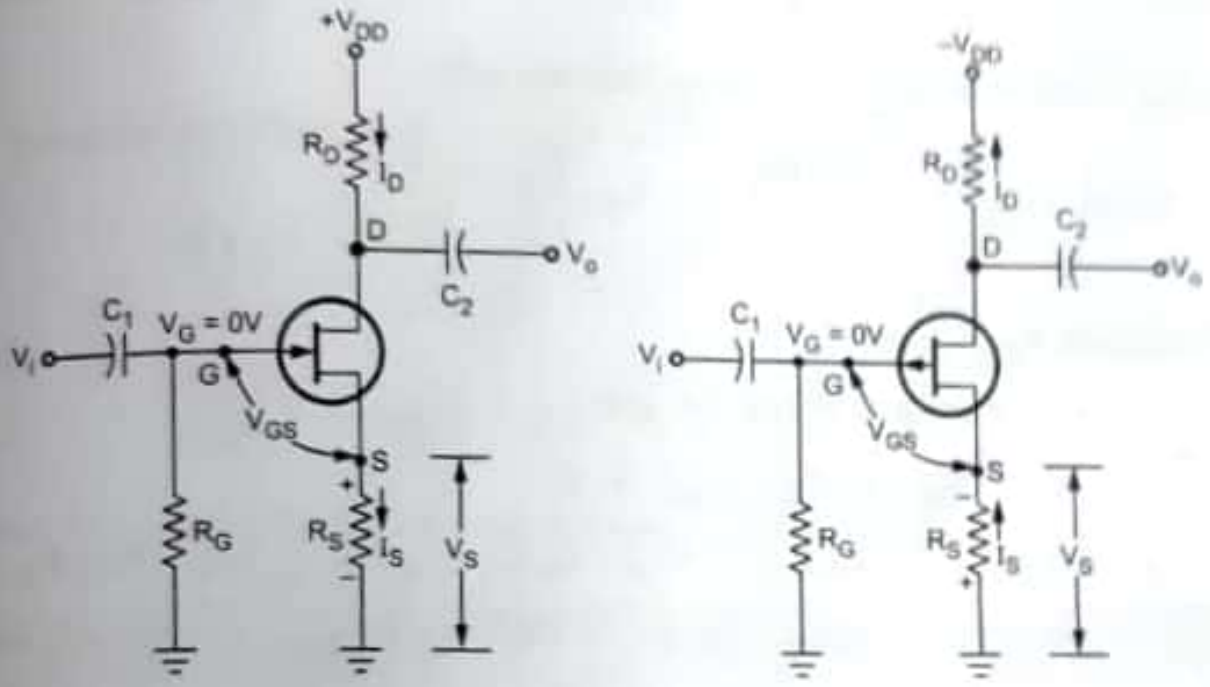
Q point of a JFET amplifier using the voltage divider bias is given by :

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$

$$V_{GSQ} = V_G - I_D R_S$$

Self bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. This can be achieved using the self bias arrangement shown in Fig. 8.2.10 The gate resistor, R_G does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V. R_G is necessary only to isolate an a.c. signal from ground in amplifier applications. The voltage drop across resistor, R_S makes gate source junction reverse biased.



(a) n-channel (b) p-channel

Note : $I_S = I_D$ in all JFETs

Fig. 8.2.10 Self bias circuits for JFET

D.C. analysis :

Step 1 : Obtain expression for V_{GS}

For the n-channel FET in Fig. 8.2.10 (a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = I_S R_S = I_D R_S$. The gate to source voltage is,

$$V_{GS} = V_G - V_S = 0 - I_D R_S = - I_D R_S$$

For the p-channel FET in Fig. 8.2.10 (b), I_S produces a voltage drop across R_S and makes the source negative with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = -I_S R_S = -I_D R_S$. The gate to source voltage is

$$V_{GS} = V_G - V_S = 0 - (-I_D R_S) = +I_D R_S$$

In the following d.c. analysis, the n-channel JFET shown in Fig. 8.2.10 (a) is used to for illustration . For d.c. analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent, since $I_G = 0$. This is illustrated in Fig. 8.2.11.

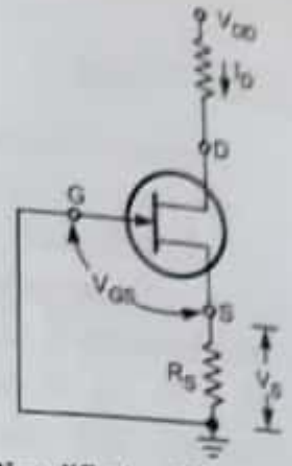


Fig. 8.2.11 Simplified self bias circuit for d.c. analysis

Step 2 : Calculate I_{DQ}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_p}\right)^2 = I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2 \quad \ldots (8.2.5)$$

Step 3 : Calculate V_{DS}

Applying KVL to the output circuit we get,

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore \quad V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D = V_{DD} - I_D (R_S + R_D)$$

Q35. Discuss Zener and avalanche breakdown mechanisms.

Ans:

The diode enters the breakdown region when the magnitude of the reverse voltage exceeds a threshold value that is specific to the particular diode, called the breakdown voltage. In the breakdown region for very small variation in voltage the current increases rapidly. There are two types of breakdown mechanisms,

1. Avalanche breakdown
2. Zener breakdown.

1. **Avalanche Breakdown:** In this mechanism thermally generated electron-hole pairs gains energy from the external voltage applied and breaks the covalent bonds to produce new electron-hole pairs. This new electron-hole pairs, inturn, generates more electron-hole pairs by disrupting bonds and the process continues cumulatively. This cumulative process is known as Avalanche Multiplication. Due to this large current is seen at the terminals of diodes for small variations in voltage.

2. **Zener Breakdown:** In this mechanism electron-hole pairs are generated by applying strong electric field. Because of the presence of strong electric field direct rupture of covalent bonds takes place. Due to this new electron-hole pairs are generated. The breakdown occurring due to application of strong electric fields is known as Zener breakdown.

Q36. With neat diagram, explain the operation of Zener diode and its forward and reverse characteristics. Also distinguish between Avalanche and Zener Break downs.

Ans:

Zener Diode: The power dissipated at the junction of a normal PN diode operating in breakdown region is very large. Due to large power dissipation, the diode gets damaged. The diode which is designed to operate in breakdown region under certain conditions is known as Zener diode. Zener diode is heavily doped than normal PN-Junction diodes. The circuit symbol of Zener diode is as shown in figure (1).

Characteristics: Figure (2) illustrates that V-I characteristics of Zener diode.

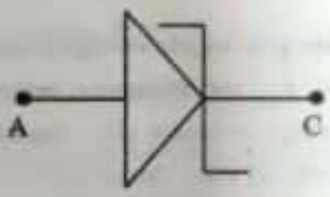


Figure (1): Symbol of Zener Diode

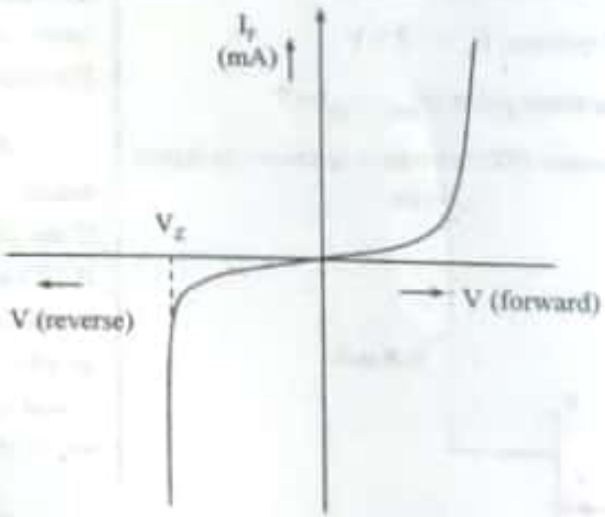


Figure (2): V-I Characteristics of Zener Diode

It can be observed from figure (2) that under forward biased condition, a zener diode operates like an ordinary diode. Under reverse-biased condition, an increase in reverse voltage (V_R), decreases the reverse current (I_R). A further increase in V_R causes a sharp breakdown in I_R. Such breakdown in zener diode is called zener breakdown and the voltage at which breakdown occurs is called zener voltage (V_Z). After, the breakdown, zener diode operates with a constant voltage.

The breakdown in voltage largely depends on the amount of doping. If the diode is heavily doped, the width of depletion layer decreases and the breakdown occurs at a lower reverse voltage. On the other hand, if diode is lightly doped, a higher breakdown of voltage occurs.