PCC-CS492

Computer Architecture Lab

Assignment Set 1 : HDL Introduction

Problem Statements

11) Print a simple text using iverilog.

12) Implement the following basic gates and verify their truth tables using iverilog:

- **a)** BUFFER and NOT
- **b)** AND
- **c)** OR
- **d)** XOR
- **e)** NAND
- **f)** NOR
- **g)** XNOR

13) Implement the following expressions using iverilog:

- **a)** A + B . C
- **b)** A’ . B + C’ . B
- **c)** (X + Y) $\oplus$ Z’
- **d)** (P . Q)’ $\odot$ (P $\oplus$ R)

Assignment Set 2 : Design of Different Adder-Subtractor

Problem Statement

21) Design a half adder circuit using iverilog.

22) Design a full adder circuit using iverilog.

23) Design a 8-bit parallel adder circuit using full adder as a component.

24) Design a 8-bit adder-subtractor composite circuit.

25) Design a 4 bit BCD adder .

26) Design a half subtractor using logic gates in VHDL.

27) Design a full subtractor using half subtractor as a component.

28) Design a 8 bit parallel subtractor.

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Assignment Set 3 : Design of Decoder

Problem Statements

31) Design a 1:2 decoder circuit using iverilog.

32) Design a 2:4 decoder circuit using iverilog.

33) Design a 3:8 decoder circuit using iverilog.

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Assignment Set 4 : Design of MUX and DEMUX

Problem Statements

41) Design a 2:1 multiplexer using iverilog.

42) Design a 4:1 multiplexer using 2:1 multiplexer as component.

43) Design a 8:1 multiplexer using 4:1 and 2:1 multiplexer as component.

44) Design a 1:2 demultiplexer using iverilog.

45) Design a 1:4 demultiplexer using 1:2 demultiplexer as component.

46) Design a 1:8 demultiplexer using 1:4 and 1:2 demultiplexer as component.

Assignment Set 5 : Design of Sequential Circuit

Problem Statements

51) Design Gray Code using iverilog.

52) Design T Flip Flop using iverilog.

53) Design JK Flip Flop using iverilog.

54) Design Shift Register using iverilog.

Assignment Set 6 :

Design of multiplier and Divisor Circuit

Problem Statements

61) Design Booth's Algorithm to multiply 2 signed n bit number using iverilog.

62) Design restoring division algorithm to implement division operation of two n bit numbers using iverilog.

63) Design non-restoring division algorithm to implement division operation of two n bit numbers using iverilog.

Assignment Set 7 :

Design of Memory, ALU and Mini Computer

Problem Statements

71) Design ALU using iverilog.

72) Design ROM using iverilog.

73) Design RAM using iverilog.

74) Design a small computer by combining ROM, RAM and ALU.

- **a)** ROM should store opcode and address of data.
- **b)** RAM should store data in some addresses.
- **c)** ALU must get the opcode and address from ROM and access data from RAM to perform the operation.