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RV COLLEGE OF ENGINEERING®

(An Autonomous Institution affiliated to VTU) III Semester B. E. Examinations Nov/Dec-19

Computer Science and Engineering

FOUNDATIONS OF COMPUTER SYSTEMS DESIGN

Time: 03 Hours Maximum Marks: 100

Instructions to candidates:

- 1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
- 2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

PART-A

1	1.1	Write the <i>IEEE</i> standard floating point representation for both single and						
		double precision.						
	1.2	Simplify the expression	02					
		$F(A,B,C,D) = \sum m(0,1,5,9,13,14,15) + d(3,4,7,10,11)$ using K-map method.						
	1.3	Write the timing diagram for positive edge triggered SR flip flop.	02					
	1.4	Give the differences between synchronous and asynchronous counters.	02					
	1.5	Construct the state diagram for the following state table:						
		Present State Next state Output						
		$Q1 \ Q2 \ x = 0 \ x = 1 \ x = 0 \ x = 1$						
		0 0 11 01 0 0						
		0 1 11 00 0 0						
		1 0 10 11 0 1						
		1 1 1 10 10 0 1						
	1.6	Obtain the performance for the processor with clock rate= 800mHz, No of	02					
		instructions executed= 1000 and average number of steps						
		needed/machine instructions= 20.						
	1.7	Consider a 32-bit integer in hexadecimal representation is 12345678 <i>H</i> , by	02					
		assuming 100 is the starting location of memory, represent the data in						
		both little-endian and big-endian alignment.						
	1.8	List the operations performed by the <i>CALL</i> instruction.						
	1.9	Draw the simple arrangement of cache memory and also give its use.						
	1.10	Write the control sequence for the instruction ADD R4, R5, R6 for the three						
		bus organization.						

PART-B

2	а	Write and explain the register configuration of sequential circuit binary multiplier and also multiply 13 by 11 using sequential multiplier.	08
	b	Design the following combinational circuits:	
		i) $F(A,B,C,D) = \sum m(2,4,5,7,10,14)$ using 8:1 multiplier (consider LSB as MEV)	
		ii) Full adder using appropriate decoder and logic gates (consider	
		both enable and outputs are active high enable)	08
	•		
3	а	Illustrate the working of positive edge triggered JK flipflop along with its	
		circuit diagram, truth table, excitation table and timing diagram.	08

b Design ripple counter for the following state chagram using negative edge triggered 7-flipflop also write the timing diagram for the same. OR 4 a Construct the SR latch using NOR gates and explain its operation along with truth table and timing diagram. b Write the logic symbol, truth table and timing diagram for a new negative edge clocked X - Y flipflop is defined with two inputs X & Y and two outputs Q & Q̄. The flipflop functions as follows: If XY = 00 flipflop state Q becomes 1 with next clock pulse If XY = 10 flipflop state Q becomes 0 with next clock pulse If XY = 10 flipflop state Q becomes 0 with next clock pulse If XY = 11 flipflop state Q becomes 0 with next clock pulse If XY = 10 flipflop state Q becomes 0 with next clock pulse If XY = 11 flipflop state Q becomes 0 with next clock pulse Design mod-3 asynchronous ripple counter using negative edge triggered 7-flipflops. To R OR 6 a Design the circuit for a sequence recognizer to detect an input sequence of '1011'. The sequence recognizer outputs a '1' on the detection of this input sequence. Use Ir and D flipflops to implement the circuit. Describe the basic performance equation. Find the total time required execute the program contains 1000 instructions, out of that 25% instructions requires 4 clock cycles, 40% instructions require 5 clock cycles and remaining instruction requires 3 clock cycles for execution. The processor is running at 161lz frequency. 7 a Discuss any four addressing modes with an example. B llustrate the working subroutine with a coding example also explain parameter passing in subroutine. 8 a Write and explain internal organization of a 2M × 8 dynamic memory chip. b Write the control sequence for execution of the instruction ADD (R ₃), R ₁ 04 Hierotropic and the program control unit organization.				
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