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RV COLLEGE OF ENGINEERING®

(Autonomous Institution affiliated to VTU)

III Semester B. E. Fast Track Examinations Oct-2020

Computer Science and Engineering

COMPUTER ORGANIZATION

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

PART-A

1	1.1	Define clock and clock rate.	01
	1.2	Write a program that can evaluate the expression $A * B + C * D$ in a single-accumulator processor. Assume that the processor has Load, Store, Multiply and Add instructions, and that all values fit in the accumulator.	02
	1.3	Name any two conditional codes and illustrate their significance.	02
	1.4	Assume Register $R2$ contains $1000, R10$ contains 2. The numbers 1,2,3,4,5,6 are stored in successive word locations starting at memory addresses 1000. Discuss the effect of executing this ARM instruction: $LDR\ R1, [R2], R10, LSL\ \#2$.	02
	1.5	With respect to cache memories, differentiate between write back protocol and write through protocol.	02
	1.6	Convert the following pairs of decimal numbers to 5-bit, signed, 2's complement, and binary and add them. State whether or not overflow occurs in each case. a) -14 and 11 b) -10 and -13	02
	1.7	Mention the difference between a subroutine and Interrupt service routine.	01
	1.8	Define Direct Memory Access.	01
	1.9	When $E' = 0$ and $M = 0$ the value represented is called _____.	01
	1.10	Summarize the algorithm for non restoring division.	02
	1.11	Define memory interleaving.	01
	1.12	Mention the importance of Translation Look Aside Buffer (TLB).	01
	1.13	Mention any two design objectives of USB.	02

PART-B

2	a	With a neat diagram of connections between the processor and memory, list and explain the basic steps needed to execute the machine instruction Move $LOCA, R0$ in terms of transfers between the components of processor, memory and some control commands.	10
	b	Define addressing mode. Explain any five addressing modes with examples.	06
3	a	Define subroutine linkage. With an example explain different mechanism of passing parameters to subroutines.	08

	b	With syntax and examples explain multiplication and division instructions.	04
	c	Discuss the subroutines for a safe pop operation and safe push operations to check stack full and stack empty respectively.	04
		OR	
4	a	Discuss the following with respect to ARM processor with an example for each. i) $LDMIA$ ii) MLA iii) BIC.	06
	b	Explain the difference between Pre indexed addressing node, Pre indexed mode with write back and post indexed addressing node with examples.	06
	c	Discuss ARM instruction format.	04
5	a	What are interrupts? With a neat diagram explain the interrupt hardware and ways of enabling and disabling interrupts.	08
	b	Define bus arbitration. Explain the different ways of bus arbitration with suitable diagram.	08
		OR	
6	a	Explain registers in DMA interface.	02
	b	Define Bus Master. With the help of timing diagram differentiate between synchronous bus and asynchronous bus.	06
	c	With the help of neat diagram explain data transfer operation of PCI bus.	08
7	a	Design $2M \times 32$ memory module using $512k \times 8$ memory chip and explain various external connections.	06
	b	Discuss direct mapped, associative mapped and set associative mapped cache memory system with suitable diagrams.	06
	c	Consider main memory size of $16GB$, block size of $4KB$ and number of tag bits in the address are 10, for a 4 way set associative cache, determine: i) Number of cache lines ii) Total cache size.	04
8	a	With the neat diagram of three bus organization of the data path, demonstrate the control sequence for the instruction $Add\ R4, R5, R6$	06
	b	Multiply each of the following pairs of numbers using Booth Algorithm and Bit pair recording of multipliers. i) 010111 and 110110 ii) 110101 and 011011.	08
	c	Identify the value of the binary number in 32-bit $IEEE$ format: 00111110011011010000000000000000	02