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RV COLLEGE OF ENGINEERING®
 (An Autonomous Institution affiliated to VTU)
 III Semester B. E. Examinations March-2021

Computer Science and Engineering
FOUNDATIONS OF COMPUTER SYSTEMS DESIGN

*Time: 03 Hours**Maximum Marks: 100**Instructions to candidates:*

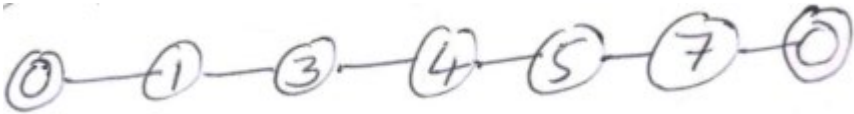
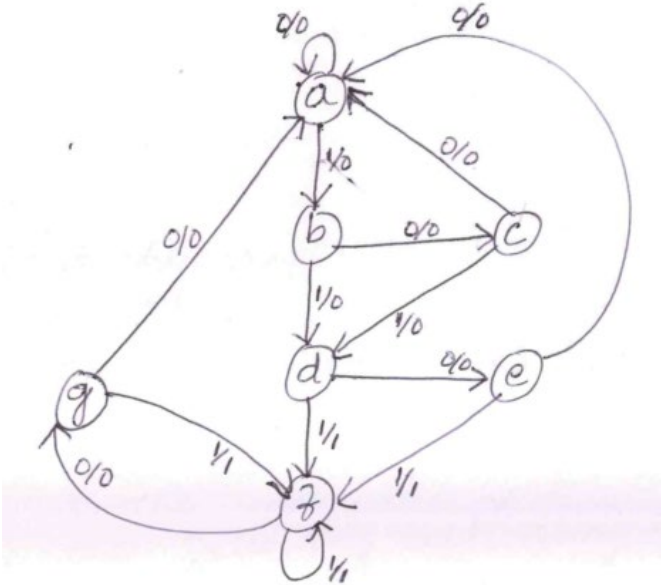
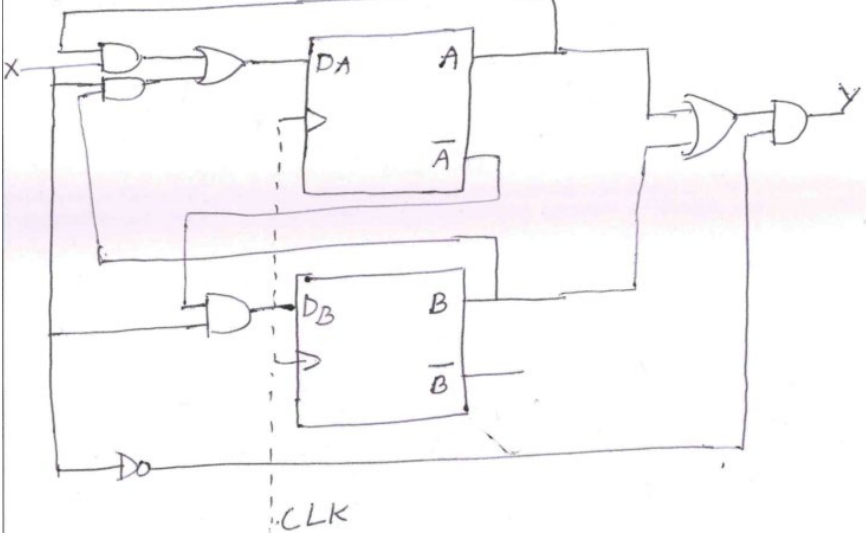
1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6.

PART-A

1	1.1	Subtract the following using 2's complement method i) -3 and +4 ii) -7 and -5	02
	1.2	Write the truth table and circuit of 2×4 decoder using basic gates.	02
	1.3	Give the differences between flip-flops and latches.	02
	1.4	Write the truth table and circuit of the 3-bit ripple counter using T-flip-flops.	02
	1.5	Construct the state table for the following state diagram in Fig. 1.5 <div align="center"> </div> <p align="center">Fig. 1.5</p>	02
	1.6	Mention the function of MAR and PC in computer.	02
	1.7	What are the two ways that byte addresses can be assigned?	02
	1.8	What is the significance of SP and FP in stack frame?	02
	1.9	Calculate the total memory locations if the computer having 16 address lines and 32 address lines.	02
	1.10	Write the control sequence for the instruction : <i>MOVE R2, (R1).</i>	02

PART-B

2	a	Write and explain the circuit arrangement for binary division along with restoring and non-restoring algorithms.	08
	b	Design a circuit such that it has four inputs w, x, y, z and one output F . D_1 and D_2 represent two binary numbers each consisting of two bits wx and yz respectively. The output F is to be HIGH only if $ D_1 - D_2 < 2$. Write the truth tables, using K-map technique. Find a minimum sum of product form and implement using basic gates.	08
3	a	Illustrate the working of Master-Slave JK flip-flop along with its circuit diagram, truth table and timing diagram.	08
	b	Write and explain the following circuit using D flip-flop i) Serial left shift ii) Serial right shift iii) Ring counter iv) Johnson Counter	08

		<p style="text-align: center;">OR</p> <p>4 a Write the circuit diagram, characteristic table, characteristic equation and excitation table for the following i) SR flip-flop ii) JK flip-flop</p> <p> b Design Synchronous counter for the sequence in Fig. 4b using T flip-flop.</p> <div style="text-align: center;">  <p>Fig. 4b</p> </div>	<p>08</p> <p>08</p>
		<p>5 a Write the State table, reduced State table and reduced State diagram for the State diagram in Fig. 5a</p> <div style="text-align: center;">  <p>Fig. 5a</p> </div> <p> b Briefly explain functional units of a computer with a neat diagram.</p> <p style="text-align: center;">OR</p> <p>6 a Derive the state equation, output equation, state table and state diagram for the sequential circuit in Fig. 6a</p> <div style="text-align: center;">  <p>Fig. 6a</p> </div> <p> b Write the interface connection between processor and memory and also explain the steps to execute instruction <i>ADD R0, LOCA.</i></p>	<p>08</p> <p>08</p> <p>08</p> <p>08</p>

7	a	Give the importance of the following assembler directives. i) EQU ii) ORIGIN III) Dataword iv) Reserve v) END vi) RETURN	06
	b	Write the assembler syntax and effective address for the following addressing modes: I) Register ii) Absolute iii) Index iv) Autoincrement	04
	c	Illustrate the working of subroutine with example	06
8	a	With example explain direct-mapped cache and associative-mapped cache.	08
	b	Discuss about execution of complete instruction and also write the control sequence for the following instruction execution i) <i>ADD (R3),R1</i> ii) Unconditional Branch	08