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RV COLLEGE OF ENGINEERING®

(Autonomous Institution affiliated toVTU)

III Semester B. E. Fast Track ExaminationsJuly-19

Computer Science and Engineering

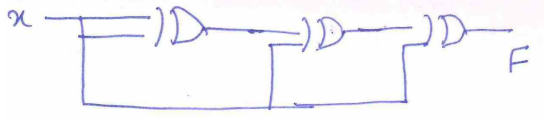
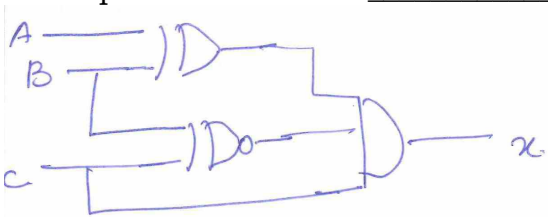
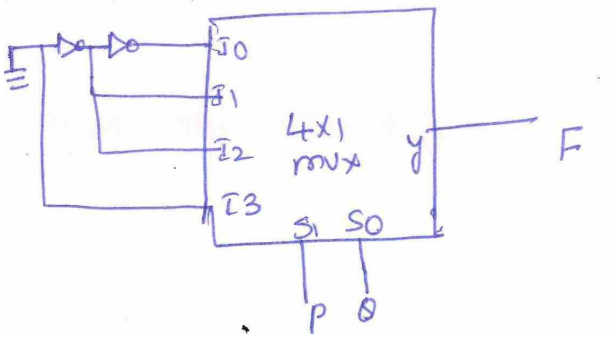
LOGIC DESIGN

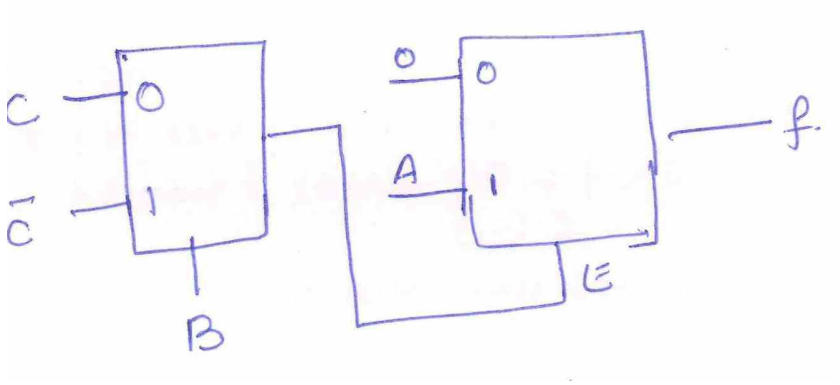
Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B.In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

PART-A

1	1.1	The output of a logic gate is '1' when all its input are at logic. The gate is either _____ or _____.	01
	1.2	For the circuit shown below Fig 1.2, the output F is given by  Fig 1.2	02
	1.3	How many AND, OR and EX-OR gates are required for the configuration of full adder?	02
	1.4	For the logic circuit shown in fig 1.4, the required input condition (A,B,C) to make the output $x = 1$ is ABC=_____.  fig 1.4	02
	1.5	What will be the output of multiplexers shown below in fig 1.5?  Fig 1.5	02

	1.6	The Boolean function f implemented in the figure 1.6 using two input multiplexer is _____.  Fig 1.6	02
	1.7	The canonical sum of product form of the function $y(A,B) = A + B$ is _____.	01
	1.8	The odd parity generator output of decimal number 9 is _____.	01
	1.9	Define registers.	01
	1.10	Write the characteristics equation of SR,JK, T and D.	02
	1.11	Define race around condition.	02
	1.12	Give the excitation table for SR and JK F/F.	02

PART-B

2	a	Apply K-map method to determine the SOP and POS expressions for the given functions. i. $y(A,B,C,D) = \sum m(0,4,7,8,9,11) + d(1,6)$ ii. $y(A,B,C,D) = \sum m(0,1,5,7,10,13,14) + d(2,4)$ iii. $y(A,B,C,D) = \prod m(2,4,6,8,9,10,12,14)$	06
	b	Explain with example the static and dynamic hazard in logic circuits.	04
	c	Find all the prime implicants of the function $f(a,b,c,d) = \sum m(7,9,12,13,14,15) + dc(4,11)$ using Quine –mcClusky algorithm.	06

3	a	Explain carry look ahead adder with a necessary expressions and diagram.	06
	b	With an eat diagram explain the decimal adder.	04
	c	Implement the Boolean function $f(a,b,c,d) = \sum m(4,5,7,8,10,12,15)$ using a 4 to 1 line MUX and external gates if, i. a and b are connected to select lines a_1 *and* a_0 respectively. ii. c and d are connected to select lines a_1 *and* a_0 respectively.	06
		OR	
4	a	Use active low 3 to 8 line decoder and 2 AND gates to implement the following function: $f_1(x_0,x_1,x_2) = \sum m(0,2,6,7)$ $f_2(x_0,x_1,x_2) = \sum m(3,5,6,7)$	04
	b	Configure a 4 to 16 line decoder using 2 to 4 line decoder.	04
	c	Implement the following Boolean functions using a PROM PLD $f_1(a,b,c) = \sum m(2,4,6,7)$ $f_2(a,b,c) = \sum m(0,1,2,5,)$ $f_3(a,b,c) = \sum m(2,6,7)$	04

	d	Implement the following functions using $3 \times 4 \times 2$ PLA. $f_1(a,b,c) = \sum m(1,2,3,7)$ $f_2(a,b,c) = \sum m(1,5,7)$	04

5	a	Define set-up time, hold time and propagation delay with necessary timing diagrams.	06
	b	Using excitation table, present state and next state table of F/F convert JK F/F to SR F/F.	06
	c	Explain the switch Debouncer circuit using SR latch with necessary diagram.	04
		OR	
6	a	Design a 4-bit registers using positive edge triggered D flip flops to operate as indicated in the table below:	

Mode Select		Register Operation
a_1	a_0	
0	0	Hold
0	1	Synchronous clear
1	0	Complement content
1	1	Circular shift right

10

	b	With neat circuit diagram and timing diagram explain positive edge triggered D F/F.	06

7	a	Design a mod -5 up control using asynchronous, with necessary timing diagram.	06
	b	Design a mod 6 synchronous up counter using positive edge triggered JK F/F.	10

8	a	Design a synchronous circuit using Positive edge triggered JK F/F with minimal combinational gating to generate the following sequence. $0 \rightarrow 1 \rightarrow 2 \rightarrow 0 \; if \; input \; x = 0 \; and$ $0 \rightarrow 2 - 1 - 0 \; if \; input \; x = 1$ Provide an output which goes high to indicate the non-zerostate in the $0 - 1 - 2 - 0$ sequence.Is this amealy machine?	10
	b	In detail explain the mealy or moore model with necessary diagrams.	06