16CS35/12CS35

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RV COLLEGE OF ENGINEERING®

(Autonomous Institution affiliated toVTU)

III Semester B. E. Fast TrackExaminationsJuly-19

Computer Science and Engineering

COMPUTER ORGANIZATION

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B.In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

PART-A

1	1.1	The following two statements cause the values 300 to be stored in location 1000, but at different times: i. ORIGIN 1000 DATAWORD 300 ii. MOV #300, 1000 Identify and illustrate the difference.	02
	1.2	Assume the following register and memory contents in an ARM computer: i. Register R_o contains 1000 ii. The numbers 1,2,3,4,5 *and* 6 are stored in successive word locations starting at memory address 1000. What is the effect of executing the following sequence of instructions. Identify the contents of register $R_0, R_8 R_9$ *and* R_{10} after executing the sequence of instructions. $LDR\ R_8, [R_O]$ $LDR\ R_9, [R_O, \#4]$ ADD R_{10}, R_8, R_9.	02
	1.3	Name the signal used during a configuration operation that causes the device to be selected.	01
	1.4	The Universal Serial Bus (USB) operates on the basis of _____.	01
	1.5	Why is the wait –for memory function completed step needed, when reading from or writing to the main memory?	01
	1.6	State an advantage of DDR-SDRAM.	01
	1.7	Define page fault.	01
	1.8	In many computers the cache block size is in the range of 32 to 128 bytes. Indicate the advantage and disadvantage of making the size of cache block larger or smaller.	02
	1.9	Construct the Booth recording of a multiplier for the following sequence. 0101101100101001	01

	1.10	Consider the following signed 6 bit binary numbers represented in 2's complement.Perform addition, specify whether or not arithmetic overflow occurs. 010110 +001001	01
	1.11	Represent the number +2.25 in IEEE standard floating point formats for single precision.	01

	1.12	Consider the following code segment. Assume each instruction takes 4 clock cycles to complete.
		$Add\ R_1, R_2$
		Sub R_3, R_4
		$Add\ R_5, R_6$
		Sub R_7, R_8
		Identify the number of clock cycles required when executed on
		i. Sequential processor
		ii. Pipelined processors with 4 stages.
			02

	1.13	The following code segment has to be loaded at memory address 1000. Indicate the necessary changes required for loading the program at address 1000. $MOVE\ N, R_1$ MOVE #NUM, R_2 $CLEAR\ R_o$ $LOOP\ ADD\ (R_2) + R_o$ $DEC\ R_1$ $BGT2\ LOOP$	01
	1.14	List any two possibilities of increasing the clock rate.	01
	1.15	Consider the number 25. If this value is to be used as an immediate operand, it can be given as decimal number as in the instruction $VE\ \#25, R_2$. Give the similar representation for this instruction if the value given is in i. Binary ii. Hexadecimal.	02

PART-B

2	a		Write a program to evaluate the expression $A * B + C * D$ in a single accumulator processor. Assume that the processor has Load, Store, Multiply and Add instructions and that all values fit in the accumulator.	04
	b		Identify the basic steps required to execute the machine instruction ADD LOCA, R_o in terms of transfer between the components of a processor, memory and some control commands with the help of neat diagram.	05
	c		Define addressing mode. Demonstrate the addressing functions for any three addressing modes with an example for each.	07

3	a	Consider a register R_5 used to point to the top of a stack in a program. Write sequence of instructions using the Index, Auto increment and Auto decrement addressing modes to perform each of the following tasks. i. PoP the top two items off the stack , add them and then Push the result onto the stack. ii. Copy the fifth item from the top into register R_3. iii. Remove the top ten items from the stack assembly language.	05
	b	Write an ARM assembly language program to add N numbers.	05
	c	Illustrate and discuss the structure of ARM registers. Explain the significance of each register.	06
		OR	
4	a	With an appropriate example discuss the indexed addressing modes used in ARM Processor.	08
	b	Consider the following possibilities for saving the return address of a subroutine. i. In a processor register ii. In a memory location associated with the call, so that a different location is used, when the subroutine is called from different places. iii. On a stack. Which of these possibilities supports subroutine nesting and which supports subroutine recursion.	04
	c	Write sequence of instructions for safe PoP and Push operations.	04

5	a	Three devices A, B and C are connected to the bus of a computer. I/O transfers for all three devices use interrupt control . Interrupt nesting for devices A and B is not allowed, but interrupt requests from C may be accepted while either A or B is being serviced. Suggest different ways in which this can be accomplished in each of the following cases: i. The computer has one interrupt request-line ii. Two interrupt- request lines INTR1 and INTR2 are available, with INTR1 having higher priority. Specify when and how interrupts are enabled and disabled in each case.	06
	b	With the help of neat timing diagram discuss how a read operation is performed on PCI bus.	10
		OR	
6	a	Write an ISR to read a line of characters from a keyboard and discuss how it is different from program controlled I/O operation.	08
	b	Explain the hardware registers that are required in a DMA controller chip. Why is it necessary for a DMA controller to be able to interrupt the processor? Explain.	08

7	a	Assume a system having a main memory with 16MB of addressable locations and a 32 kilobyte (KB) direct mapped, Cache with 8 bytes per block. The minimum addressable unit is a byte. i. How many blocks are there in the cache? ii. Show how the main memory address is partitioned.	04

	b	Discuss how an address generated by the processor gets translated into a main memory address.	08
	c	Differentiate between static RAMs and dynamic RAMs.	04

8	a	Illustrate and differentiate the approaches used to generate the control signals to execute the instructions.	08
	b	Multiply the pair of signed 2's complement numbers using the Booth algorithm, where A represent multiplicand and B is multiplier. $A = 110011\ and\ B = 101100$	04
	c	Divide 15/3 using non restoring technique.	04