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RV COLLEGE OF ENGINEERING®

(An Autonomous Institution affiliated to VTU)

III Semester B.E. Fast-track Examinations January-2023

Computer Science and Engineering

LOGIC DESIGN

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

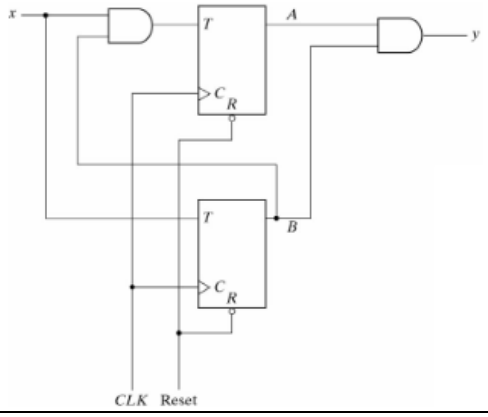
PART-A

1	1.1	_____and _____ are Universal gates	02
	1.2	A 3 variable K-map has _____cells.	01
	1.3	The minterm designator for the term : $\bar{A}\,B\,\bar{C}\,D$is _____	01
	1.4	0011 is a valid BCD member. Justify	01
	1.5	16:1 Multiplexer circuit will have _____select lines	01
	1.6	The filpflop that follows the input is a _____flip flop	01
	1.7	Draw the logical diagram of a 1 bit magnitude comparator	02
	1.8	Draw the timing diagram of a 2 bit down counter with negative edge triggered flip flops.	02
	1.9	A counter with 4 flip flops will have _____unique states	01
	1.10	Write the truth table and block diagram of 2:4 line decoder.	02
	1.11	_____is an IC with programmable gates divided into an AND array and an OR array to provide an AND –OR- SOP implementation	01
	1.12	What are state diagrams? Given an example	02
	1.13	What is the supply voltage level of TTL IC's	01
	1.14	Define a register.	01
	1.15	A n-stage Johnson counter has _____states	01

PART-B

2	a	Minimize the following Boolean expressions using K map. i. F(A, B, C, D) = Σm(0, 1, 2, 5, 7, 8, 9, 10, 13, 15) ii. F(A, B, C, D) = Σm(1, 3, 4, 6, 8, 9, 11, 13, 15) + Σd(0, 2, 14)	08
	b	Simplify the following Boolean function, f(w,x,y,z)=Σ(0,2,5,7,10,13,14,15) using Quine-McClukey tabular method.	08
3	a	With a neat diagram explain a decimal adder	08
	b	Implement the Boolean function using 8: 1 and also using 4:1 multiplexer F (A, B, C, D) = ∑m (0, 1, 2, 4, 6, 9, 12, 14)	08

OR

4	a	Explain 2 bit magnitude comparator	08
	b	Design a full adder and subtractor using 3 to 8 line decoder	08
5	a	What is race condition? How this can be avoided? Illustrate how Master-Slave JK flip flop overcomes this problem.	10
	b	With relevant function table and symbols explain positive edge triggered D flip flop.	06
		OR	
6	a	What are shift registers? Explain with diagram SISO and SIPO unidirectional shift registers.	08
	b	With a neat diagram explain universal shift register.	08
7	a	Design a synchronous counter to count the following sequence 7,4,3,1,5,0,7,4,3,... Implement the circuit using T-flip-flops.	08
	b	Design a Mod 4 synchronous up-counter using JK flip flop	08
8	a	Differentiate between Mealy model and Moore models synchronous sequential networks	08
	b	Construct the excitation table, transition table, state table and state diagram for the following sequential circuit. 	08