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# RV COLLEGE OF ENGINEERING®

**(An Autonomous Institution affiliated to VTU)**

**III Semester B.E. Fast Track Examinations January - 2023**

## Computer Science and Engineering

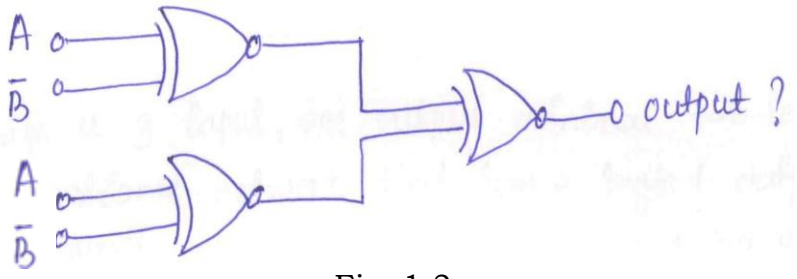
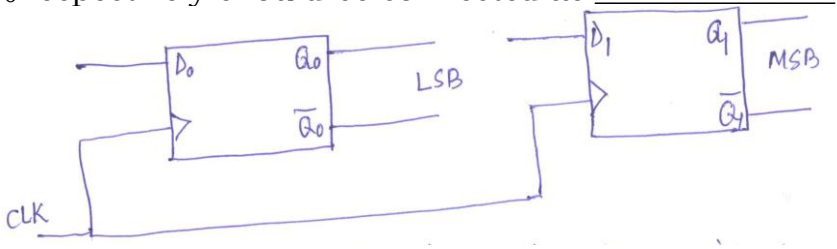
## FOUNDATIONS OF COMPUTER SYSTEMS DESIGN

***Time: 03 Hours*** ***Maximum Marks: 100***

***Instructions to candidates:***

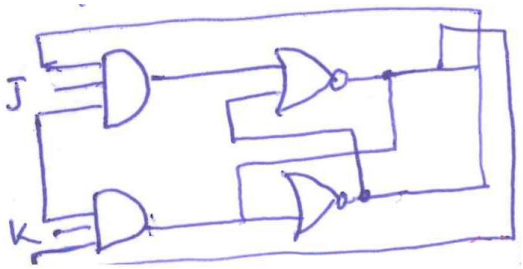
1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

### PART-A

| | | | |
|---|---|---|---|
| 1 | 1.1 | Subtract $(101010)_2$ from $(10010)_2$ in 2's complement format. | 02 |
| | 1.2 | Write down the algorithm for non-restoring division | 02 |
| | 1.3 | Write down the output of the circuit shown below   Fig. 1.3 | 02 |
| | 1.4 | Realize a half subtractor circuit using minimum number of 2:1 MUX | 02 |
| | 1.5 | Convert a JK flipflop to T flipflop | 02 |
| | 1.6 | A 0 *to* 6 counter consists of 3 flipflops and a combination circuit of 2 input gates. Which gate / gates are best suitable for the combination circuit? | 02 |
| | 1.7 | Two D flipflops are to be connected as s synchronous counter as shown below, that goes through the following $Q_1Q_0$ sequence $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow$ The $D_1D_0$ respectively should be connected as _____   Fig. 1.7 | 02 |
| | 1.8 | Two processors A and B have clock frequencies of 700Mhz and 900Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of same instruction which processor is faster? | 02 |

| | | | |
|---|---|---|---|
| | 1.9 | Write the assembly code for the expression $C = A + B * D$. | 02 |
| | 1.10 | A computer has a single cache (off-chip) with a 2ns hit time and a 98% hit rate. Main memory has a 40ns access time. What is the computers effective access time? | 02 |

**PART-B**

| | | | |
|---|---|---|---|
| 2 | a | Design a three input, one output minimal two–level gate combinational network that has a logic-1 output, when the majority of inputs are logic 1 and has a logic – 0 output when the majority of its inputs are logic – 0. | 05 |
| | b | Using a $4-bit$ binary adder, design a network to convert a decimal digit in 8421 code into a decimal digit in excess 3 code. | 05 |
| | c | Realize the Boolean expression $f(w,x,y,z) = \sum m(4,5,7,8,10,12,15)$ using a $4\ to\ 1$ line multiplier and external gates.<br>i) Let $w$ and $x$ appear on the select lines $S_1$ and $S_0$ respectively<br>ii) Let $y$ and $z$ appear on the select lines $S_1$ and $S_0$ respectively | 06 |
| | | | |
| 3 | a | A logic diagram and a function table for a proposed gated $JK$ latch is shown in Fig. 3.a. Discuss the problems that can be encountered with this network and under what constraints proper $JK$ flipflop behavior is achieved? | |
| | |  | |
| | | $J$ $K$ $C$ $Q^+$ $\bar{Q}^+$<br>0 0 1 $Q$ $\bar{Q}$<br>0 1 1 0 $Q$<br>1 0 1 1 0<br>1 1 1 $\bar{Q}$ $Q$<br>$X$ $X$ 0 $Q$ $\bar{Q}$ | |
| | | Fig. 3.a | 04 |
| | b | Design a register incorporating four multiplexer and four positive edge triggered D flipflops, having the behavior specified in the below table 3.b. | |
| | | Table. 3.b<br>*Select lines* $S_1$ $S_0$ \| *Register operations*<br>0 0 \| *Hold*<br>0 1 \| *Synchronous clear*<br>1 0 \| *Complement contents*<br>1 1 \| *Circular shift right* | 04 |
| | c | Design a synchronous mod-6 counter whose counting sequence is $000 \rightarrow 001 \rightarrow 100 \rightarrow 110 \rightarrow 111 \rightarrow 101 \rightarrow 000$ etc by obtaining its minimal sum equations use positive edge triggered D-flipflop. | 08 |
| | | **OR** | |
| 4 | a | Design and explain $4-bit$ binary ripple up-counter using a positive edge triggered D-flipflop. Do not include a count enable line. | 08 |
| | b | Verify the characteristic equation for the JK, D and T flipflops by constructing appropriate K-maps and obtaining the minimal sums. | 08 |

5 a For the clocked synchronous sequential network shown in Fig. 5.a, construct the excitation table, transition table, state table and state diagram.

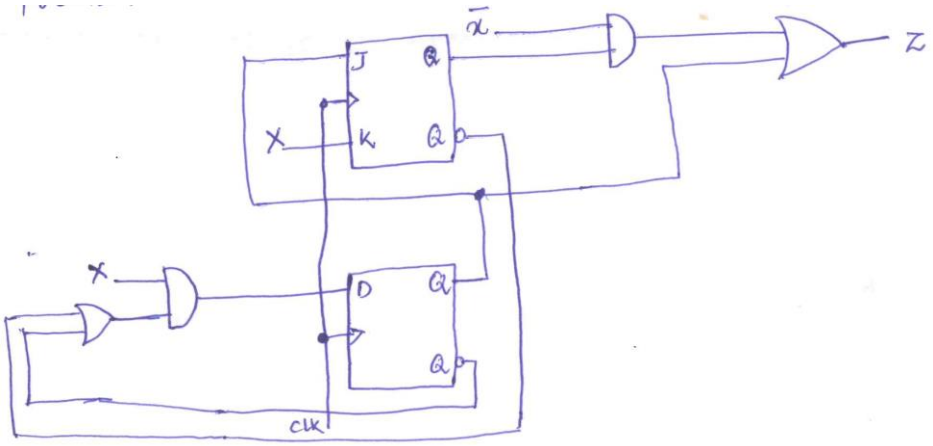



Fig. 5.a 10

b List the steps needed to execute the machine instruction $SUB(R_1), R_2$. Explain the steps in terms of basic operational concept of the computer. Assume that the instruction is stored in memory at location $X$ and the address of same in the PC register. 06

**OR**

6 a Obtain a minimal state table for a clocked synchronous sequential network having a single input line $x$, in which the symbols 0 and 1 are applied, and a single output line $z$. The network is to produce an output of 1 coincident with each input 1 if it is immediately preceeded by at least three $1's$. At all other times the network is to produce output as 0. An example of input/output that satisfies the condition is given below.

$x = 01100111111 \quad 000111101$

$z = 00000000111 \quad 000000100$ 06

b The state table of a clocked synchronous sequential network is given below. Assigning codes in binary order to the states, determine minimal sum excitation and output expressions for the sequential network assuming the use of a D flipflops.

| *Present state* | *Next state* | | *Output* $(z)$ | |
|---|---|---|---|---|
| | *Input* $(x)$ | | *Input* $(x)$ | |
| | $x = 0$ | $x = 1$ | $x = 0$ | $x = 1$ |
| $A$ | $B$ | $A$ | 0 | 0 |
| $B$ | $A$ | $C$ | 1 | 0 |
| $C$ | $D$ | $A$ | 0 | 0 |
| $D$ | $D$ | $E$ | 1 | 0 |
| $E$ | $C$ | $D$ | 1 | 1 |

10

7 a Explain the instruction execution and straight line sequencing with a neat diagram and also explain branching with example program. 06

b Define addressing mode with an example for each explain any five addressing modes. 10

| | | | |
|---|---|---|---|
| 8 | a | The size of the physical address space of a processor is $2^p$ bytes. The word length is $2^w$ bytes. The capacity of cache memory is $2^N$ bytes. The size of each cache block is $2^M$ words. For a K-way set associative cache memory, determine the length of the tag field. | 04 |
| | b | A block set associative memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit words.<br>i) How many bits are required for addressing the main memory?<br>ii) How many bits are needed to represent the TAG, SET and WORD fields. | 06 |
| | c | Explain the single bus organization of the data path inside a processor with supporting block diagram. | 06 |