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RV COLLEGE OF NGINEERING®

(An Autonomous Institution Affiliated to VTU)

III Semester B. E. Examinations April/May-2023

Computer Science and Engineering

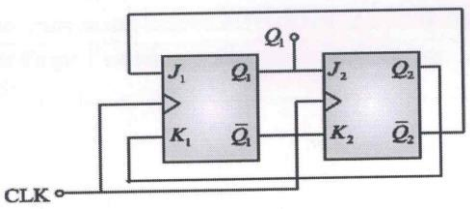
FOUNDATIONS OF COMPUTER SYSTEMS DESIGN

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2 is compulsory. Answer any one full question from 3 and 4, 5 and 6, 7 and 8, 9 and 10.

PART-A

1	1.1	Represent the number 263.3 in 32 bit floating point representation.	02
	1.2	Identify the logic gate utilized in the following applications: a) Two way switch b) To access a bank locker c) Duplicate key to open the door of a house d) Detection of 1 bit errors in digital communication	02
	1.3	Represent the following expression using only 2 input $NAND$ gates: $(AB + A'B')(CD' + C'D)$	02
	1.4	Design a 32 to 1 multiplexer, using lower order multiplexers.	02
	1.5	Realize (conversion) the following: JK flip flop using SR flip flop.	02
	1.6	Multiply $+13$ with -6 using bit pair recoding.	02
	1.7	Registers $R4$ and $R5$ contain the decimal numbers 2000 and 3000 before each of the following addressing modes is used to access a memory operand. What is the effective address (EA) in each case? a) Add $12(R4), R5$ b) Move $(R4, R5), R0$	02
	1.8	Illustrate with examples any two assembler directives.	02
	1.9	The outputs of the two flipflops $Q1, Q2$ in the Fig. 1.9 are initialized to $0, 0$. Give the sequence generated at $Q1$ upon the application of clock signal.  Fig. 1.9	02
	1.10	A program contains 1000 instruction, out of that 25% of instructions requires 4 clock cycles, 40% instruction required 5 clock cycles and remaining required 3 clock cycles for execution. Find the total time required to execute the program running on a $1GHz$ machine.	02

PART-B

2 a A small company has 100 shares of stock and each share entities its owner to vote at a stockholders meeting. Mr. A owns 10 shares, Mr. B owns 20 shares, Mr. C owns 30 shares and Mr. D owns 40 shares. A two-thirds majority is required in order to pass a measure at a stockholders meeting, Each of the four stockholders has a switch which he or she closes to vote 'yes' for all of his or her shares and opens to vote $'no'$. A switching circuit is to be designed to turn on a light if the measure passes

i) Derive a truth table for the output function Z

ii) Write the minterm expansion for Z and simplify using K map

iii) Design two level gate logic diagram using the simplified SoP. 06

b A logic network has two data inputs A and B, and two control inputs $C0$ and $C1$. It implements the function F according to the following table $USING\ 4\ TO\ 1\ MUX$ and appropriate gates.

$C1$	$C0$	$Function\ performed\ By\ network\ F$
0	0	$(A+B)'$
0	1	$A+B$
1	0	$A\ XOR\ B$
1	1	$A\ XNOR\ B$

06

c Using restoring division algorithm, divide 1000 by 0011, show the steps. 04

3 a Mention the problem posed by JK flip flop, realize the Master Slave JK flip flop using only $NAND$ gates, and describe how the Master Slave JK flip flop solves this issue. Show the truth table and waveforms. 06

b Derive the characteristic equation and excitation table for SR and JK flip flops. 04

c Explicate $0's$ and $1's$ catching problem present in JK flip flop. How can this problem be resolved? 06

OR

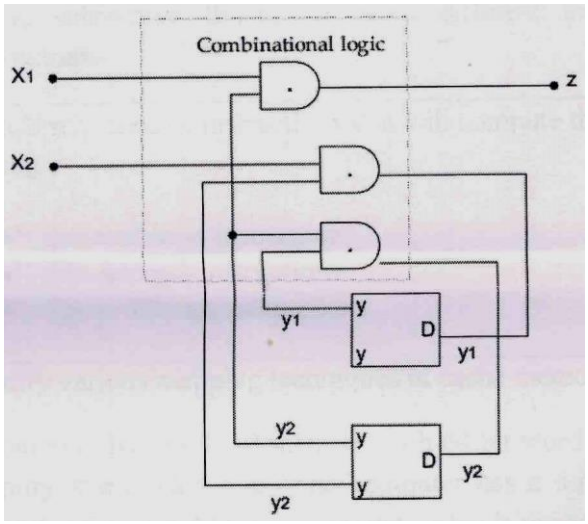
4 a A positive edge triggered D flip flop is connected to a positive edge triggered JK flip flop. The Q output of the D flip flop is connected to both the J and K inputs of the JK flip flop, while the Q output of the JK flipflop is connected to the input of the D flip flop. Initially, the output of the D flip flop is set to logic one and and the output of the JK flip flop is cleared. What is the bit sequence generated at the Q output of the JK flip flop when the flip flops are connected to a free running common clock? Both the flip flops have non zero propagation delays. 02

b Design a self-correcting $Mod\ 5$ Synchronous up counter using JK flip flops, move the unused states to 0 state. 08

c Design a $4-bit$ Universal shift register using positive edge triggered D flip- flops to operate as indicted in the table below.

$Mode\ Select$		$Register\ Operation$
$A1$	$A0$	
0	0	$Complement\ contents$
0	1	$Circular\ Shift\ Right$
1	0	$Shift\ left$
1	1	$Parallel\ load$

06

5	a	Analyze the following circuit in Fig. 5.a by deriving the excitation equations, transition equations, excitation table, transition table and state diagram.  Fig. 5.a	10
	b	Model the serial binary adder Mealy and Moore networks and show the state table.	06
		OR	
6	a	Give any four differences between mealy and moore models. Recognize the sequence 0110/1001 using mealy model.	08
	b	For the state table given in Table 6.b, eliminate the redundant states using Row elimination implication table method. Show the reduced state table and state transition diagram.	

Present State	*Next State*		*Output*
	$x = 0$	$x = 1$	
S_0	S_1	S_2	1
S_1	S_3	S_5	1
S_2	S_5	S_4	0
S_3	S_1	S_6	1
S_4	S_5	S_2	0
S_5	S_4	S_3	0
S_6	S_5	S_6	0

08

7	a	List and explain the basic steps needed to execute the machine instruction $ADD\ LOCA, R0$ in terms of transfers between the components of processor, memory and some control commands.	04
	b	List and explain any five addressing modes with examples. A processor has 40 distinct instructions and 24 general purpose registers. A $32 - bit$ instruction word has an opcode, two registers operands and an immediate operand. Give the number of bits available for the immediate operand field.	08
	c	Describe the factors that affect the performance of the computer? Explain any two ways in which performance can be improved.	04
		OR	
8	a	Illustrate with a neat diagram, connections between the processor and the memory.	05
	b	Define subroutine linkage. Explain different mechanism of passing parameters to subroutines.	05

	c	Write a sequence of instructions that will compute the value of $y = x^2 + 3x + 6$ for a given x using: i) Three-address instructions ii) Two-address instructions iii) Zero-address instructions	06
9	a	Identify various mapping techniques in cache memory along with necessary diagrams. A computer has an $8GB$ memory with $64\,bit$ word sizes. ($1\,word = 4\,bytes$). Each block of memory stores 16 words. The computer has a direct-mapped cache of 128 blocks. The computer uses word level addressing. What is the address format?	08
	b	Write the control sequence, with comments for the execution of the following instructions, using Single bus and Three bus data paths. $ADD\ (R5), R3$.	08
		OR	
10	a	Examine all the memory types available under RAM and ROM, which are used in building embedded systems and Personal computers. Design $2M \times 32$ memory chip using $512k \times 8$ memory chip along with external connections.	08
	b	Illustrate with neat diagrams, hardwired control unit and micro programmed control unit and discuss their advantages and disadvantages.	08