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RV COLLEGE OF ENGINEERING®

(An Autonomous Institution affiliated to VTU)

III Semester B. E. Examinations Nov/Dec-19

Computer Science and Engineering

LOGIC DESIGN

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

PART-A

1	1.1	Simplify the Boolean expression : $A + \bar{A}B + AB$	02
	1.2	Write any two differences between karnaughs maps and Quine-Mcclusky methods used for simplification of Boolean expressions.	02
	1.3	Develop the simplified expression for carry of a full Adder.	02
	1.4	Mention static and dynamic hazards in logic circuits.	02
	1.5	Define the following: a) Multiplexer, b) Decoder.	02
	1.6	List any two applications of Flip flops.	02
	1.7	Draw the logic block diagram of a 4 bit Serial-in Serial-out ($SISO$) register.	02
	1.8	Distinguish between Synchronous and Asynchronous counter.	02
	1.9	What are the differences between Mealy and Moore model?	02
	1.10	Write the representation structure of an implication table.	02

PART-B

2	a	Simplify the following expression and realize the logic diagram using 2 input gates $f(A,B,C,D) = \sum m\,(4,5,8,9,11,12,13,15)$.	08
	b	Minimize the expression using Quine Mcclusky method for the following functions: $f(A,B,C,D) = \sum m\,(1,3,5,10,11,12,13,14,15)$.	08
3	a	Design a 4 bit adder using 4 full adders. Illustrate the working with an example.	08
	b	Write a Boolean expression for single bit magnitude comparator. Develop a logic circuit diagram for the obtained expressions.	08
		OR	
4	a	Draw and explain the logic diagram of a 4:1 multiplexer with the help of a truth table.	08
	b	Design and explain a basic three input and two output $PLA's$.	08

5	a	Develop the logic circuit diagram and explain the operation of a master-slave JK flip flop.	08
	b	Using the truth table and logic circuit diagram, explain the working of $NAND$ latch.	08
		OR	
6	a	Construct 4 bit parallel-in-parallel-out ($PIPO$) shift register and explain the working operation along with a neat wave form diagram.	08
	b	Discuss the different applications of shift register in realization of logic circuits.	08
7	a	Design a modulo-5 counter using JK-flip flop. Explain its action by writing a truth table and waveforms for the outputs of the flip flop.	08
	b	Write the design excitation aspects of the following flip flop: i) D-flip flop ii) JK-flip flop.	08
8	a	Draw and explain a Mealy model of a clocked synchronous sequential network in detail.	08
	b	Develop and explain a state diagram for a Moore serial binary adder.	08