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# RV COLLEGE OF ENGINEERING®
**(An Autonomous Institution affiliated to VTU)**
**III Semester B. E. Examinations April/May - 2023**
## Computer Science and Engineering
# LOGIC DESIGN

*Time: 03 Hours*                                    *Maximum Marks: 100*
*Instructions to candidates:*
   1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
   2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

## PART-A

| 1 | 1.1 | What are state diagrams and state tables? | 02 |
|---|---|---|---|
| | 1.2 | 16:1 multiplexer circuit will have _____ select lines. | 01 |
| | 1.3 | The minterm designator for the term $\overline{A}BC\overline{D}$ is _____. | 01 |
| | 1.4 | A n-stage Johnson counter has _____ states. | 01 |
| | 1.5 | _____ is an $IC$ with programmable gates divided into an $AND$ array and an $OR$ array to provide an $AND - OR - SOP$ implementation. | 01 |
| | 1.6 | The flip-flop that follows the input is a _____ flip-flop. | 01 |
| | 1.7 | Draw the logical diagram of a 1bit magnitude comparator. | 02 |
| | 1.8 | Define a register. | 01 |
| | 1.9 | A counter with 4 flip-flops will have _____ unique states. | 01 |
| | 1.10 | Write the truth table and block diagram of $2:4$ line decoder. | 02 |
| | 1.11 | Draw the timing diagram of a 2 bit down counter with negative edge triggered flip-flops. | 02 |
| | 1.12 | What is the supply voltage level of $TTL\ IC's$? | 01 |
| | 1.13 | Simplify the Boolean expression: $Y = \overline{(A + B + C) + (B + \bar{C})}$ | 02 |
| | 1.14 | How many JK flip-flops are required to achieve the frequency division of 8? | 01 |
| | 1.15 | A device which converts $BCD$ to seven segment is called _____. | 01 |

## PART-B

| 2 | a | Minimize the following Boolean expression using K map:<br>    i)    $F(A, B, C, D) = \sum m(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$<br>    ii)    $F(A, B, C, D) = \sum m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \sum d(0, 2, 14)$ | 08 |
|---|---|---|---|
| | b | Simplify the following Boolean function $f(w, x, y, z) = \sum(0, 2, 5, 7, 10, 13, 14, 15)$ using Quine-McCluskey tabular method. | 08 |
| | | | |
| 3 | a | With a neat diagram, explain a decimal adder. | 08 |
| | b | Implement the Boolean function using 8:1 and also using 4:1 multiplexer $F(A, B, C, D) = \sum M(0, 2m\ (0, 1, 2, 4, 6, 9, 12, 14)$. | 08 |

| | | | |
|---|---|---|---|
| | | **OR** | |
| 4 | a | Explain 2 bit magnitude comparator. | 08 |
| | b | Design a full adder and subtractor using 3 to 8 line decoder. | 08 |
| | | | |
| 5 | a | What is race condition? How this can be avoided? Illustrate how Master-Slave *JK* flip-flop overcomes this problem? | 10 |
| | b | With relevant function table and symbols, explain positive edge triggered *D* flip-flop. | 06 |
| | | **OR** | |
| 6 | a | What are registers? Explain with diagram *SISO* and *SIPO* unidirectional shift registers. | 08 |
| | b | With a neat diagram, explain universal shift register. | 08 |
| | | | |
| 7 | a | Design a synchronous counter to count the following sequence $7, 4, 3, 1, 5, 0, 7, 4, 3, ....$ Implement the circuit using *T* flip-flops. | 08 |
| | b | Design a mod 4 synchronous up-counter using *JK* flip-flop. | 08 |
| | | | |
| 8 | a | Differentiate between Mealy model and Moore models synchronous sequential networks. | 08 |
| | b | Construct the excitation table, transition table, state table and state diagram for the sequential circuit shown in Fig 8b. | |
| | |  Fig 8b | 08 |