USN | | | | | | | | | | |

RV COLLEGE OF ENGINEERING®

(An Autonomous Institution affiliated to VTU)

III Semester B. E. Fast Track Examinations Oct-2020

Computer Science and Engineering

FOUNDATIONS OF COMPUTER SYSTEMS DESIGN

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

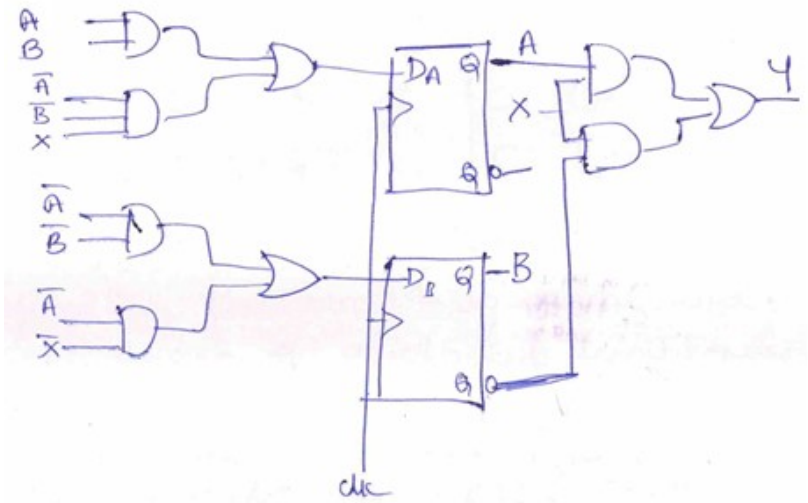
1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

PART-A

1	1.1	Consider the following bit pattern and represent the floating point number in $IEEE754$ single precision format. 11000011111100000000000000000000	02
	1.2	Find prime implicants and essential prime implicants of the following boolean fiction using K-map $f(a,b,c,d) = \sum m(0,2,5,7,8,10,13,15) + dc(1,4,11,14)$	02
	1.3	Implement the following function using a $3-8$ decoder with active low output $f(a,b,c) = \pi M(0,1,3,5,6)$	01
	1.4	Construct positive-edge-triggered T flip flop using D flip flop.	02
	1.5	Registers $R4$ and $R5$ contain the decimal numbers 2000 and 3000 before each of the addressing modes is used to access a memory operand. What is the effective addresses (EA) in each case i) $Add\ 12(R4), R5$ ii) $Move -(R4), R1$	02
	1.6	Write the Booth's recoded and bit pair recoded multiplier values for the number -6.	02
	1.7	Give the RTN(Register Transfer Notation) equivalent of the following instructions: i) $Move\ LOC, R1$ ii) $Add\ R1, R2, R3$	01
	1.8	Give the characteristic equation for The Toggle flip flop.	01
	1.9	Draw a state diagram of $753\bar{6}$ code sequence for mod 10 counter.	02
	1.10	Draw the state diagram of the serial binary adder.	02
	1.11	Define "Relative mode" in finding effective address (EA).	01
	1.12	List out the analysis procedure in designing a synchronous sequential networks.	02

PART-B

2	a	Divide the following numbers using restoring division method Divisor = 0011,Dividend = 1000.	05
	b	With a neat diagram describe how carry look ahead adder overcomes the problems of ripple carry adder	06
	c	Analyse the boolean function $f(a,b,c,d) = \sum m(0,1,5,6,7,9,10,15)$ using 4 to 1 mux(consider a, b as select lines)	05

3	a	Design and explain a synchronous mod−10 counter using positive edge triggered JK flip flops, whose counting sequence corresponds to the 5421 code by obtaining its minimal sum equations	10
	b	Describe how edge triggered 'D' flip flop over comes the problems of 0's and 1's catching problems.	06
		OR	
4	a	Design a self correcting mod-6 counter using SR flip flops(redirect all invalid states to 000)	08
	b	With a neat diagram, illustrate the working of universal shift register	08
5	a	Analyse and interpret the working of the sequential circuit given in fig 5a	
		 Fig 5a	08
	b	List and explain the basic steps needed to execute the machine instruction Add $LOCA, R0$ in terms of transfer between the components of processor, memory and some control commands with the help of neat diagram	08
		OR	
6	a	With implication table method achieve minimal state table for the state table given below:	

$Present\ state$	$Nest\ state$		$Output(z)$	
	$input(x)$		$input(x)$	
	0	1	0	1
A	A	B	0	0
B	D	C	0	1
C	F	E	0	0
D	D	F	0	0
E	B	G	0	0
F	G	C	0	1
G	A	F	0	0

			06
	b	Differentiate between Mealy model and Moore model of a clocked synchronous sequential network	04
	c	Discuss how the performance equation 'T' behaves in $CISC$ and $RISC$ instruction set	06

7	a	Write an assemble language program for finding the number of negative integers in a list of 'n' 32-bit integers and store in location $NEGNUM$.	05
	b	Illustrate the significance of the following assembler directives: i) Origin ii) $DATA\ WORD$ iii) $RESERVE$ iv) EQU v) END.	05
	c	Register $R5$ is used in a program to point to the top of a stack containing 32-bit number. Write a sequence of instructions using the index, Auto-increment and Auto-decrement addressing modes to perform each of the following tasks: i) Pop the top two items off the stack, add them, then push the result onto the stack ii) Copy the fifth item from the top into register $R3$ iii) Remove the top ten items from the stack For each case, assume that the stack contains ten or more elements.	06
8	a	Design $2M \times 8$ memory module using $512K \times 8$ memory chip and explain various external connections & its requirements in detail	06
	b	Mention different types memory mapping techniques of cache memory. Also explain each technique with the help of a neat diagram	06
	c	With the neat diagram explain three bus organization of the data path.	04