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RV COLLEGE OF ENGINEERING®

(An Autonomous Institution affiliated to VTU)

III Semester B. E. Fast Track Examinations Oct-2020

Computer Science and Engineering

LOGIC DESIGN

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

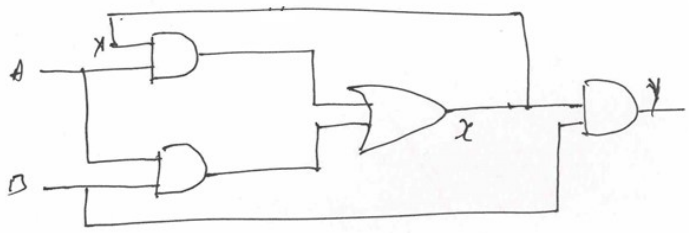
1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

PART-A

1	1.1	Realize the logic circuit for the Boolean equation $Y = A + B$ using $NAND$ gates.	02
	1.2	Construct the karnaugh map for the Boolean expression function $F(A,B,C,D) = \sum m(7) + d(10,11,12,13,14,15)$.	02
	1.3	Distinguish between static and dynamic hazards in logic devices.	02
	1.4	What is the maximum number of inputs for an OR gate in a 4-bit parallel adder?	01
	1.5	Perform 2's complement subtraction between -43 and -78.	02
	1.6	Show the clocked RS flip flop using only $NAND$ gates.	02
	1.7	Write any two differences between encoders and decoders.	02
	1.8	Distinguish between an edge-triggered and pulse triggered JK flip flop.	02
	1.9	Draw a logic circuit for positive-edge triggered JK flip flop.	02
	1.10	What is Ring counter?	01
	1.11	What modulus counter can be constructed with the use of five flip flops?	01
	1.12	Write the state sequence of a modulo-6 counter.	01

PART-B

2	a	Design a Karnaugh map for the Boolean equation expressed by minterms: $Y = F(A,B,C,D) = \sum m(7,9,10,11,12,13,14,15)$ Also write the simplified Boolean expression along with the corresponding logic circuit.	08
	b	Find all the prime implicants of the function $f(a,b,c) = \sum(0,1,2,5,6,7)$.Also design a logic circuit for the realized expression.	08
3	a	Using binary adder subtract logic block diagram, illustrate the working of 8 bit binary adder with an example.	08
	b	Design a 32 to 1 multiplexer using two 16-1 multiplexers and one 2 to 1 multiplexer. Illustrate the working operation of the logic circuit.	08
		OR	

4	a	Create a logic circuit to show multi input OR gates using a 3 to 8 decoder for the Boolean expression : $F1(A,B,C) = \sum m(0,4,6)$ $F2(A,B,C) = \sum m(0,5), F2(A,B,C) = \sum m(1,2,3,7)$	08
	b	With the help of a block diagram, truth table, analyze the working of two 1-bit comparator.	08
5	a	Draw the JK master-slave flip flop block diagram and briefly explain the operation with corresponding waveform and truth table.	08
	b	What is characteristic equation of a flip flop? Analyze the characteristic equations of SR and T-flip flop along with its truth table.	08
		OR	
6	a	Draw the waveforms to shift the numbers 0100 using 4-bit serial input shift register. Also explain its operation with the help of logic block diagram.	08
	b	Show how modulo-8 switched tail counter works if it is initialized with 1001. How to decode this counter?	08
7	a	Draw the logic diagram and waveforms for three-bit binary ripple counter. Also illustrate its working operation in detail along with the truth table.	10
	b	What are the differences between synchronous and asynchronous counters? Mention any two real-time applications of it.	06
8	a	What are the differences between Moore and Melay model. Using state transition diagram briefly explain each one in detail.	08
	b	Analyze the Melay model asynchronous sequential circuit shown in fig 8b and show its stable state and corresponding outputs. Give the state diagram of this circuit.  Fig 8b	08