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RV COLLEGE OF ENGINEERING®

(An Autonomous Institution affiliated to VTU)

III Semester B. E. Examinations April/May-2023

Computer Science and Engineering

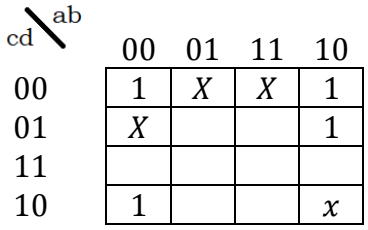
FOUNDATIONS OF COMPUTER SYSTEMS DESIGN

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

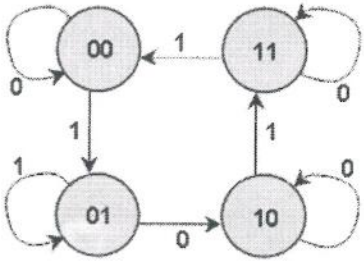
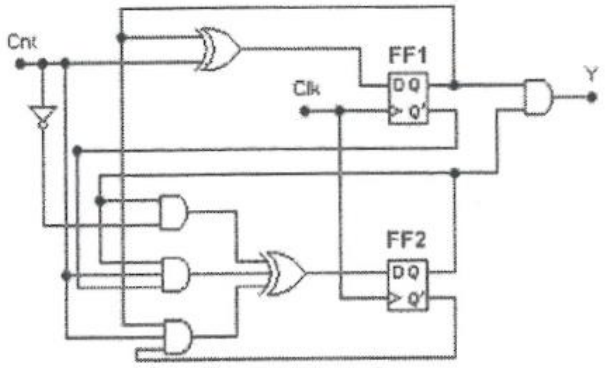
1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

PART-A

1	1.1	Define clock and clock rate	02
	1.2	Write a program that can be evaluate the expression $A * B + C * D$ in a single-accumulator processor. Assume that the processor has Load, Store, Multiply and Add instructions, and that all values fit in the accumulator.	02
	1.3	Derive the characteristic equation of SR flip flop.	01
	1.4	 What is the minimal form of the Karnaugh map shown above? Assume that X denotes a don't care term.	02
	1.5	Simplify the equation $F = AB + A(B + C) + B(B + C)$ into SOP form.	01
	1.6	With respect to cache memories, differentiate between write back protocol and write through protocol.	02
	1.7	Realize the function $f(a, b, c, d) = \Sigma m(1,4,5,7,9,12,13)$ using a 4 to 1 mux.	02
	1.8	List down the different assembler directives.	01
	1.9	Convert the following pairs of decimal numbers to 5-bit, signed, 2's complement, and binary and add them. State whether or not overflow occurs in each case. i) -14 and 11 ii) -10 and -13	02
	1.10	Write sum and carry Boolean expressions for a full adder.	02
	1.11	Summarize the algorithm for non restoring division	02
	1.12	List various conditional codes.	01

PART-B

2	a	Compare the performance of array multiplication with sequential circuit binary multiplier in terms of combinational logic. Also explain how Multiplicand = 1101 and Multiplier= 1011 can be multiplied using sequential binary multiplier.	10

	b	Demonstrate the multiplication process in bit-pair recoding for the values given 010111 and 110110	06
3	a	With a neat diagram explain SR flip-flop as an switch debouncer application	06
	b	Describe race around condition problem faced by JK flip-flop. Give solution for the same using master slave JK flip flop.	10
		OR	
4	a	Design mod-10 synchronous counter using JK flip-flops. Draw the neat state diagram and circuit diagram with Flip-Flops.	10
	b	Show with logic and timing diagrams how an asynchronous counter can be implemented having a modulus of 12 with a straight binary sequence from 0000 through 1011.	06
5	a	For the state diagram shown in Fig 5a, using JK flip flop draw the logic diagram of sequential circuit using JK flip flops.  Fig 5a	08
	b	A sequential circuit has two JK flip-flops A and B. Two inputs x and y and one output z. The flip-flop input functions and the circuit output functions are as follows: $JA = Bx + B'y'$ $JB = A'x$ $KA = B'xy'$ $KB = A + xy'$ $z = Axy + Bx'y'$ i) Draw the logic diagram of the circuit. ii) Tabulate the state table. iii) Derive next state equations for A and B.	08
		OR	
6	a	Derive the next state, the output table and state diagram for the sequential circuit shown in Fig 6a  Fig 6a	08
	b	With a neat block diagram explain the connections between the processor and memory.	08

7	a	Define addressing modes. Explain any 5 addressing modes with examples	04
	b	Write the subroutines for a safe pop operation and safe push operations to check stack full and stack empty respectively.	06
	c	Discuss the different ways in which parameters are passed to subroutines with illustrative examples.	06
8	a	Design $2M * 32$ memory module using $512k * 8$ memory chip and explain various external connections	06
	b	With the neat diagram of three bus organization of the data path, demonstrate the control sequence for the instruction $Add\ R4, R5, R6$.	10