	R V College of Engineering Department of Computer Science and Engineering CIE - I : (Test1) Question Paper		
Course: (Code)	APPLIED DIGITAL LOGIC DESIGN AND COMPUTER ORGANIZATION (CS234AI)		Semester : 3rd BE
Date : 9th Jan 2024	Duration : 90 minutes	Staff :	KB/PSB/MH/DD
Name :	USN :	Section :	A/B/C/D/CD/CY

Sl. no	Answer all the questions	Marks	L1-L6	CO
1	i) Simplify the Boolean function using QM Method. F (P, Q, R, S) = ∑ m (0, 1,2, 4, 5,7,8, 9,14,15) ii) Simplify the following Boolean expressions using K maps. F (w, x, y, z) = ∑ m (0,1,4,5,8,9,14,15) + dc(11,12)	10	L2	CO1
2	Represent the following numbers, as indicated below. i) 40 and -32 in 8 bit signed magnitude representation ii) 9 and 18 in BCD representation iii) 0 and 4 in Excess 3 representation iv) -237.5 in 32 bit (single precision) floating point number representation v) +342.64 in 32 bit (single precision floating point representation)	10	L2	CO1
3	i) Using booths algorithm, multiply the numbers: +14 x -7 ii) Using Restoring Division Algorithm, divide: +13 / +7	10	L3	CO1
4	Design 1bit Parallel Adder (write Truth Table, KMap Simplification and final expressions) and using 1bit Parallel Adders design a 4bit parallel(ripple) adder/subtractor circuit, with suitable control input to select addition/subtraction. Describe the working of the circuit. Using the above design, Write the answer for the following cases of addition /subtraction. a. X=1001 Y=1101 ADD/SUB = 0 b. X=0011, Y=1010 ADD/SUB = 1 Justify with suitable example, the above circuit works for signed 4 bit numbers, clearly indicating the meaning of Overflow.	10	L3	CO2

5	Discuss the merits of CLA adder over normal ripple adders. Derive the Carry equations, C1 to C4 for 4-bit CLA adder. Draw the circuit diagram, clearly indicating the circuits and all the connections. Suggest time calculations, for designing 16 bit adder using Ripple adder, CLA adder, cascading CLA adders and any other methods	10	L4	CO2

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Course Outcomes: After completing the course, the students will be able to:-	
CO 1	Apply design requirements for digital systems and Computer organization
CO 2	Analyze the models used for designing various Ccombinational and Sequential circuits
CO 3	Develop applications of synchronous sequential networks using flip flops, registers and counters
CO 4	Design optimized modern processors and memories for given specifications
CO 5	Investigate techniques of digital system design for building industry relevant real-world systems using electronic components and modern tools

Course Outcomes:

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	CO5	L1	L2	L3	L4	L5	L6
	Test	Max Marks	30	20	**	**	**	**	20	20	10	**	**

ADLD - I

	R V College of Engineering Department of Computer Science and Engineering CIE - II : (Test2) Question Paper		
Course: (Code)	APPLIED DIGITAL LOGIC DESIGN AND COMPUTER ORGANIZATION (CS234AI)	Semester :	3rd BE
Date : 22nd Feb 2024	Duration : 90 minutes	Staff :	KB/PSB/MH/DD
Name :	USN :	Section :	A/B/C/D/CD/CY

Sl. no	Answer all the questions	Marks	L1-L6	CO
1	a. Implement $f(A, B, C) = \sum m(0, 1, 4, 5, 6, 7)$ using (i) 8:1 MUX with a, b, c as select lines. (ii) 4:1 MUX with a, b as select lines. b. Design a digital circuit for full adder using Dual 4:1 Multiplexer IC (Ex.74153)with necessary gates. c. Construct 5-to-32-line decoder from two 4 to 16-line decoder.	4+4+2	L3	CO2
2	a. Design 3-bit Asynchronous Up Counter, using positive edge triggered T flip-flops. b. Design JK flip flop using a D flip-flop, a 2 to 1 mux and an inverter if required and show all the steps.	4+6	L4	CO2
3	a. Design a Master Slave JK Latch/Flip Flop using only Nand gates. Show the timing diagram and function table. b. Explain with proper timing diagrams 0's and 1's catching	6+4	L3	CO3
4	Design a 4-bit Universal Shift Register, Which supports following modes of operation-	6+4	L3	CO3

S1	S0	Operations
0	0	Hold
0	1	Shift Right Data
1	0	Circular Shift Left Data
1	1	Parallel Load the Data

	Justify how the shift registers can be used as counters (Ring and Johnson). (4 M)			
5	Design Synchronous Counter using JK Positive Edge Triggered Flip Flops, which produces the following sequence: 111,110,101,011,001, 000. Verify the above design as a self-correcting counter or not.	8+ 2	L4	CO3

Course Outcomes: After completing the course, the students will be able to:-	
CO 1	Apply design requirements for digital systems and Computer organization
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Course Outcomes:

	Particulars		CO1	CO2	CO 3	CO4	CO5	L1	L2	L3	L 4	L 5	L6
Marks Distribution	Test	Max Marks	**	20	30	**	**	**	**	30	20	**	**

ADLD -II

	R V College of Engineering Department of Computer Science and Engineering CIE - I : (ReTest) Question Paper		
Course: (Code)	APPLIED DIGITAL LOGIC DESIGN AND COMPUTER ORGANIZATION (CS234AI)		Semester : 3rd BE
Date : 27th March 2024	Duration : 90 minutes	Staff :	KB/PSB/MH/DD
Name :	USN :	Section :	A/B/C/D/CD/CY

Sl. no	Answer all the questions	Marks	L1-L6	CO
1	Design a digital circuit for full adder and full subtractor using 4:1 Multiplexers. Draw the truth table and demonstrate the circuit with all the connections.	10	L3	CO2
2	i) Using booths algorithm, multiply the numbers: +8 x -5 ii) Using Restoring Division Algorithm, divide: +11 / +3	10	L2	CO1
3	Design 4 bit Parallel and 4bit CLA adders. Draw the circuits for both type of adders.	10	L3	CO2
4	-Simplify the Boolean function into Sum of products (SOP) and Products of sum (POS) form. f (A, B, C, D) = ∑ m (0, 1, 2, 5, 8, 9, 10) -Simplify the following Boolean expressions using K maps. F (w, x, y, z) = ∑ m (0,1,4,5,8,9,14,15) + dc(11,12)	10	L3	CO1
5	Design a single bit comparator, by writing the truth table and realize the circuits. Indicate the circuits for designing n bit comparator using cascading one bit comparator	10	L4	CO2

Course Outcomes: After completing the course, the students will be able to:-	
CO 1	Apply design requirements for digital systems and Computer organization
CO 2	Analyze the models used for designing various Ccombinational and Sequential circuits
CO 3	Develop applications of synchronous sequential networks using flip flops, registers and counters
CO 4	Design optimized modern processors and memories for given specifications
CO 5	Investigate techniques of digital system design for building industry relevant real-world systems using electronic components and modern tools

Course Outcomes:

Particulars		CO1	CO2	CO3	CO4	CO5	L1	L2	L3	L4	L5	L6
Marks Distribution	Test	Max Marks	30	20	**	**	**	**	10	30	10	**	**

RV COLLEGE OF ENGINEERING®

(An Autonomous Institution Affiliated to VTU)

III Semester B. E. Examinations Apr/May-2024

Computer Science Engineering

Common to CD / CY / CS

APPLIED DIGITAL LOGIC DESIGN AND COMPUTER ORGANIZATION

Time: 03 Hours *Maximum Marks: 100*

Instructions to candidates:

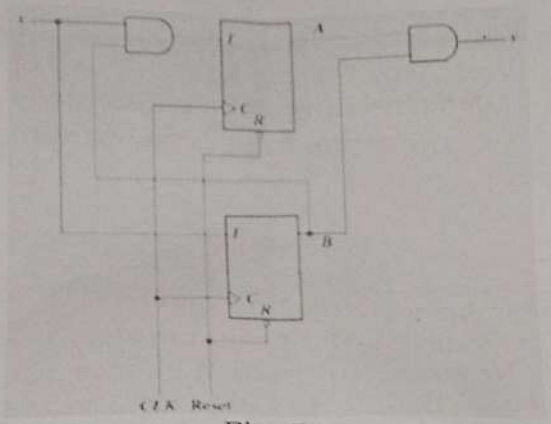
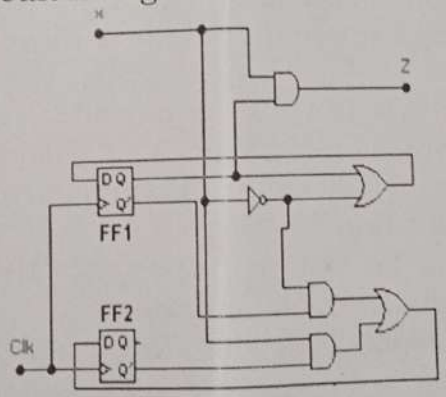
1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2 is compulsory. Answer any one full question from 3 and 4, 5 and 6, 7 and 8, 9 and 10.

PART-A

			M	BT	CO
1	1.1	What are state diagrams and state tables?	02	2	1
	1.2	Draw the logical diagram of a 1*bit* magnitude comparator.	01	3	2
	1.3	Assume that a $4-bit$ serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the $4-bit$ pattern after the second clock pulse? (Right-most bit first).	01	2	1
	1.4	Draw the timing diagram of a 2 *bit* down counter with negative edge triggered flip flops.	02	2	2
	1.5	Simplify the Boolean expression: $Y = \overline{(A + \bar{B} + C) + (B + \bar{C})}$.	01	3	3
	1.6	Given $F = \Sigma m(1,5,6,7,11,12,13,15)$, find the number of implicants, prime implicants and essential prime implicants.	02	2	4
	1.7	List and discuss various conditional codes.	02	2	4
	1.8	How many *JK* flipflops are required to achieve the frequency division of 8?	01	3	4
	1.9	Determine the number of min-terms after minimizing the following Boolean expression $[D' + AB' + A'C + AC'D + A'C'D]'$.	01	3	1
	1.10	Represent -48.625 in hexadecimal notation, in single precision after applying normalization.	01	3	1
	1.11	Consider the following bit pattern represents the floating point number in *IEEE* 754 single precision format: 1 10000111 11100000000000000000000. Represent this number in decimal format.	02	2	1
	1.12	Summarize the algorithm for non-restoring division.	02	2	1
	1.13	Realize the function $f(a,b,c,d) = \Sigma m(1,4,5,7,9,12,13)$ using a 4 to 1 *mux*.	02	3	2

PART-B

2	a	Multiply each of the following pairs of signed 2's complement numbers using Bit Pair recoding. Assume that A is multiplicand and B is multiplier. i) $A = 010111$ and $B = 110110$ ii) $A = 001111$ and $B = 001111$	08	2	2
	b	Simplify the following Boolean function, $f(w,x,y,z) = \Sigma(0,2,5,7,10,13,14,15)$ using Quine-McClukey tabular method.	08	3	2

3	a	With a neat diagram explain a decimal adder in detail.	08	2	2
	b	Implement the Boolean function using 8:1 and also using 4:1 multiplexer $F(A,B,C,D) = \Sigma m(0,1,2,4,6,9,12,14)$.	08	3	4
		OR			
4	a	Explain Master Slave JK flip-flop with the help of circuit diagram and waveforms.	08	3	3
	b	With the help of logic diagram, explain the 4 *bit* universal shift register using D flip-flops and 4:1 MUX.	08	3	4
5	a	Construct the excitation table, transition table, state table and state diagram for the following sequential circuit shown in Fig. 5.a			
					
		Fig. 5.a	08	3	2
	b	Design a *Mod* 4 synchronous up-counter using JK flipflop.	08	3	2
		OR			
6	a	Derive the next state, the output table and the state diagram for the sequential circuit in Fig. 6.a			
					
		Fig. 6.a	08	2	2
	b	Design a synchronous counter to count the following sequence 7, 4, 3, 1, 5, 0, 7, 4, 3, ... implement the circuit using T –flipflops.	08	3	3
7	a	With a neat diagram of connections between the processor and memory, list and explain the basic steps needed to execute the machine instruction Move $LOCA, R0$ in terms of transfers between the components of processor, memory and some control commands.	06	2	3
	b	Define subroutine linkage. With an example explain different mechanism of passing parameters to subroutines.	10	3	4
		OR			

8	a	Describe with an example, usage of stack frame in nested subroutine. In the example demonstrate how the main program calls subroutine1 further subroutine1 calls subroutine2.	10	3	4
	b	Write an *ALP* that finds the number of negative integers in a list of n $32-bit$ integers and stores the count in location *NEGNUM*. The value n is stored in memory location N, and the first integer in the list is stored in location *NUMBERS*. Include the necessary assembler directives and a sample list that contains six numbers, some of which are negative.	06	3	4
9	a	With a neat diagram of three bus organization of the data path, demonstrate the control sequence for the instruction Add $R4, R5, R6$.	08	2	3
	b	Design $2M \times 32$ memory module using $512k \times 8$ memory chip and explain various external connections.	08	3	4
		OR			
10	a	Discuss direct mapped, associative mapped and set associative mapped cache memory system with suitable diagrams.	12	2	3
	b	Consider main memory size of $4GB$, cache size of $16MB$ and block size of $1KB$ determine the tag size for an 8 way associative cache.	04	2	3