**16CS34**

**USN** | | | | | | | | | | |

# R. V. COLLEGE OF ENGINEERING

**Autonomous Institution affiliated toVTU**

**III Semester B. E. Examinations Nov/Dec-18**

## Computer Science and Engineering

## LOGIC DESIGN

***Time: 03 Hours*** ***Maximum Marks: 100***

***Instructions to candidates:***

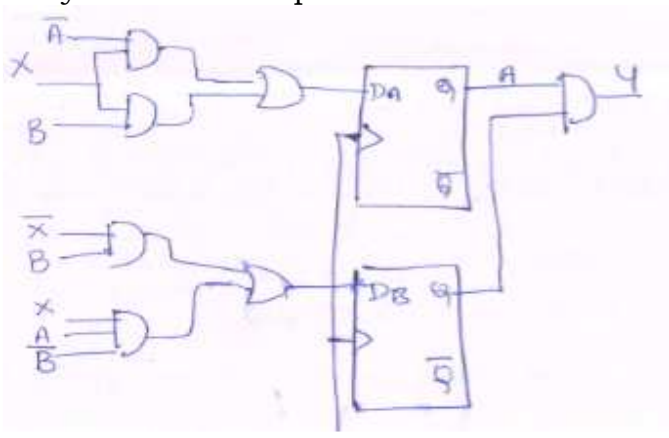
1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B.In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

### PART-A

| | | | |
|---|---|---|---|
| 1 | 1.1 | Give the simplest logic circuit for the following logic equation: $F(A,B,C,D) = \sum m(7) + d(10,11,12,13,14,15)$ | 02 |
| | 1.2 | Justify positive $OR \leftrightarrow$ negative $AND$. | 02 |
| | 1.3 | Design a comparator to check if two $n$-bit numbers are equal. Configure these using cascaded stages of 1-bit comparators. | 02 |
| | 1.4 | Write the truth table for 2 to 4 line decoder. | 01 |
| | 1.5 | Implement the following function using a 4 to 1 $MUX$: $f(a,b,c) = \sum m(0,1,2,7)$. | 02 |
| | 1.6 | Differentiate between $PROM$ (Programmable $ROM$) and $PLA$(Programmable Logic Array). | 01 |
| | 1.7 | What is 0's catching problem in Master-Slave $JK\ FF$? Give solution for the same. | 02 |
| | 1.8 | Write the characteristic equation for '$T$' flip flop. | 01 |
| | 1.9 | Configure a synchronous 4-bit up-counter with parallel load inputs to count from 0000 to 1001. | 02 |
| | 1.10 | Draw the state diagram for a Mealy serial binary adder. | 02 |
| | 1.11 | Write the 4 to 2 line priority encoder table by assigning highest priority to the least significant input. | 02 |
| | 1.12 | Define "Minimum pulse width" | 01 |

### PART-B

| | | | |
|---|---|---|---|
| 2 | a | Design a minimal sum and a minimal product combinational gate circuit to generate the odd parity bit for a 8421 $BCD$ code. | 08 |
| | b | Obtain all the prime implicants of the given Boolean function using Quine-Mccluskey method: $f(a,b,c) = \sum m(0,1,2,3,4,5,6)$ | 08 |
| | | | |
| 3 | a | With a neat diagram explain decimal adder. | 08 |
| | b | Implement the following function using<br>i) 8 to 1 $MUX(a,b,c$ as select lines)<br>ii) 4 to 1 $MUX(a,b$ as select lines) for the function $f(a,b,c) = \sum m(0,1,5,6,7,9,10,15)$ | 08 |

| | | | |
|---|---|---|---|
| | | **OR** | |
| 4 | a | Construct a 3 to 8 line decoder using two 2 to 4 line decoder. | 06 |
| | b | Implement the following Boolean function using a $PLA$ with both true and complemented outputs. Map 1's and 0's to arrive at a design with minimal number of product terms in $PLA$. Write $PLA$ table. ($PLA$-Programmable Logic Array)<br>$f_1(a,b,c) = \sum m(0,1,2,5,7)$<br>$f_2(a,b,c) = \sum m(3,4,5)$<br>$f_3(a,b,c) = \sum m(3,4,5,6)$ | 10 |
| | | | |
| 5 | a | Illustrate how Master-Slave $JK$ flip flop overcomes the problem of race around condition in $JK$ flip flop. | 08 |
| | b | With a neat diagram explain the working of universal shift register. | 08 |
| | | **OR** | |
| 6 | a | With the help of function table and symbols, explain positive edge triggered '$D$' flip flop. | 08 |
| | b | With a neat diagram explain parallel-in unidirectional shift register. | 08 |
| | | | |
| 7 | a | Design a self-correcting mod-6 counter using clocked $SR$ flip flop(redirect invalid entries to 000). | 10 |
| | b | Describe how registers are applications of mod-7 twisted-ring counter. | 06 |
| | | | |
| 8 | a | Construct the excitation table, transition table, state table and state diagram for the synchronous sequential circuit shown in figure 8a.<br>  <br>figure 8a | 12 |
| | b | Differentiate between Mealy model and Moore model synchronous sequential networks. | 04 |