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RV COLLEGE OF ENGINEERING®
(An Autonomous Institution affiliated to VTU)
III Semester B. E. Fast Track Examinations Jan/Feb -2023
Computer Science Engineering

COMPUTER ORGANIZATION

Time: 03 Hours **Maximum Marks: 100**

Instructions to candidates:
1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6.

PART A

1	1.1	Define computer organization.	01
	1.2	Give the basic performance equation.	01
	1.3	Name any two key objective of USB.	02
	1.4	What is Big-Endian and Little-Endian representation?	02
	1.5	Define page fault.	01
	1.6	The Universal Serial Bus (USB) operates on the basis of _____.	01
	1.7	Construct the Booth recoding of a multiplier for the following sequence: 0101101100101001	02
	1.8	Write the algorithm for restoring-division method.	02
	1.9	Name any two data transfer signals on PCI Bus along with their functionalities.	02
	1.10	Register R_1 and R_2 of a computer contain the decimal values 2500 and 1800. Find the effective address of the memory operand in each of the following instructions: a. STORE $R_3, 50(R_1, R_2)$ b. ADD-$(R_1), R_5$	02
	1.11	What is Bit pair recoding? Give one example.	02
	1.12	In many computers the cache block size is in the range of 32 to 128 bytes. Indicate the advantage and disadvantage of making the size of cache block smaller or larger.	02

PART B

2	a	List and explain the basic steps needed to execute the machine instruction ADD LOCA,R_0 in terms of transfer function between the components of processor, memory and some control commands with the help of the neat diagram.	08
	b	Define addressing mode. Demonstrate the addressing function for any three addressing modes with example for each.	08
3	a	Define Sub-routing linkage. With an example explain different mechanism of passing parameters to subrouting.	08
	b	Describe the ARM register structure and also write the ARM instruction format.	08

		OR	
4	a	Discuss the addressing mode of ARM architecture with an example for each.	10
	b	Write sequence of instructions for safe pop and push operations.	06
5	a	With the help of a neat diagram discuss how a read operation is performed in PCI bus.	10
	b	In a situation where a number of devices are capable of initiating interrupts are connected to processor. Illustrate i. How can the processor recognize the device requesting an interrupt? ii. How should two or more simultaneous request be handled.	06
		OR	
6	a	Mention the main features of SCSI bus.	08
	b	Explain the hardware register that are required in a DMA controller chip. Why it is necessary for a DMA controller to be able to interrupt the processor? Explain.	08
7	a	Discuss how an address generated by the processor gets translated into a main memory address.	08
	b	Design a $8M \times 32$ memory system using $512k \times 8$ memory chips and explain the memory architecture.	08
8	a	With the help of a single bus architecture, explain how to transfer a word of data from one processor register to ALU.	08
	b	Divide 15/3 using both non-restoring and restoring division Technique.	08