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R. V. COLLEGE OF ENGINEERING

Autonomous Institution affiliated to VTU

III Semester B. E. Examinations Nov/Dec-18

Computer Science and Engineering

COMPUTER ORGANIZATION

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

PART-A

1	1.1	Define computer organization.	01
	1.2	Give the basic performance equation.	01
	1.3	Give a short sequence of machine instructions for the task "Add the contents of memory location A to those of location B and place the answer in location C. Instructions $LOAD\ LOC$, R_i and $STORE\ R_i, LOC$ are the only instructions available to transfer data between memory and general purpose registers. Do not destroy the contents of either location A or B.	02
	1.4	Register R_1 and R_2 of a computer contain the decimal values 2500 and 1800. Find the effective address of the memory operand in each of the following instruction: a) $STORE\ R_3\ 50(R_1, R_2)$ b) $ADD\ -(R_1), R_5$	02
	1.5	Name any two data transfer signals on PCI bus along with their functionalities.	02
	1.6	Two processes A and B have clock frequencies of $700MHz$ and $900MHz$ respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of same instruction which processor is faster?	02
	1.7	When a subroutine is called, the address of the instruction following the $CALL$ instruction is stored in _____.	01
	1.8	What is Big-Endian and little Endian representation?	01
	1.9	What is Bit-Pair recording? Give an example.	01
	1.10	Write the algorithm for restoring division method.	02
	1.11	Define datapath in a processor unit.	01
	1.12	Define cache hit and cache miss.	01
	1.13	Why I/O devices cannot be directly connected to the system bus?	01
	1.14	Differentiate between synchronous and asynchronous bus.	01
	1.15	Name any two key objective of USB.	01

PART-B

2	a	List and explain the basic steps needed to execute the machine instruction $ADD\ LOCA, R_0$ in terms of transfer between the components of processor, memory and some control commands with the help of neat diagram.	08

	b	With examples explain the following assembler directive: i) EQU ii) $ORIGIN$ iii) $DATAWORD$ iv) $RESERVE$.	04
	C	Briefly describe the factors that influence the performance of processor.	04
3	a	Register R_5 is used in a program to point to the top of a stack containing 32-bit numbers. Write a sequence of instructions using the Index, auto-increment, auto-decimal addressing modes to perform each of the following tasks: i) Pop the top two items off the stack, add them and then push the result to the stack ii) Copy the fifth item from the top into register R_3 iii) Remove the top 10 items from the stack. For each case assume that the stack contains more than 10 items.	08
	b	Define sub-routine linkage. With an example explain different mechanism of passing parameters to sub-routine.	08
		OR	
4	a	Discuss the addressing mode of ARM architecture with an example for each.	10
	b	Describe the ARM register structure and also write the ARM instruction format.	06
5	a	In a situation where a number of devices are capable of initiating interrupts are connected to processor. Illustrate i) How can the processor recognize the device requesting an interrupt? ii) How should two or more simultaneous request be handled?	08
	b	Define the bus arbitration. Explain the different ways of bus arbitration with suitable diagram.	08
		OR	
6	a	What is DMA? Explain the registers in a DMA interface.	04
	b	Differentiate between synchronous and asynchronous bus with proper timing diagram.	04
	c	Mention the main features of $SCSI$ Bus.	08
7	a	Our system has a main memory with $16MB$ of addressable locations and a $32kB$ direct cache with 8 bytes per block. The minimum addressable unit is a byte i) How many blocks are there in the cache? ii) Show how the main memory address is partitioned.	06
	b	Design a $8M \times 32$ memory system using $512k \times 8$ memory chips and explain the memory architecture.	06
	c	Explain the advantages of set-associative mapping over direct mapping with an example.	04
8	a	With the help of single bus architecture explain how to transfer a word of data from one processor register to another to ALU.	08
	b	Multiply the following numbers using Booth's bit pair recording algorithm i) 13 and -6 ii) 21 and 5	04
	c	Divide 12 by 4 using non-restoring division algorithm.	04