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RV COLLEGE OF ENGINEERING®

(An Autonomous Institution affiliated to VTU)

V Semester B. E. Examinations Nov/Dec-19

Electronics and Communication Engineering

EMBEDDED SYSTEM DESIGN

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

PART-A

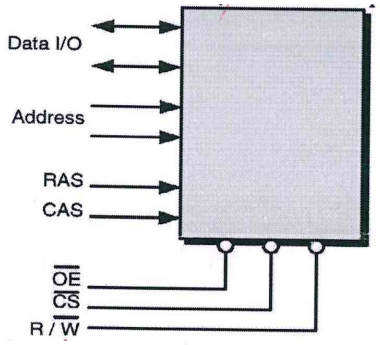
1	1.1	A _____ is a piece of hardware that can be used to automatically detect software anomalies and reset the processor if any occur.	01
	1.2	The most important feature to have in a microcontroller/microprocessor in designing a extremely low power, embedded system is _____.	01
	1.3	What is the major difference between hard real time and soft real time system?	01
	1.4	Give an example for hardware accelerators.	01
	1.5	What is invalidation technique in cache?	01
	1.6	Write a diagram of active low power on Reset circuit.	01

	1.7	Write the *MISRA C* 2012 standard compliant equivalent of the following code:
		$int\ x = 1;$
		$while\ (x == 0)$
		{
		$/*\ x\ is\ not\ modified\ within\ the\ loop\ and\ is\ modified\ by\ other\ execution\ units\ */$
		}
			01

	1.8	Priority ceiling and Priority inheritance are the two mechanisms for avoiding Priority_____ in a multitasking environment.	01
	1.9	Mention the four quality concepts of any coding standard.	02
	1.10	Consider a pipeline having 4 phases with duration 60,50,90 and 80ns. Given latch delay is 10ns. Calculate Pipeline cycle time.	02
	1.11	Give any two differences between a thread and process.	02
	1.12	List any two techniques to map cache memory to the main memory.	02
	1.13	What are arguments to be passed while creating a task using pthread_create *POSIX API*?	02
	1.14	Differentiate between User space and Kernel space.	02

PART-B

2	a	Write a block diagram of chocolate vending machine to vend chocolates from four companies of 4 different price. Clearly specify the software and hardware units in the system.	10
	b	Discuss the design challenges faced in an Embedded system.	06

3	a	Explain the various refreshing techniques used for $DRAM$ with relevant timing diagram.	10
	b	Give the address space table and the address decoding scheme (Digital circuits for Chip select) for interfacing two $ROMs$ of $2k$ and $8k$ capacity, one RAM of $2K$ and two peripheral devices to a processor with 24 bit address lines.	06
		OR	
4	a	For the memory sketch shown in Fig 4a and explain the read and write cycles.  Fig 4a	08
	b	Explain coherence problem in cache? How to mitigate the coherence problem? Give two algorithms.	08
5	a	Design an interface where processor reads a peripheral chip as per $I2C$ standard and put the read data to ports continuously. Show the interface diagram, timing diagram and write the relevant pseudo code.	10
	b	Explain the different types of errors in CAN?	06
		OR	
6	a	Explain arbitration in CAN protocol.	06
	b	Sketch the interface diagram, timing diagram and write the pseudo code for communication between one master and two slaves as per SPI communication protocol.	10
7	a	What are the coding practices and rules followed to ensure reliability, maintainability, portability and efficiency as per $MISRA\ C$ 2012 guidelines?	08
	b	Compare: i) Compilers and cross compilers. ii) Assembly language and high level language for embedded system software development.	08
8	a	Mention the services offered by $RTX - ARM$ kernel? Explain.	08
	b	Write a program to create thread and communicate/pass messages from parent to child thread using message queues $POSIX$ standard functions.	08