USN | | | | | | | | | | |

# RV COLLEGE OF ENGINEERING®

**(An Autonomous Institution affiliated to VTU)**

**V Semester B. E. Examinations Nov/Dec-19**

## Electronics and Communication Engineering

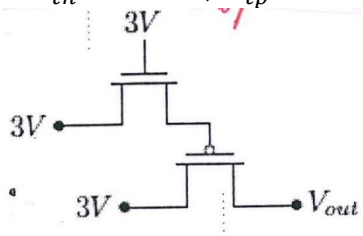
# DIGITAL VLSI DESIGN

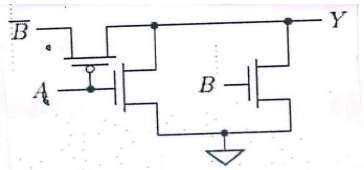
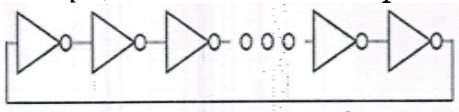
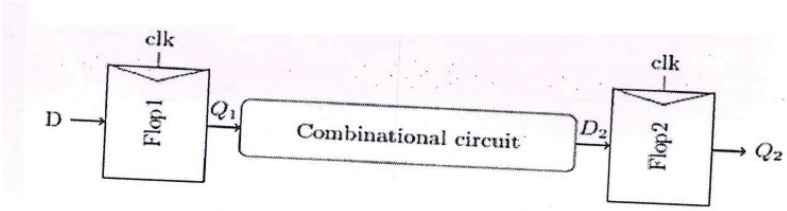
***Time: 03 Hours*** ***Maximum Marks: 100***

***Instructions to candidates:***

1. Answer all questions from Part A. Part A questions should be answered in first three pages of the answer book only.
2. Answer FIVE full questions from Part B. In Part B question number 2, 7 and 8 are compulsory. Answer any one full question from 3 and 4 & one full question from 5 and 6

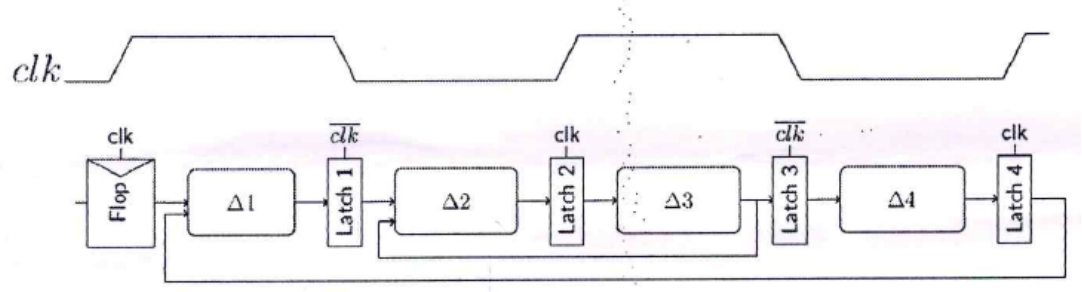
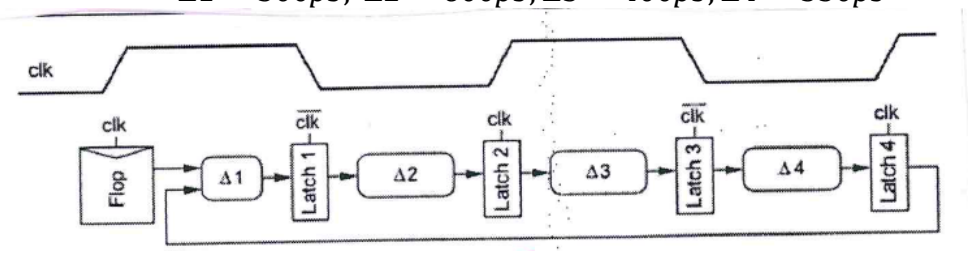
## PART-A

| | | | |
|---|---|---|---|
| 1 | 1.1 | The input condition of a $CMOS$ inverter for $PMOS$ to work in saturation and $NMOS$ to work in linear region is _____. | 01 |
| | 1.2 | In a Hi-skewed inverter, the value of $\frac{\beta_n}{\beta_p}$ is _____. | 01 |
| | 1.3 | Due to high vertical field strength, carriers are attracted more towards the channel edge and cause collision with the oxide interface that results in _____, is a type of second order effect. | 01 |
| | 1.4 | For a unit size $CMOS$ inverter, the switching threshold voltage is _____. | 01 |
| | 1.5 | The $NMOSFET$ is driving the gate of $PMOS\ FET$ as shown in Fig 1.5, Calculate the $V_{out}$ . Given $V_{tn} = +0.5V$, $V_{tp} = -0.5V$.   Fig 1.5 | 01 |
| | 1.6 | Name the photoresist which is initially soluble and becomes insoluble when exposed to $UV$ light. | 01 |
| | 1.7 | What is the name of process involved in growing a single crystal film on the silicon surface by subjecting to an elevated temperature and a source of dopant material? | 01 |
| | 1.8 | Silicon dioxide is used in the $IC$ fabrication process for _____ and _____. | 01 |
| | 1.9 | The process used to cut the wafers from ingots of a single crystal silicon that have been pulled from a crucible melt of pure molten silicon. | 01 |

| | | | |
|---|---|---|---|
| | 1.10 | Identify the logic function for the circuit shown in fig 1.10<br>  <br><br>Fig 1.10 | 01 |
| | 1.11 | A ring oscillator is constructed from an odd number of inverters, as shown in fig 1.11. Estimate the frequency of an $N$-stage ring oscillator. If there are 29 stages and the inverter is constructed in a 65nm process with $\tau = 3ps$, calculate the frequency of oscillation.<br>  <br>Fig 1.11 | 02 |
| | 1.12 | In stick diagram of $CMOS$ process $n$ and $P$ transistors are separated by using _____. | 01 |
| | 1.13 | For the circuit shown in Fig 1.13, the maximum allowable logic delay= _____ ps and the minimum logic contamination delay = _____ ps. Assume that flip-flops have a set up time of $36ps$, hold time of $40ps$, propagation delay of $90ps$, and contamination delay of $25ps$ and are operated at a clock frequency of $1GHz$ with zero clock skew.<br>  <br><br>Fig 1.13 | 02 |
| | 1.14 | In $DRAM$, the information is degraded over time due to _____. | 01 |
| | 1.15 | To ensure both read and write stability in $SRAM$; The $NMOS$ pull down transistor must be sized _____ as compared to access transistors and a $PMOS$ transistor must be sized _____. | 02 |
| | 1.16 | Realize all 0's detector circuit of 4-bit word using pseudo-$NMOS$ logic. Size them by assuming that the $NMOS$ is $4\times$ times stronger than $pMOS$. | 02 |

**PART-B**

| | | | |
|---|---|---|---|
| 2 | a | Explain $VLSI$ design flow with necessary flow diagram. | 08 |
| | b | Draw the $CMOS$ inverter transfer characteristics and explain its operation by indicating regions of operation of each transistor. | 08 |
| | | | |
| 3 | a | Implement the function $Y = \overline{(A.(B+C)+D.E}$ using static $CMOS$ logic and size the transistors appropriately to get equal propagation delay as that of a minimum sized inverter with $\left(\frac{\omega}{L}\right)_p = 3$ and $\left(\frac{\omega}{L}\right)_n = 1$. Estimate the logical effort and parasitic delays. | 06 |
| | b | Sketch a 4 input $CVSL\ XOR/XNOR$ gate. | 04 |
| | c | Realize Wallace tree multiplier with a block diagram. Show the worst path delay incurred in it. | 06 |
| | | **OR** | |

| | | | |
|---|---|---|---|
| 4 | a | What is monotonicity problem in dynamic $CMOS$ logic? Explain how domino logic overcomes this problem? | 10 |
| | b | Construct a full adder using transmission gate logic. Comment about the transistors count with respect to static $CMOS$ version. | 06 |
| | | | |
| 5 | a | Show the $CMOS$ implementation of a $NOR$ based $SR$ Latch. Explain its operation with truth table and evaluate the load capacitance at the output node. Give its rise time expression. | 07 |
| | b | Calculate the minimum allowable logic delay for all the 3 static sequencing method with a neat graph. | 09 |
| | | **OR** | |
| 6 | a | Realize $CMOS$ clocked $JK$ latch based on $AOI$ implementation. | 04 |
| | b | Determine the minimum clock period at which the circuit in Fig 6b will operate correctly for each of the following logic delays. Assume there is zero clock skew and that the latch delays are accounted for in the propagation delay. Use data from table 6b<br>i) $= 300ps;$ $= 400ps;$ $= 200ps;$ $= 350ps$<br>ii) $= 300ps;$ $= 400ps;$ $= 400ps;$ $= 550ps$<br>iii) $= 300ps;$ $= 900ps;$ $= 200ps;$ $= 350ps$ | |
| | |  | |
| | | Fig 6b | |
| | | Table 6b : Timing parameters for sequential circuits | |
| | | | 08 |
| | c | For the path shown in Fig 6( c), calculate the borrow time required through different latches and check any set up time violation occurs. Assume that there is zero clock skew and that the latch delays are accounted for in the propagation delay. Given tsu_flop= $65ps$, tsu_latch= $30ps$ and clock period, $Tc = 1000ps$<br>$\Delta 1 = 300ps;\ \Delta 2 = 600ps; \Delta 3 = 400ps; \Delta 4 = 550ps$ | |
| | |  | |
| | | Fig 6(c) | 04 |
| | | | |

| | *set up time* | *clk-to-Q delay* | *D-Q delay* | *contamination delay* | *hold time* |
|---|---|---|---|---|---|
| *Flip flops* | $65ps$ | $50ps$ | $n/a$ | $35ps$ | $30ps$ |
| *Latches* | $25ps$ | $50ps$ | $40ps$ | $35ps$ | $30ps$ |

| | | | |
|---|---|---|---|
| 7 | a | Using $6T\ SRAM$ cell and appropriate waveforms, explain the read/write operation of it. Also discuss how the cell stability conditions are used in the design. | 10 |
| | b | Realize a 4-word by 6-bit $ROM$ using Pseudo $-nMOS$ pull –ups with the following contents.<br>$word0: 010101$<br>$word1: 011001$<br>$word2: 100101$<br>$word3: 101010$ | 06 |
| | | | |
| 8 | a | With a neat sketch, explain shallow trench isolation. | 06 |
| | b | What are layout design rules and explain the basic rules used in $\lambda$ –based design rules? Design a minimum sized inverter layout based on the rules mentioned above. Also calculate the area for the inverter layout. | 10 |