CS43(00)

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RAMAIAH Institute of Technology

(Autonomous Institute, Affiliated to VTU)
(Approved by AICTE, New Delhi & Govt. of Karnataka)
Accredited by NBA & NAAC with 'A+' Grade

SEMESTER END EXAMINATIONS – AUGUST 2024

Program	:	**B.E :- Computer Science and Engineering**	**Semester**	:	**IV**
Course Name	:	**Microprocessor and Microcontrollers**	**Max. Marks**	:	**100**
Course Code	:	**CS43(00)**	**Duration**	:	**3 Hrs**

Instructions to the Candidates:

- Answer one full question from each unit.

UNIT - I

1.	a)	Discuss the two Pipeline Hazards while using a RISC Processor.	CO1	(08)
	b)	Explain the various control signals for Data operations in MU0 Microprocessor with a diagram showing various registers.	CO1	(06)
	c)	Discuss the two Pipeline Hazards while using a RISC Processor.	CO1	(06)
2.	a)	Explain the various control signals for Data operations in MU0 Microprocessor with a diagram showing various registers.	CO1	(08)
	b)	Discuss the salient system features of CortexM0 processors.	CO1	(06)
	c)	i)Discuss Instructions used for branching with NZCV status flags and suffixes used. ii)What is result and NZCV status flag values when the following arithmetic operations are done on APSR register. Justify your answer i) 0x50000000 +0x50000000 ii) 0x00044321 - 0x00034000 iii) 0x20000000 +0x30000000 iv) 0x90000000 + 0x90000000.	CO1	(06)

UNIT - II

3.	a)	Elaborate on various embedded system programing design techniques used while writing embedded programs.	CO2	(06)
	b)	Discuss the utility of Program counter, link register and stack pointer with example.	CO2	(08)
	c)	Explain the various features supported by the NVIC in Cortex M0.	CO2	(06)
4.	a)	Explain the programing model of Cortex M0 in terms modes and states with a neat diagram.	CO2	(06)
	b)	Discuss the special purpose registers and their utility and instructions used to examine them.	CO2	(08)
	c)	Explain the Startup sequence of a Cortex M0 processor with a net diagram.	CO2	(06)

UNIT - III

5.	a)	Write a program to extract bits 16 to 11 using logical shift instruction? And also Write an assembly language program to realize the switch statement to allow a program to branch to multiple possible address locations based on the input.	CO3	(10)
	b)	Discuss the utility of memory barrier instructions and sleep mode instructions. Also demonstrate the to transfer 256 bytes of data transfer from one memory location to another using LDMIA and STMIA instructions	CO3	(10)

6.	a)	Write a program to discuss nested loop and stack utility for nested functions.	CO3	(08)

	b)	Find the output of following code
		i) LDR r2,=0x08000080;
		LSRS r0,r2,#05;
		ii) LDR r2,=0x80000080;
		ASRS r0,r2,#05;
		iii) LDR r2,=0x80000080;
		RORS r0,r2,#05;
			CO3	(06)

	c)	Write an assembly level program to implement a function 2x+9 using stack.	CO3	(06)

UNIT- IV

7.	a)	Explain the stacking and unstacking process when interrupt is handled? Explain the importance EX _ RETURN value and where it is stored?	CO4	(08)
	b)	Write a timing diagram for: i) LR set to EXC_RETURN values at exceptions (main stack is used in Thread mode). ii) LR set to EXC_RETURN values at exceptions (process stack is used in Thread mode).	CO4	(08)
	c)	Contrast the functioning of sensors and actuators.	CO4	(04)
8.	a)	Discuss the attributes of various parts of the memory map of CORTEX M0 and its utility.	CO4	(08)
	b)	Write a note on following Exception sequences: Late Arrival ii) Tail Chaining.	CO4	(08)
	c)	Write an assembly code to enable and disable interrupt#3 use relevant instruction set.	CO4	(04)

UNIT - V

9.	a)	Elaborate on Micropython interpreter its, auto intent and auto completion and soft reset.	CO5	(05)
	b)	Examine the scarcity of runtime resources of Nodemcu.	CO5	(05)
	c)	Explain the RTC socket and buffer overflow and SSL/TLS limitations of Nodemcu 8266.	CO5	(10)
10.	a)	What are the general features of 8266 Nodemcu microcontroller? How it is different from other microcontrollers?	CO5	(10)
	b)	Implement a micropython code for the following: i. Interrupt programming ii. Soft reset iii. Past mode.	CO5	(10)

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