2.2 Combination and arithmetic circuits

1)What is a multiplexer?
a) It is a type of decoder which decodes several inputs and gives one output
b) A multiplexer is a device which converts many signals into one
c) It takes one input and results into many output
d) It is a type of encoder which decodes several inputs and gives one output
Explanation: A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

2)Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to output line?
a) Data Selector
b) Data distributor
c) Both data selector and data distributor
d) DeMultiplexer
Explanation: Data Selector is another name of Multiplexer. A multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line, depending on the active select lines.

3)It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large number of _____
a) Inputs
b) Outputs
c) Selection lines
d) Enable lines
Explanation: It is possible for an enable or strobe input to undergo an expansion of two or more MUX ICs to the digital multiplexer with the proficiency of large number of inputs.

4)Which is the major functioning responsibility of the multiplexing combinational circuit?
a) Decoding the binary information
b) Generation of all minterms in an output function with OR-gate
c) Generation of selected path between multiple sources and a single destination
d) Encoding of binary information

5) What is the function of an enable input on a multiplexer chip?
a) To apply Vcc

b) To connect ground
c) To active the entire chip
d) To active one half of the chip

6)One multiplexer can take the place of _____
a) Several SSI logic gates
b) Combinational logic circuits
c) Several Ex-NOR gates
d) Several SSI logic gates or combinational logic circuits

7)A digital multiplexer is a combinational circuit that selects _____
a) One digital information from several sources and transmits the selected one
b) Many digital information and convert them into one
c) Many decimal inputs and transmits the selected information
d) Many decimal outputs and accepts the selected information

8) In a multiplexer, the selection of a particular input line is controlled by _____
a) Data controller
b) Selected lines
c) Logic gates
d) Both data controller and selected lines

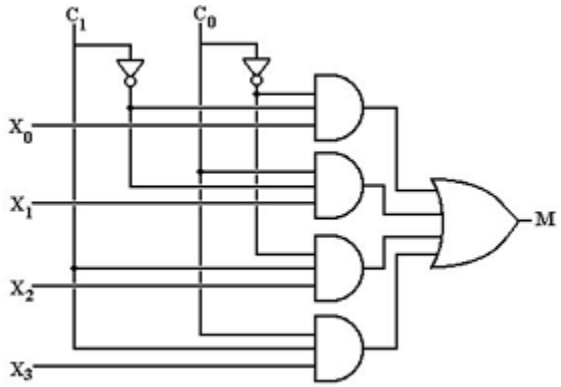
9)If the number of n selected input lines is equal to 2^m then it requires _____ select lines.
a) 2
b) m
c) n
d) 2n

10)How many select lines would be required for an 8-line-to-1-line multiplexer?
a) 2
b) 4
c) 8
d) 3

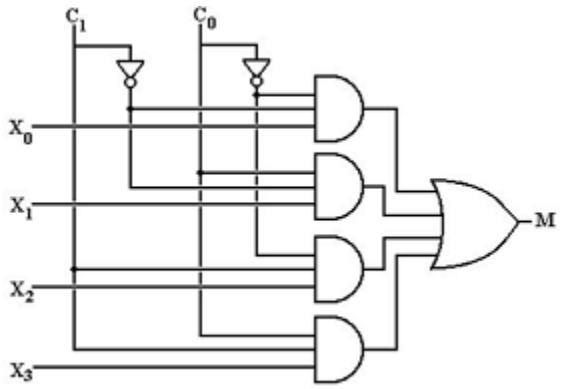
11)A basic multiplexer principle can be demonstrated through the use of a _____
a) Single-pole relay
b) DPDT switch

c) Rotary switch
d) Linear stepper

12) How many NOT gates are required for the construction of a 4-to-1 multiplexer?
a) 3
b) 4
c) 2
d) 5
Explanation: There are two NOT gates required for the construction of 4-to-1 multiplexer. x0, x1, x2 and x3 are the inputs and C1 and C0 are the select lines and M is the output.
The diagram of a 4-to-1 multiplexer is shown below:



13) In the given 4-to-1 multiplexer, if c1 = 0 and c0 = 1 then the output M is _____

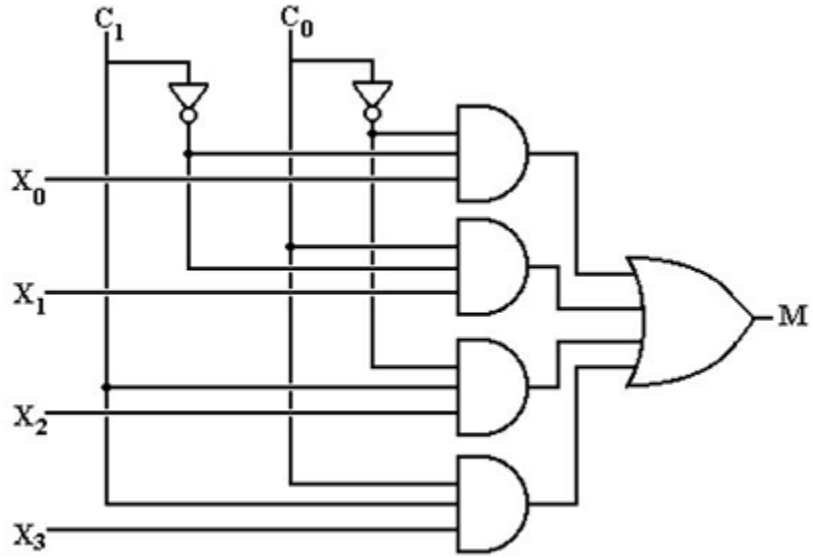


a) X0
b) X1
c) X2
d) X3

Explanation: The output will be X1, because c1 = 0 and c0 = 1 results into 1 which further results as X1. And rest of the AND gates gives output as 0.

14)The enable input is also known as _____
a) Select input
b) Decoded input
c) Strobe
d) SinkAnswer
Explanation: The enable input is also known as strobe which is used to cascade two or more multiplexer ICs to construct a multiplexer with a larger number of inputs. Enable input activates the multiplexer to operate.

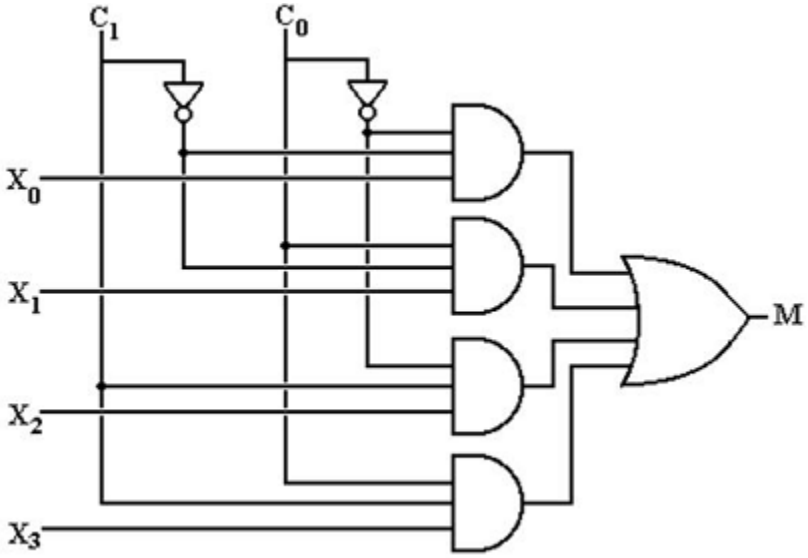
15) 4 to 1 MUX would have _____
a) 2 inputs
b) 3 inputs
c) 4 inputs
d) 5 inputs
Explanation: 4 to 1 multiplexer would have 4 inputs (X0, X1, X2, X3), 2 select lines (C1, C0) and 1 output (M). It can be observed from this diagram:



16)The two input MUX would have _____
a) 1 select line
b) 2 select lines
c) 4 select lines
d) 3 select lines
Explanation: The two input multiplexer would have n select lines in 2n. Thus n =1. Therefore, it has 1 select line.

17)A combinational circuit that selects one from many inputs are _____
a) Encoder
b) Decoder
c) Demultiplexer
d) Multiplexer
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer. Whereas, a combinational circuit that divides one input into multiple outputs is known as Demultiplexer.

18) 4 to 1 MUX would have _____
a) 1 output
b) 2 outputs
c) 3 outputs
d) 4 outputs
Explanation: 4 to 1 multiplexer would have 4 inputs (X0, X1, X2, X3), 2 select lines (C1, C0) and 1 output (M). It can be observed from this diagram:



19) Which of the following circuit can be used as parallel to serial converter?
a) Multiplexer
b) Demultiplexer
c) Decoder
d) Digital counter
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer. In multiplexer, different inputs are inserted parallely and then it gives one output which is in serial form.

19) A combinational circuit is one in which the output depends on the _____

a) Input combination at the time
b) Input combination and the previous output
c) Input combination at that time and the previous input combination
d) Present output and the previous output
Explanation: A combinational circuit is one in which the output depends on the input combination at the time, whereas, a sequential circuit is one in which the output depends on present input as well past outputs.

20)Without any additional circuitry an 8:1 MUX can be used to obtain _____

a) Some but not all Boolean functions of 3 variables
b) All function of 3 variables but none of 4 variables
c) All functions of 3 variables and some but not all of 4 variables
d) All functions of 4 variables

21)A basic multiplexer principle can be demonstrated through the use of a _____

a) Single-pole relay
b) DPDT switch
c) Rotary switch
d) Linear stepper
Explanation: A combinational circuit that selects one from many inputs is known as Multiplexer. A basic multiplexer principle can be demonstrated through the use of a rotary switch. Because rotary switch gives one output corresponding to their inputs.

22) The inputs/outputs of an analog multiplexer/demultiplexer are _____

a) Bidirectional
b) Unidirectional
c) Even parity
d) Binary-coded decimal
Explanation: One multiplexer can be used as demultiplexer. Hence, it is called bidirectional or two-way transmission.

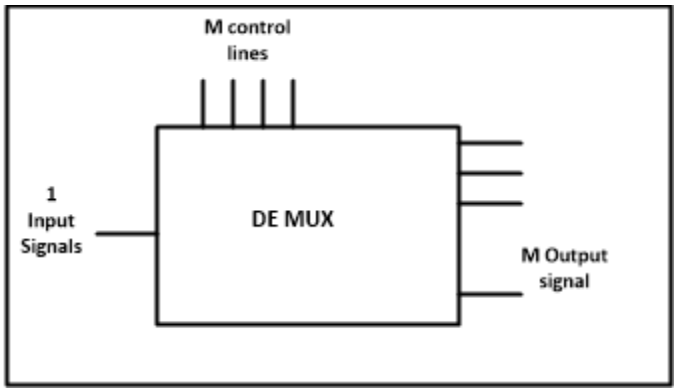
23) If enable input is high then the multiplexer is _____

a) Enable
b) Disable
c) Saturation

d) High Impedance
Explanation: If enable input is high then the multiplexer is disabled because enable input is in inverted mode always (i.e. E').

24)What is data routing in a multiplexer?
a) It spreads the information to the control unit
b) It can be used to route data from one of several source to destination
c) It is an application of multiplexer
d) It can be used to route data and it is an application of multiplexer
Explanation: Multiplexing means passing more than one data through the same channel. Data routing is an application of multiplexer and it can be used to route data from one of several source to destination.

25)The word demultiplex means _____
a) One into many
b) Many into one
c) Distributor
d) One into many as well as Distributor
Explanation: The word demultiplex means "one into many" and distributor. A demultiplexer sends a single input to multiple outputs, depending on the select lines. It is clear from the diagram:



26) Why is a demultiplexer called a data distributor?
a) The input will be distributed to one of the outputs
b) One of the inputs will be selected for the output
c) The output will be distributed to one of the inputs
d) Single input to Single Output

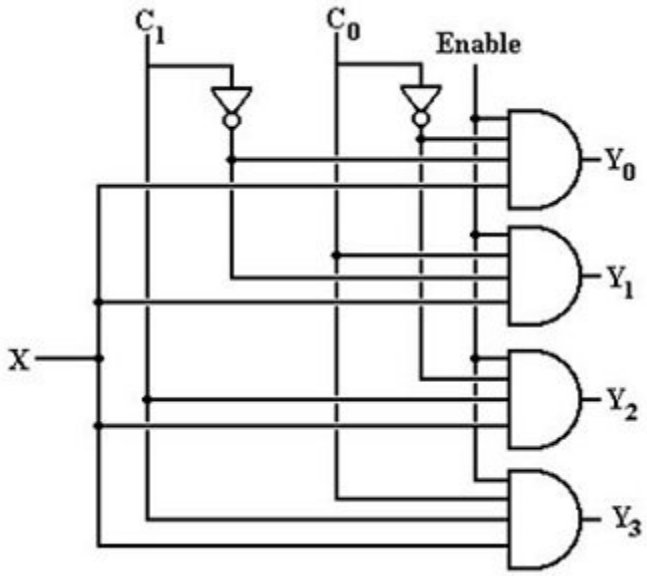
27)Most demultiplexers facilitate which type of conversion?
a) Decimal-to-hexadecimal
b) Single input, multiple outputs

c) AC to DC
d) Odd parity to even parity
Explanation: A demultiplexer sends a single input to multiple outputs, depending on the select lines. Demultiplexer converts single input into multiple outputs.

28)In 1-to-4 demultiplexer, how many select lines are required?
a) 2
b) 3
c) 4
d) 5
29)In a multiplexer the output depends on its _____
a) Data inputs
b) Select inputs
c) Select outputs
d) Enable pin

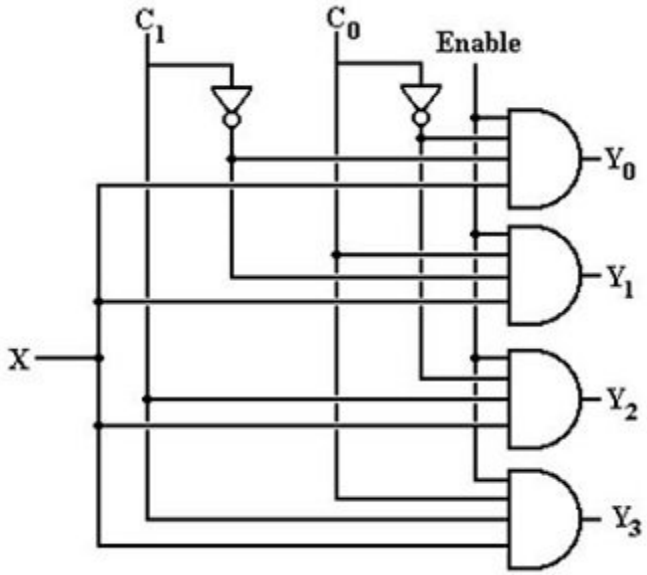
30) In 1-to-4 multiplexer, if C1 = 0 & C2 = 1, then the output will be _____
a) Y0
b) Y1
c) Y2
d) Y3

31)In 1-to-4 multiplexer, if C1 = 0 & C2 = 1, then the output will be _____
a) Y0
b) Y1
c) Y2
d) Y3
Explanation: It can be calculated from the figure shown below:



For C0 =1 and C1 =0, Y1 will be the output as 0 and 1 are the bit combinations of 1.

32) In 1-to-4 multiplexer, if C1 = 1 & C2 = 1, then the output will be _____
a) Y0
b) Y1
c) Y2
d) Y3
Explanation: It can be calculated from the figure shown below:

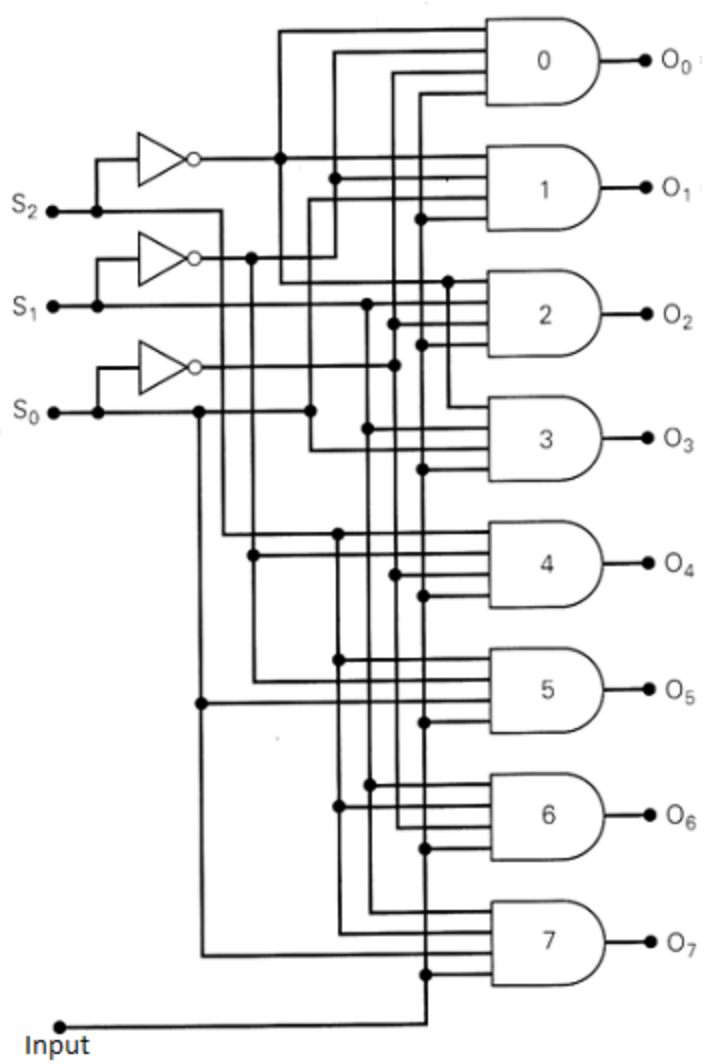


For C0 =1 and C1 =0, Y3 will be the output as 0 and 1 are the bit combinations of 1.

33) How many select lines are required for a 1-to-8 demultiplexer?
a) 2
b) 3
c) 4
d) 5

34)How many AND gates are required for a 1-to-8 multiplexer?
a) 2
b) 6
c) 8
d) 5
Explanation: The number of AND gates required will be equal to the number of outputs in a demultiplexer, which are 8.

35)The output Q4 of this 1-to-8 demultiplexer is _____



a) Q2.(Q1)'.Q0.I
b) Q2.Q1.(Q0)'.I
c) Q2.(Q1)'.(Q0)'.I
d) Q2.(Q1).Q0.I
Explanation: The output Y4 = Q2.(Q1)'.(Q0)'.I. since the bit combinations of 4 are 100.

36) Which IC is used for the implementation of 1-to-16 DEMUX?
a) IC 74154
b) IC 74155
c) IC 74139
d) IC 74138
Explanation: IC 74154 is used for the implementation of 1-to-16 DEMUX, whose output is inverted input.

37)Why is a demultiplexer(data distributor) called a data distributor?
a) The input will be distributed to one of the outputs
b) One of the inputs will be selected for the output
c) The output will be distributed to one of the inputs
d) Single input gives single output

38)Most demultiplexers facilitate which type of conversion?
a) Decimal-to-hexadecimal
b) Single input, multiple outputs
c) AC to DC
d) Odd parity to even parity

39)In 1-to-4 demultiplexer, how many select lines are required?
a) 2
b) 3
c) 4
d) 5

40)In a multiplexer the output depends on its _____
a) Data inputs
b) Select inputs
c) Select outputs
d) Enable pin

41)In 1-to-4 multiplexer, if C1 = 1 & C2 = 1, then the output will be _____
a) Y0
b) Y1
c) Y2
d) Y3

42)How many select lines are required for a 1-to-8 demultiplexer?
a) 2
b) 3
c) 4
d) 5

43)How many AND gates are required for a 1-to-8 multiplexer?
a) 2
b) 6
c) 8

d) 5
Explanation: The number of AND gates required will be equal to the number of outputs in a demultiplexer, which are 8.
44)Which IC is used for the implementation of 1-to-16 DEMUX?
a) IC 74154
b) IC 74155
c) IC 74139
d) IC 74138

45)A decoder converts n inputs to _____ outputs.
a) n
b) n2
c) 2n
d) nn
Explanation: Decoder is a circuit with n input lines and 2n output lines.

46) Which of the following are building blocks of encoders?
a) NOT gate
b) OR gate
c) AND gate
d) NAND gate
Explanation: Encoders are made up of three OR gates.

47) Which of the following can be represented for a decoder?
a) Sequential circuit
b) Combinational circuit
c) Logical circuit
d) None of the mentioned
Explanation: Combinational circuit in which output depends only on the state of inputs.

48)BCD to seven segment conversion is a _____
a) Decoding process
b) Encoding process
c) Comparing process
d) None of the mentioned
Explanation: BCD to seven segment code conversion can be treated as a decoding process.

49)Which of the following is a decoder IC?

a) 7890
b) 8870
c) 4047
d) 4041

50)DTMF stands for _____
a) Dual Tone Magnetic Frequency
b) Double Tone Magnetic Frequency
c) Dual Tone Multiple Frequency
d) Dual Tone Mechanical Frequency
Explanation: DTMF is the short form of Dual Tone Multiple Frequency.

51)Invalid BCD can be made to valid BCD by adding with _____
a) 0101
b) 0110
c) 0111
d) 1001
Explanation: Invalid BCD are numbers greater than 1001, and they can be made valid BCD by adding with 0110.

52)Decoder is constructed from _____
a) Inverters
b) AND gates
c) Inverters and AND gates
d) None of the mentioned
Explanation: Decoder circuits are constructed from Inverters and AND gates.

53)Which of the following represents a number of output lines for a decoder with 4 input lines?
a) 15
b) 16
c) 17
d) 18
Explanation: For n input lined decoder will have 2n output lines.

54) Decoders and Encoders are doing reverse operation.
a) True
b) False

55)How many inputs will a decimal-to-BCD encoder have?

a) 4
b) 8
c) 10
d) 16

56) How many outputs will a decimal-to-BCD encoder have?
a) 4
b) 8
c) 12
d) 16

57)How is an encoder different from a decoder?
a) The output of an encoder is a binary code for 1-of-N input
b) The output of a decoder is a binary code for 1-of-N input
c) The output of an encoder is a binary code for N-of-1 output
d) The output of a decoder is a binary code for N-of-1 output
Thus, an encoder different from a decoder because of the output of an encoder is a binary code for 1-of-N input.

58)If we record any music in any recorder, such types of process is called _____
a) Multiplexing
b) Encoding
c) Decoding
d) Demultiplexing
Explanation: If we record any music in any recorder, it means that we are giving data to a recorder. So, such process is called encoding. Getting back the music from the recorded data is known as decoding.

59)Can an encoder be a transducer?
a) Yes
b) No
c) May or may not be
d) Both are not even related slightly
Explanation: Of course, a transducer is a device that has the capability to emit data as well as to accept. Transducer converts signal from one form of energy to another.

60) How many OR gates are required for a Decimal-to-bcd encoder?
a) 2

b) 10
c) 3
d) 4

61)How many OR gates are required for an octal-to-binary encoder?
a) 3
b) 2
c) 8
d) 10
In the octal to binary encoder there are 8 (=23) inputs, thus 3 output lines.
62)For 8-bit input encoder how many combinations are possible?
a) 8
b) 2^8
c) 4
d) 2^4

63)The discrepancy of 0 output due to all inputs being 0 or D0, being 0 is resolved by using additional input known as _____
a) Enable
b) Disable
c) Strobe
d) Clock

64) Can an encoder be called a multiplexer?
a) No
b) Yes
c) Sometimes
d) Never

65) If two inputs are active on a priority encoder, which will be coded on the output?
a) The higher value
b) The lower value
c) Neither of the inputs
d) Both of the inputs

66) Perform binary addition of 1101 + 0010 is _____
a) 1110
b) 1111
c) 0111

d) 1,1101

67) The addition 1+1 gives 0 as a result.
a) True
b) False

68)11010 + 11100
11010
+11100
110110

69)101011 + 110101
101011
+110101
1100000

70)11011 + 10001
11011
+10001
101100

71)10101 + 110001
10101
+110001
1000110

72) 11110000
+ 1000011001
1100001001

73) 10101000
+ 010001001
100110001

74)101011111
+ 110011010
1011111001

75)Subtract 11010 from 111101.

111101
-11010
100011

76)Subtract 1001 from 1101.
1101
-1001
100

77)Subtract 111001 from 1111001.
1111001
- 111001
1000000

78)_____ is a straightforward method of representing positive and negative numbers.
a) Radix
b) Complement
c) Sign Magnitude
d) Encode
Explanation: Sign Magnitude is used for the representation of positive and negative numbers. If the leftmost digit is 0, the number is positive. If the leftmost digit is 1, the number is negative.

79)The additive inverse of a number is the number which when added to the original number gives 1 as a result.
a) True
b) False
Explanation: Additive Inverse of a number is the number which gives 0 and not 1 when added to the original number. e.g. number=45, additive inverse =-45, after addition they give 0.

80)The 1's complement of 1 in 4 bits is _____
a) 0001
b) 0
c) 1001
d) 1110
Explanation: 1's complement is obtained by reversing the bits from 0 to 1 and vice-versa. Binary of 1 is : 0001 and 1's complement is : 1110.

81)The binary number 111 in its 2's complement form is _____
a) 010
b) 001
c) 000
d) 111
Explanation: 2's complement is obtained by adding 1 to the 1's complement. 1's complement of 111: 000 and 2's complement:001.

82)The sign magnitude representation of -9 is _____
a) 00001001
b) 11111001
c) 10001001
d) 11001
Explanation: In case of a negative number, the leftmost digit is 1 if the number is negative. Therefore, +9=00001001 and -9=10001001. Similarly for all other negative numbers.

83)If you are given a word of size n bits, the range of 2's complement of binary numbers is _____
a) -2^{n+1} to $+2^{n+1}$
b) -2^{n-1} to $+2^{n-1}$
c) -2^{n-1} to $+2^{n+1}$
d) -2^{n-1} to $+2^{n-1}-1$

84)In both signed magnitude and 2's complement , positive and negative numbers are separated using _____
a) LSB
b) MSB
c) 0
d) 1

85)Single Precision format comprises of _____ bits.
a) 4
b) 8
c) 16
d) 32
Explanation: The single precision format comprises of 32-bits. It has 1 sign bit, 8 bits for exponent and 23 for the mantissa.

86) If m is the 2's complement and n is the binary number, then _____
a) m=n'
b) m=n'+1

c) m=n'-1
d) m=n

87)The possible number of bit patterns with 8 bits _____
a) 128
b) 8
c) 24
d) 256
Explanation: The total number of patterns that can be formed using n-bits are 2n. Here, possible patterns are: 28=256.

88): How to represent -9 with signed 2's complement?
10001001
11110110
11110111
11110011

89) Positive integers can be represented as
a)Signed numbers
b)Unsigned numbers
c)Negative integers
d)Both a and b

90) The more convenient system for representing the negative numbers is
a)Signed-complement system
b)Unsigned-complement system
c)Negative integer system
d)Positive integer system

91) 1's complement as a logical operation is equivalent to
a)Logical design
b)Illogical design
c)Logical complement
d)Illogical complement