2.6 Interrupt operations

1)While CPU is executing a program, an interrupt exists then it
a) follows the next instruction in the program
b) jumps to instruction in other registers
c) breaks the normal sequence of execution of instructions
d) stops executing the program
Explanation: An interrupt function is to break the sequence of operation.

2) An interrupt breaks the execution of instructions and diverts its execution to
a) Interrupt service routine
b) Counter word register
c) Execution unit
d) control unit
Explanation: An interrupt transfers the control to interrupt service routine (ISR). After executing ISR, the control is transferred back again to the main program.

3)While executing the main program, if two or more interrupts occur, then the sequence of appearance of interrupts is called
a) multi-interrupt
b) nested interrupt
c) interrupt within interrupt
d) nested interrupt and interrupt within interrupt
Explanation: If an interrupt occurs while executing a program, and the processor is executing the interrupt, if one more interrupt occurs again, then it is called a nested interrupt.

4)Whenever a number of devices interrupt a CPU at a time, and if the processor is able to handle them properly, it is said to have
a) interrupt handling ability
b) interrupt processing ability
c) multiple interrupt processing ability
d) multiple interrupt executing ability
Explanation: The processor if handles more devices as interrupts then it has multiple interrupt processing ability.

5)NMI stands for
a) nonmaskable interrupt
b) nonmultiple interrupt
c) nonmovable interrupt
d) none of the mentioned

6) If any interrupt request given to an input pin cannot be disabled by any means then the input pin is called
a) maskable interrupt
b) nonmaskable interrupt
c) maskable interrupt and nonmaskable interrupt
d) none of the mentioned

7) The INTR interrupt may be
a) maskable
b) nonmaskable
c) maskable and nonmaskable
d) none of the mentioned
Explanation: the INTR (interrupt request) is maskable or can be disabled.

8)The Programmable interrupt controller is required to
a) handle one interrupt request
b) handle one or more interrupt requests at a time
c) handle one or more interrupt requests with a delay
d) handle no interrupt request
Explanation: If more than one interrupt request (INTR) occurs at a time, then an external chip called programmable interrupt controller is required to handle them.

9) The INTR interrupt may be masked using the flag
a) direction flag
b) overflow flag
c) interrupt flag
d) sign flag
Explanation: If a microprocessor wants to serve any interrupt then interrupt flag, IF=1. If interrupt flag, IF=0, then the processor ignores the service.

10)If an interrupt is generated from outside the processor then it is an
a) internal interrupt
b) external interrupt
c) interrupt
d) none of the mentioned
Explanation: If an external device or a signal interrupts the processor from outside then it is an external interrupt.

11)If the interrupt is generated by the execution of an interrupt instruction then it is
a) internal interrupt
b) external interrupt
c) interrupt-in-interrupt

d) none of the mentioned
Explanation: The internal interrupt is generated internally by the processor circuit or by the execution of an interrupt instruction.

12) Example of an external interrupt is
a) divide by zero interrupt
b) keyboard interrupt
c) overflow interrupt
d) type2 interrupt
Explanation: Since the keyboard is external to the processor, it is an external interrupt.

13) Example of an internal interrupt is
a) divide by zero interrupt
b) overflow interrupt
c) interrupt due to INT
d) all of the mentioned

14)The interrupt request that is independent of IF flag is
a) NMI
b) TRAP
c) Divide by zero
d) All of the mentioned

15)The type of the interrupt may be passed to the interrupt structure of CPU from
a) interrupt service routine
b) stack
c) interrupt controller
d) none of the mentioned

16)During the execution of an interrupt, the data pushed into the stack is the content of
a) IP
b) CS
c) PSW
d) All of the mentioned
Explanation: The contents of IP, CS and PSW are pushed into the stack during the execution.

17)After every response to the single step interrupt the flag that is cleared is
a) IF (Interrupt Flag)
b) TF (Trap Flag)

c) OF (Overflow Flag)
d) None of the mentioned

18)At the end of ISR, the instruction should be
a) END
b) ENDS
c) IRET
d) INTR

19)When the CPU executes IRET,
a) contents of IP and CS are retrieved
b) the control transfers from ISR to main program
c) clears the trap flag
d) clears the interrupt flag

20)The interrupt for which the processor has the highest priority among all the external interrupts is
a) keyboard interrupt
b) TRAP
c) NMI
d) INT
Explanation: The Non-Maskable Interrupt input pin has the highest priority among all the external interrupts.

21)The interrupt for which the processor has highest priority among all the internal interrupts is
a) keyboard interrupt
b) TRAP
c) NMI
d) INT

22) In case of string instructions, the NMI interrupt will be served only after
a) initialisation of string
b) execution of some part of the string
c) complete string is manipulated
d) the occurrence of the interrupt

23) The NMI pin should remain high for atleast
a) 4 clock cycles
b) 3 clock cycles
c) 1 clock cycle
d) 2 clock cycles

24) The INTR signal can be masked by resetting the
a) TRAP flag
b) INTERRUPT flag
c) MASK flag
d) DIRECTION flag
Explanation: The INTR signal can be masked by resetting the interrupt flag.

25)For the INTR signal, to be responded to in the next instruction cycle, it must go _____ in the last clock cycle of the current instruction
a) high
b) low
c) high or low
d) unchanged

26)The status of the pending interrupts is checked at
a) the end of main program
b) the end of all the interrupts executed
c) the beginning of every interrupt
d) the end of each instruction cycle

27) Once the processor responds to an INTR signal, the IF is automatically
a) set
b) reset
c) high
d) low

28)If the pin LOCK (active low based) is low at the trailing edge of the first ALE pulse, then till the start of the next machine cycle, the pin LOCK (active low) is
a) low
b) high
c) low or high
d) none of the mentioned

29)With the trailing edge of the LOCK (active low), the INTA (active low) goes low and remains in it for
a) 0 clock cycle
b) 1 clock cycle
c) 2 clock cycles
d) 3 clock cycles
Explanation: The INTA (active low) goes low and remains low for two clock cycles before returning back to the high state.