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## Performance Impact of Hardware **Accelerators and Schedulers on Modern** Computing

Daivik Gangappa, Kyle Maiorana, Kothe Viswanati Syracuse University, dgangapp, kdmaiora , skothe

## I. INTRODUCTION

Hardwar accelerators, schedulers, and parallelism implementations have been used to improve system performance during recent advancements in computational technology. Each of these improvements needs to account for bottlenecks, including memory and power usage, to ensure a net positive benefit. By analyzing architecture decisions being made, this study intends to document the most effective strategies and system configurations for minimizing these pitfalls. Key metrics will be discussed, including raw performance (throughput, latency), energy consumption, and resource utilization. By computing and contrasting various combinations of accelerating

technology against the above metrics, a confident optimal recommendation can be reached for what should be implemented in

## II. BACKGROUND

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In the dynamic world of modern computing, where every microsecond counts, the goal of peak performance is a never-ending process. This research study goes into the complex world of schedulers, hardware accelerators, and parallelism implementation, attempting to understand the massive impact on the efficiency of modern computing systems. With the constantly evolving technology and the unpredictable computational challenges from energing fields of machine learning to the complicated interconnected network, there is a crucial demand for fresh approaches to improve system performance.

According to Semiconductors.org and Investopedia.com, the major players working on developing these performance-enhancing technologies are Samsung, Taiwan Semiconductor Company, NVIDIA Corporation, and Intel Corporation (1)[8]. As more options for parallelized and optimized technology reach consumer markets, the ideal combination of system components has become more complex. Despite this context, the study involves a detailed examination of the complicated