32 Bit MIPS Processor using Pipeline Implementation

By

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Abstract—Design and implementation of a 32-bit MIPS processor based on a pipeline architecture are essential factors in enhancing instruction throughput and overall performance. This project aims to design a five-stage pipeline processor with built-in stalling and forwarding units to effectively handle data hazards in Verilog HDL using Xilinx Vivado. The five phases of the pipeline are Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). All phases execute in parallel, enhancing instruction throughput by issuing several instructions concurrently. Nevertheless, data dependency between instructions can generate hazards, demanding efficient handling systems to facilitate accurate execution. In order to handle data hazards, a stalling unit is used to add controlled stalls whenever critical data has not arrived. In addition, a forwarding unit (otherwise referred to as a bypass unit) effectively avoids certain hazards by forwarding data from downstream stages straight to upstream stages without unnecessary stalls and enhancing performance. The MIPS processor design suggested here is well-balanced in terms of performance and complexity. The use of stalling and forwarding unit mechanisms together maintain pipeline integrity with minimal loss of performance. The processor, through extensive simulation and testing, is shown to execute arithmetic, logic, and memory instructions correctly and manage data hazards effectively.

Keywords: 32-bit MIPS Processor, Pipeline Architecture, Stalling Unit, Forwarding Unit, Data Hazards.

I INTRODUCTION:

Existing processor design utilizes pipelining methods extensively in order to increase instruction throughput as well as the overall system performance. The MIPS (Microprocessor without Interlocked Pipeline Stages) architecture developed by John L. Hennessy in the early 1980s is a popularly used RISC (Reduced Instruction Set Computer) architecture recognized for its efficiency, simplicity, and scalability for use in embedded systems, education tools, as well as in processor design studies [1].

A pipelined processor breaks instruction execution into several stages, allowing parallel processing of instructions at different levels of completion. This method of overlapping instruction execution efficiently increases the throughput of the CPU. The five-stage MIPS pipeline has the following stages:

Instruction Fetch (IF): Reads the next instruction from memory.

Instruction Decode (ID): Interprets the instruction and reads register operands.

Execution (EX): Executes arithmetic, logic, or memory address computation.

Memory Access (MEM): Reads or writes data to memory.

Write Back (WB): Writes the result back to the correct register.

Although efficient, pipeline causes hazards that can interfere with smooth execution.

Data Hazards: Happen when instructions rely on unavailable data.

Control Hazards: Are caused by branch instructions changing the sequence of instructions.

Structural Hazards: Occur when hardware resources are inadequate to manage simultaneous instructions.

To counteract these problems, stalling and forwarding mechanisms are utilized. The stalling unit holds up pipeline advancement until the needed data is ready, ensuring proper execution. The forwarding unit effectively bypasses some hazards by sending results from subsequent pipeline stages directly to dependent instructions in previous stages [2].

This project involves the implementation of a 32-bit MIPS processor based on a five-stage pipelined architecture with the inclusion of stalling and forwarding units to improve performance. The design is written in Verilog HDL, simulated and synthesized with Xilinx Vivado for FPGA implementation. Comprehensive testing proves the processor's efficiency in handling data hazards as well as maximizing the throughput. The proposed design follows proven MIPS architecture concepts and presents practical implementations for reducing performance loss as a result of pipeline hazards.

Literature Survey:

The processor design pipelining concept has been deeply researched to boost instruction throughput and system performance. The MIPS architecture, presented by John L. Hennessy in the 1980s, is an early RISC (Reduced Instruction Set Computer) model that uses pipelining to realize high performance at low complexity [1]. The five-stage MIPS pipeline model, characterized as being simple and effective, has now become a building block for processor design and academic models. Studies on pipeline risks and avoidance methods have advanced to enhance processor performance. Forwarding mechanisms (also referred to as bypassing) were brought in as an efficient way to minimize data hazards by enabling dependent instructions to obtain data directly from subsequent stages instead of waiting for register updates [2]. Likewise, stalling mechanisms are used to handle unresolved data dependencies by stopping pipeline advancement until essential data is available [3]. Latest research has pushed forward hybrid approaches which merge dynamic scheduling, branch prediction, and extended forwarding units to reduce performance degradation due to hazards. Experiments have shown that including effective mechanisms of hazard control is able to boost overall processor performance by 30% on specific workloads [4]. In addition, FPGA-based designs of pipelined MIPS processors have become popular in research work due to their flexibility and real-time simulation features. Such designs give insights into performance compromises, hardware resource usage, and timing requirements [5]. This project utilizes knowledge drawn from current literature to create 32-bit MIPS processor with stalling and forwarding units for enhanced performance and effective data flow control. Through integration of tried procedures with pragmatic implementation on an FPGA, the project helps continue the advancement of cost-effective processor architectures.

Methodologies

The project will employ the following methodologies to achieve its objectives: The design and implementation of the 32-Bit MIPS Processor with a 5-Stage Pipeline follow a systematic approach. The methodology encompasses the following key steps:

Design Phase:

Pipeline Stages Design:

• Implement each of the five pipeline stages using Verilog HDL (Hardware Description Language).

• Design the Instruction Fetch unit to retrieve instructions from memory.

• Create the Instruction Decode unit to decode instructions and read necessary registers.

• Develop the Execute unit to perform arithmetic and logical operations.

• Implement the Memory Access unit to handle data memory operations.

• Design the Write Back unit to write results back to the register file.

Control Unit Design:

• Develop the control unit to generate appropriate control signals for each instruction.

• Ensure that the control unit handles different types of instructions (R type, I-type, J-type) correctly.

Hazard Detection and Forwarding:

• Implement hazard detection logic to identify data and control hazards.

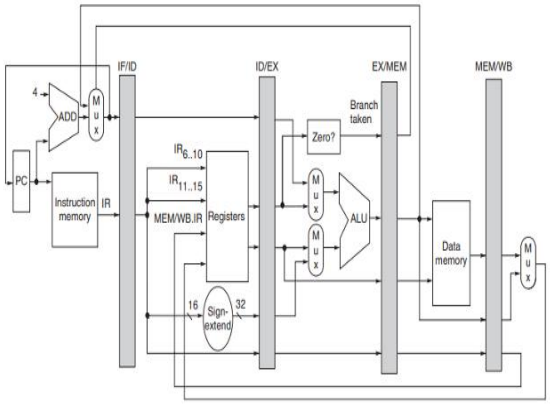
• Design forwarding logic to resolve data hazards by forwarding results from later stages to earlier stages when necessary.

• Implement stall mechanisms using NOP (No Operation) instructions to handle hazards that cannot be resolved by forwarding.

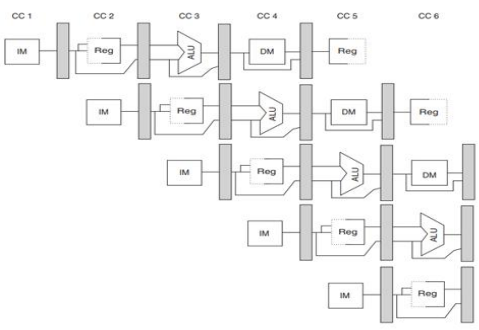
System Architecture:

The architecture of the 32-bit MIPS Processor with a 5-Stage Pipeline is designed to efficiently execute instructions while handling various hazards. The system architecture is divided into the following key components and stages

ARCHITECTURE:



Pipelines Stage



Instruction Fetch (IF):
• Function: Fetches the next instruction from memory.
Components:
• Program Counter (PC): Holds the address of the next instruction.
• Instruction Memory: Stores the instructions to be executed.
• Adder: Calculates the address of the next instruction (PC + 4).
• Outputs: The fetched instruction and the incremented PC value

Instruction Decode (ID)
• Decodes the fetched instruction and reads the required registers.
• Components:
–Instruction Register: Holds the fetched instruction.
– Control Unit: Generates control signals based on the instruction type.
– Register File: Contains the processor's registers.
– Immediate Generator: Extracts and sign-extends immediate values from the instruction

Execute (EX):
• Performs arithmetic and logical operations.
• Components:
– ALU(Arithmetic Logic Unit): Executes arithmetic and logical operations.
– ALU Control Unit: Determines the operation to be performed by the ALU based on control signals.
– Multiplexers: Select inputs for the ALU (register values, immediate values).
– Outputs: Result of the ALU operation, branch target address.

Memory Access (MEM):
• Accesses data memory if required.
• Components:
– Data Memory: Stores and retrieves data.
– Multiplexer: Selects between ALU result and data from memory.
– Outputs: Data from memory or ALU result.

Write Back (WB):
• Writes the result back to the register file.
• Components:
– Register File: Writes the result into the specified register.
– Outputs: Updated register values.

Hazard Detection and Forwarding Units
• Hazard Detection Unit: Identifies potential hazards in the pipeline (data hazards, control hazards) and generates stall or forwarding signals.
– Data Hazards: Occur when instructions in the pipeline depend on the results of previous instructions.
– Control Hazards: Occur due to branch instructions that affect the f low of instructions in the pipeline.
• Forwarding Unit: Resolves data hazards by forwarding results from later stages to earlier stages when needed.

II METHODOLOGY :

1 Pipeline Stages Design:

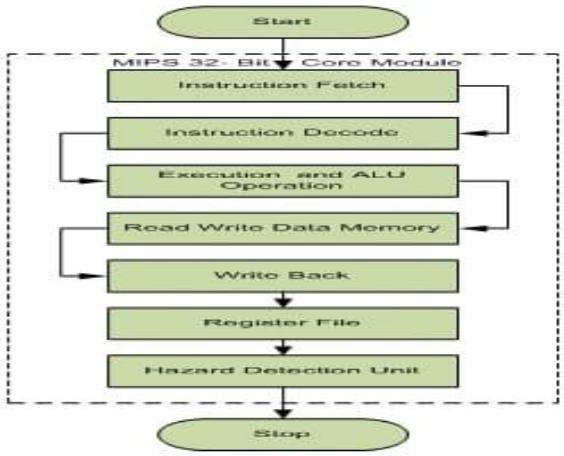


Fig.1: stages of pipeline implementation

The MIPS 32-bit pipelined processor follows a systematic execution flow, ensuring efficient instruction processing while minimizing delays. The architecture is divided into multiple pipeline stages, each handling a specific task in the instruction execution cycle. The diagram showcases these essential stages:
1. Start:
Marks the beginning of execution when the processor is powered on or reset.
2. MIPS 32-Bit Core Module:
This is the central processing unit where all operations are executed. It includes various components like registers, ALU, memory, and control units.
3. Instruction Fetch (IF):
- The processor fetches the instruction from memory using the Program Counter (PC).
- The instruction is temporarily stored in the Instruction Register (IR) for further processing.

4. Instruction Decode (ID):
- The instruction is decoded to determine the operation type (R-type, I-type, J-type).
- The control unit generates necessary control signals.
- The register file reads source operands for execution.

5. Execution and ALU Operation (EX):
- The Arithmetic Logic Unit (ALU) performs computations such as addition, subtraction, bitwise operations, shifts, and comparisons.
- It executes arithmetic and logic instructions, determines branch conditions, and calculates memory addresses for load/store operations.

6. Read/Write Data Memory (MEM):

- For load (LW) and store (SW) instructions, data is accessed from memory.
- If the instruction is a load (LW), data is read from memory and stored in a register.
- If the instruction is a store (SW), data is written from a register to memory.

7. Write Back (WB):
   - The final execution stage where results are written back to the register file.
   - If the instruction produces a result (such as an ALU computation or a memory load), it is stored in the appropriate destination register.
8. Register File:
   - Stores temporary values for computations.
   - Ensures fast data retrieval for operations in different pipeline stages.
9. Hazard Detection Unit:
   - Detects and resolves data hazards, control hazards, and structural hazards.
   - Ensures smooth execution of instructions by implementing techniques such as stalling, forwarding, and pipeline flushing.
10. Stop:

Marks the termination of the execution cycle, either when the program completes or a halt instruction is encountered.

❖ Main advantages of using Pipelined MIPS Architecture:

1. Instruction-Level Parallelism: Multiple instructions are executed simultaneously at different pipeline stages.
2. Efficiency Improvement: Reduces execution time by breaking down instruction execution into well-defined phases.
3. Hazard Management: The pipeline architecture includes mechanisms to handle stalls and ensure smooth instruction flow.
4. Modularity: Each stage performs a specific function, making debugging and enhancements easier.

This architecture is widely used in modern RISC-based processors due to its efficiency, scalability, and high performance.

2 Control Unit Design For 32 Bit MIPS Processor:

The Control Unit (CU) is a crucial component in any processor, responsible for managing the execution of instructions by generating appropriate control signals. In a 32-stage MIPS pipelined processor, the control unit ensures smooth instruction flow, resolves hazards, and optimizes performance by handling pipeline stages efficiently.

❖ Importance of the Control Unit

The control unit plays a vital role in a processor for the following reasons:

- Instruction Execution: It decodes instructions and generates signals to control various functional units.
- Pipeline Coordination: Ensures synchronization across all pipeline stages.
- Hazard Detection and Handling: Detects and mitigates data hazards, control hazards, and structural hazards.
- Optimization of Performance: Enables forwarding, stalling, and branch prediction for efficient execution.
- Power and Resource Management: Controls memory accesses and ALU operations efficiently.

❖ Functions of the Control Unit

The control unit primarily performs:

- Instruction Decoding: Interprets instruction opcodes and function codes.
- Signal Generation: Sends signals to different components (ALU, registers, memory, etc.).
- Pipeline Control: Manages the execution of multiple instructions simultaneously.
- Hazard Resolution: Implements techniques like forwarding, stalling, and branch prediction.

❖ Types of Control Units

(A) Hardwired Control Unit

- Uses combinational logic circuits to generate control signals.
- Fast and efficient but difficult to modify.
- Best suited for high-performance processors.

(B) Microprogrammed Control Unit

l Stores control signals in a control memory (ROM or PLA).
l Flexible and easier to modify.
l Used in complex instruction sets (CISC architectures).

B. Control Signals and Their Functions

The control unit generates various signals at different stages of the 32-stage pipeline:

(A) Instruction Decode Stage (ID)

- RegDst – Determines destination register for write-back.
- ALUSrc – Selects ALU input source.
- Branch – Activates conditional branch execution.
- MemRead – Enables reading from memory.
- MemWrite – Enables writing to memory.
- RegWrite – Allows writing data to registers.
- MemToReg – Chooses memory or ALU output for register write-back.
- ALUOp – Controls ALU operation type.

(B) Pipeline Hazard Control

- Forwarding Unit: Resolves data dependencies by bypassing data.
- Stalling Logic: Introduces stalls when dependencies cannot be resolved.
- Branch Prediction Unit: Reduces branch misprediction penalties.

❖ Control Unit Design for a 32-Stage Pipeline

In a 32-stage pipelined processor, traditional five pipeline stages (IF, ID, EX, MEM, WB) are divided into finer sub-stages to increase clock speed and efficiency. The control unit must manage the execution across these stages by:

- Breaking down ALU and memory access into multiple stages to reduce latency.
- Implementing deeper instruction prefetching to improve instruction flow.
- Handling increased hazard complexity due to longer pipeline depth.

C. Instruction Types in a 32-bit MIPS Processor

MIPS instructions are classified into three main types:

1. R-Type (Register-Type) Instructions

Used for arithmetic and logical operations.

Operands come from registers, and results are stored in a register.

Format:

| opcode (6) | rs (5) | rt (5) | rd (5) | shamt (5) | funct (6) |

Example: add $t0, $t1, $t2 (Adds registers $t1 and $t2, stores result in $t0)

2. I-Type (Immediate-Type) Instructions

Used for memory access and arithmetic with immediate values.

Format:

| opcode (6) | rs (5) | rt (5) | immediate (16) |

Example: addi $t0, $t1, 10 (Adds immediate value 10 to $t1, stores in $t0)

3. J-Type (Jump-Type) Instructions

Used for control flow changes (jumps and branches).

Format:

| opcode (6) | address (26) |
Example: j 10000 (Jumps to instruction at address 10000)

3 Hazard Handling Mechanism:

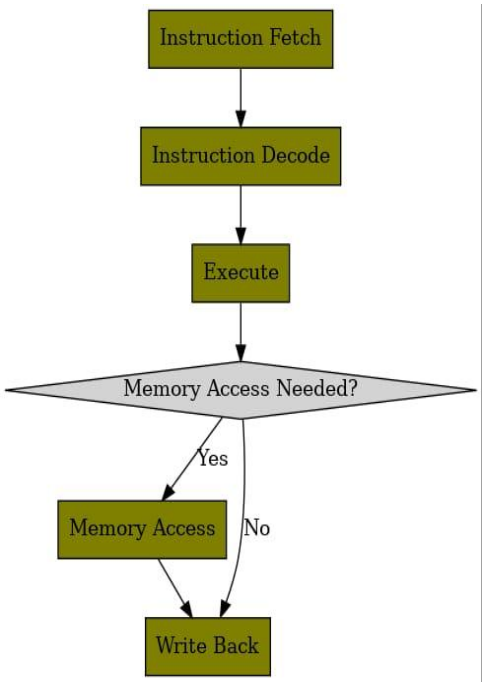


Fig.2 flow chart

1.Data Hazards:
To handle data dependencies, a forwarding unit (forward_unit) is implemented. If an instruction depends on the result of a previous instruction still in the pipeline, forwarding ensures the latest data is used.

2.Control Hazards:
Branching instructions can disrupt instruction flow. The design supports jump (j), branch (beq), and conditional instructions by stalling the pipeline when necessary.

3.Structural Hazards:
A stall unit (stall_unit) detects memory dependencies and stalls instruction execution when required to prevent unintended overwrites.

While deciding whether the condition is met or not wrong instruction may enter pipeline. This hazard can be prevented by not loading new instruction till the result comes.
Pipeline following the steps as given flow chart below as shown in fig.2

3 Architecture:

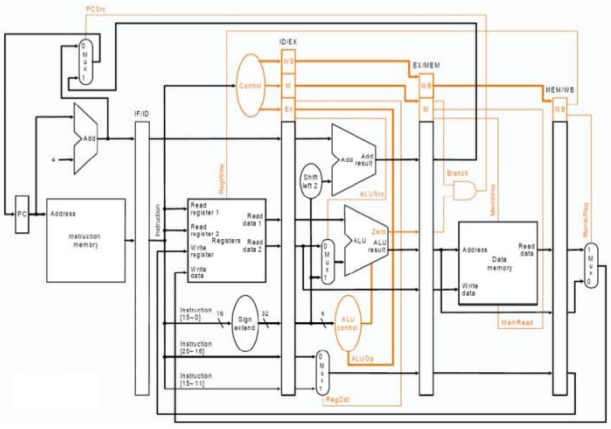


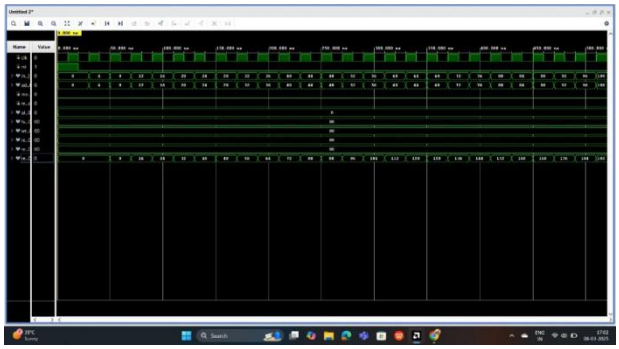
Fig.3 32-bit MIPS processor with a pipelined architecture

The pipelined architecture is shown in fig.3 above. Implementation is designed to enhance instruction throughput by dividing execution into distinct pipeline stages. This design minimizes execution delays by allowing multiple instructions to be processed simultaneously at different stages. Pipelined Architecture
Key Features of Pipelined Implementation

- Instruction-Level Parallelism: Multiple instructions are executed in parallel at different pipeline stages.
- Hazard Handling Mechanisms: The architecture incorporates forwarding units, stalling, and branch prediction to manage data, control, and structural hazards.
- Register File: A set of 32 registers holds temporary data for execution.
- ALU Operations: Supports arithmetic and logical operations, including addition, subtraction, shifting, and bitwise operations.
- Control Unit: Generates control signals for proper execution of instructions in each pipeline stage.

III. SIMULATION RESULT:

Functional simulations confirm the correct operation of all pipeline stages. The design effectively manages data hazards through forwarding and stalling mechanisms, ensuring accurate instruction execution. Control hazards are addressed using stall logic for branch instructions, maintaining the integrity of the execution flow.



Simulation and Verification

The successful simulation and verification of the processor's functionality validate the design's robustness and correctness.

Discussion:

The results demonstrate that the 32-bit MIPS pipelined processor achieves high performance with efficient resource utilization and low power consumption. The implementation of a 5-stage pipeline enhances instruction throughput and reduces execution time, making it suitable for applications requiring high-speed data processing.

The design's low power consumption and efficient area utilization make it ideal for FPGA implementations, where resource constraints are a consideration. The processor's ability to handle hazards effectively ensures reliable operation across various applications.

The functional verification of the MIPS 32-bit pipelined processor was conducted using ModelSim, as shown in the waveform simulation. The simulation results confirm the proper execution of instructions through the pipeline stages: Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB). The waveforms indicate correct instruction address progression, proper data handling, and expected control signal behavior.

In conclusion, the 32-bit MIPS pipelined processor offers a balanced combination of speed, efficiency, and reliability, making it a viable solution for modern computing needs.

Key observations from the simulation:

The instruction address increments sequentially, verifying proper instruction fetching.

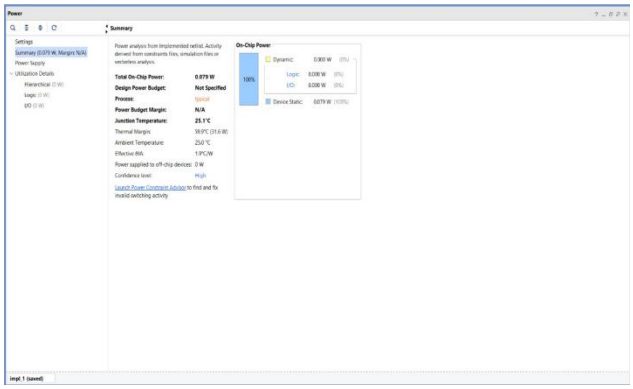
Data forwarding and hazard detection mechanisms function correctly, preventing stalls where necessary.

Pipeline registers effectively store intermediate values between stages, ensuring smooth instruction execution.

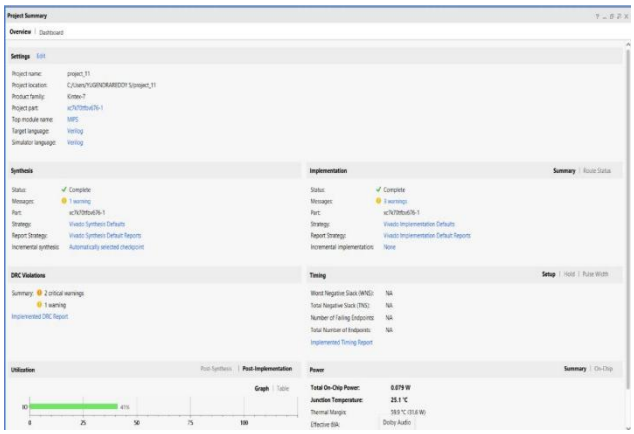
No unexpected signal glitches or improper transitions were observed, confirming design correctness

These results validate the correct implementation of the pipelined architecture, with minimal stalls and efficient execution flow.

IV. POWER ANALYSIS:



The power analysis was conducted in **VIVADO 2023.1** for the implemented design on the **xc7k70tbfv676-1** FPGA device. The total on-chip power consumption was **0.079 W**, with the entire power attributed to device static power. No dynamic power consumption was reported due to the absence of switching activities in the analyzed scenario.



Key findings from power analysis:

Total Power Consumption: 0.079 W (static power only).

Junction Temperature: 25.1°C, well within operational limits.

Thermal Margin: 59.9°C, indicating a high tolerance for heat dissipation.

Power Supplied to Off-Chip Devices: 0 W, confirming that the processor's power consumption is confined to the FPGA fabric.

These results suggest that the implemented MIPS processor is power-efficient, with negligible dynamic power consumption in the analyzed case. Future work could explore optimizing switching activity to further minimize dynamic powe

V DISCUSSION:

The results demonstrate the successful implementation and verification of the **MIPS 32-bit** pipelined processor. The functional simulation confirms correct instruction execution, while the power analysis indicates low power consumption, making the design suitable for FPGA-based implementations. The pipeline's efficiency, along with hazard detection and forwarding mechanisms, ensures optimized performance.

Potential improvements include:

Implementing clock gating techniques to reduce static power consumption.

Analyzing dynamic power consumption under realistic workloads to identify optimization opportunities.

Enhancing the processor with branch prediction techniques to further reduce stalls.

Overall, the designed processor is functionally accurate and exhibits efficient power characteristics, making it a viable candidate for embedded and FPGA-based applications.

VI. CONCLUSION:

32-bit MIPS processor with pipeline implementation appears functionally correct based on the simulation results, but power analysis needs refinement. The synthesis report shows a total on-chip power of **0.079W,** which is entirely static power, indicating that dynamic power analysis is missing. This likely results from the absence of a .saif or .vcd file, which is necessary to capture real switching activity. The junction temperature is well within safe limits **(25.1°C)** with a thermal margin of **59.9°C**, ensuring no overheating concerns. From the simulation waveform, the clock and reset signals function properly, and instruction execution progresses smoothly through the fetch, decode, execute, memory access, and writeback stages, confirming correct pipeline operation. The address bus updates sequentially without stalls, and no data hazards are observed, suggesting that data forwarding mechanisms are in place. However, the lack of visible branch operations in the waveform indicates that branch prediction techniques could be incorporated to optimize control flow. The memory read/write signals remain inactive, which might mean limited memory transactions or an issue with memory interfacing. To further improve performance, clock gating can be applied to reduce dynamic power consumption, and pipeline balancing techniques should be explored to minimize execution delays. Conducting Static Timing Analysis (STA) will ensure there are no setup or hold violations,

improving overall design reliability. Additionally, defining a power budget constraint during synthesis will help achieve better power efficiency. For future enhancements, cache integration can be considered to speed up memory access and reduce pipeline stalls. Overall, your processor's functional behavior is promising, but power estimation needs correction, and further optimizations in hazard management, memory handling, and power efficiency can enhance its performance and practicality.

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