APB AVIP

mirafra TECHNOLOGIES



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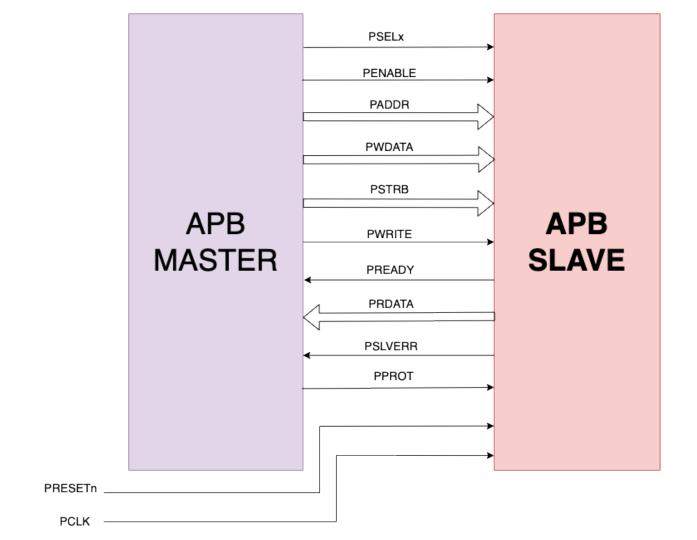
Introduction

- APB is part of the AMBA (Advanced Microcontroller Bus Architecture) protocol family.
- It defines a low-cost interface that is optimised for minimal power consumption and reduced interface complexity.
- Not pipelined, used to connect to low-bandwidth peripherals.
- APB can be interfaced with AHB, AHB-lite, AXI and AXI4.
- Used to access the programmable control registers of the peripheral devices.

KEY FEATURES

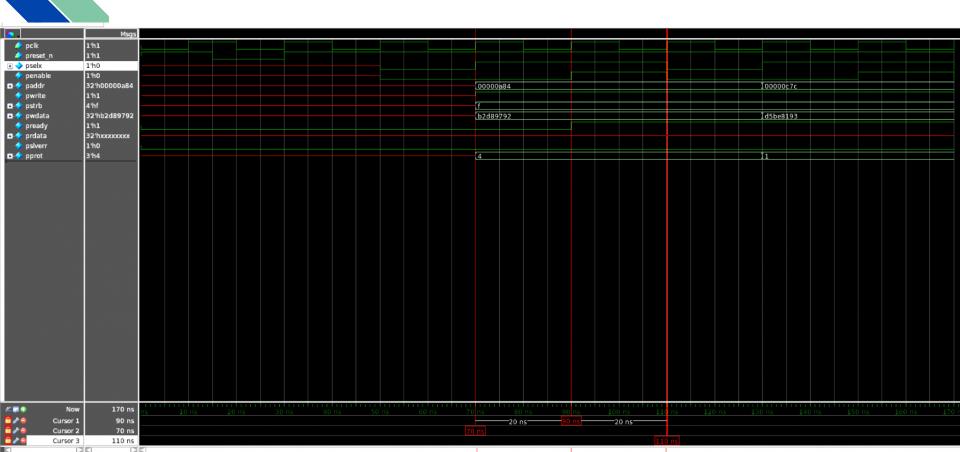
- It supports addresses up to 32 bit wide.
- APB4 support for write strobe signal to enable data transfer on the write data bus.
- Single Master Single Slave.
- Programmable wait state insertion.
- Random PSLVERR insertion.
- User preferred read-data configuration.
- In APB, every transfer takes at least two cycles (Setup Phase and Access Phase).
- Supports Memory Mapping

APB4 INTERFACE



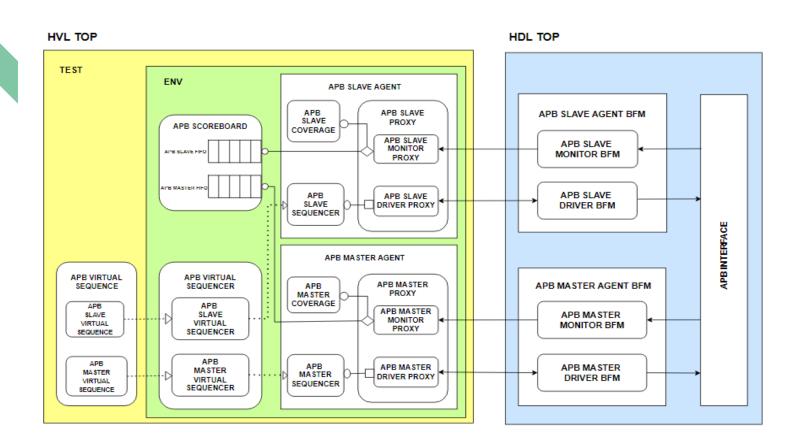
Signal	Source	Description
PCLK	Clock source	Clock. The rising edge of PCLK times all transfers on the APB.
PRESETn	System bus equivalent	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PADDR	APB bridge	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
PPROT	APB bridge	Protection type. This signal indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
PSELx	APB bridge	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a PSELx signal for each slave.
PENABLE	APB bridge	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PWRITE	APB bridge	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PWDATA	APB bridge	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is HIGH. This bus can be up to 32 bits wide.
PSTRB	APB bridge	Write strobes. This signal indicates which byte lanes to update during a write transfer. There is one write strobe for each eight bits of the write data bus. Therefore, PSTRB[n] corresponds to PWDATA[(8n + 7):(8n)]. Write strobes must not be active during a read transfer.
PREADY	Slave interface	Ready. The slave uses this signal to extend an APB transfer.
PRDATA	Slave interface	Read Data. The selected slave drives this bus during read cycles when PWRITE is LOW. This bus can be up to 32-bits wide.
PSLVERR	Slave interface	This signal indicates a transfer failure. APB peripherals are not required to support the PSLVERR pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.

Basic APB timing diagram



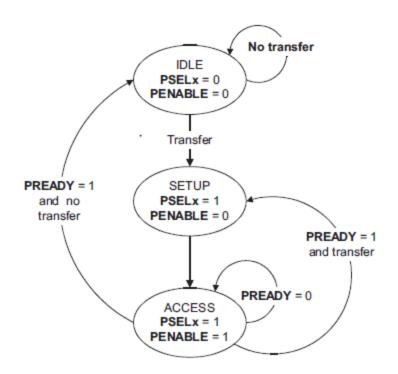
PLANNING PHASE

Verification Plan	->
apb_avip_verification_plan	
Coverage Plan	->
apb avip coverage plan	
Assertion Plan	->
apb avip assertion plan	



Implementation

APB Flowchart



Flowcharts

Master Driver	->
apb avip master driver flowchart	
Slave Driver <u>apb_avip_slave_driver_flowchart</u>	->
Master Monitor <u>apb_avip_master_monitor_flowchart</u>	->
Slave Monitor <u>apb avip slave monitor flowchart</u>	->
Scoreboard Run Phase ->	

APB Environment Configuration

APB_ENV_CONFIG			
Name	Туре	Size	Value
<pre>apb_env_cfg_h has_scoreboard has_virtual_seqr no_of_slaves</pre>	apb_env_config integral integral integral	1 1 32	@496 1 1 'd1

APB Master Agent Configuration

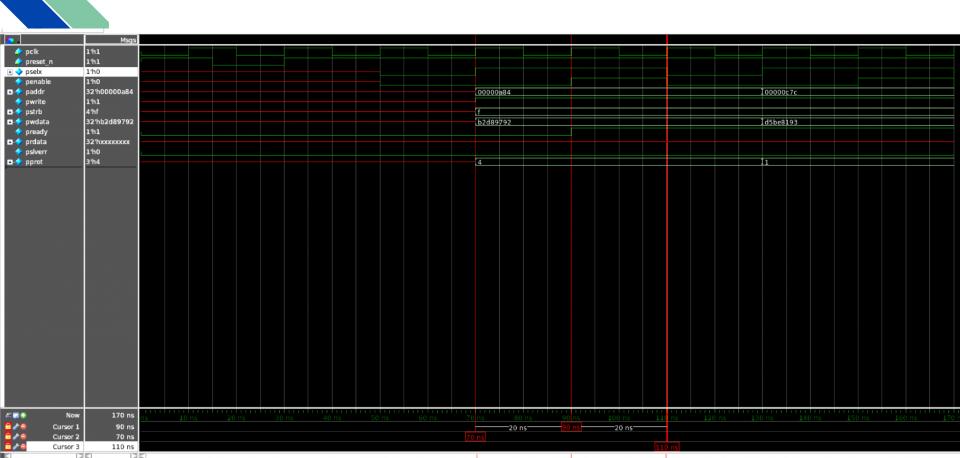
APB_MASTER_AGENT_CONFIG			
Name	Туре	Size	Value
<pre>apb_master_agent_config is_active has_coverage no_of_slaves master_min_addr_range_array[0] master_max_addr_range_array[0]</pre>	apb_master_agent_config integral integral integral integral integral	1 1 32 32 32	@497 1 1 'd1 'h0 'hfff

APB Slave Agent Configuration

APB_SLAVE_CONFIG[0]			
Name	Туре	Size	Value
apb_slave_agent_config[0] is_active slave_id has_coverage max_address min_address	apb_slave_agent_config string integral integral integral integral integral	10 32 1 32 32 32	@502 UVM_ACTIVE 'd0 1 'hfff 'h0

OUTPUT

OUTPUT WAVEFORM



Coverage

Coverage Summary by Type:

Total Coverage:			36.23%	35.80%		
Coverage Type ∢	Bins ∢	Hits ∢	Misses ∢	Weight ∢	% Hit ∢	Coverage -
Covergroups	417	37	380	1	8.87%	31.67%
Statements	1269	549	720	1	43.26%	43.26%
Branches	959	243	716	1	25.33%	25.33%
FEC Conditions	13	4	9	1	30.76%	30.76%
Toggles	1109	532	577	1	47.97%	47.97%

DEMO

References

- 1. APB TB ARCHITECTURE DIAGRAM
- 2. APB TB DOCUMENT
- 3. APB AVIP USER GUIDE
- 4. APB GITHUB LINK

Q & A

Thank You