DESIGN VERIFICATION ENGINEER

Jahnavi Vallivedu, Verification Engineer, Mirafra Technologies

EXPERIENCE SUMMARY

Experience Level: 6 months

Now: Mirafra Software Technologies Pvt. Ltd., August 2022 – Present

Education:

BTech in Electronics and Communication, 2022, sri venkateswara University, CGPA:8.18

DIPLOMA IN ECE, 2019, Sri venkateswara government polytechnic college, Percentage: 95%

IP/Protocols known:	AMBA-APB,AXI,I2C
Scope of Verification:	IP, Subsystem
Verification Approaches:	Functional based
Verification Language:	System Verilog
Methodology:	UVM
HDL:	Verilog
Scripting Language:	Python (Basic)
Tools Experienced:	Mentor Graphics-Questasim,Synopsys-VCS, cadence
Editors used:	Gvim
Open Source used:	GitHub
Subject:	Basics of Computer Architecture

PROJECT EXPERIENCE

Project 1:	**Accelerated VIP AMBA APB protocol verification**
Company:	Mirafra Technologies Pvt. Ltd.
Duration:	November 2022 - Present
Role:	Individual Contributor
Tools:	Questasim
Languages:	System Verilog (UVM based)
Description:	APB defines a low cost interface that is optimized for minimal power consumption and reduced interface complexity. The APB protocol is not pipelined, it connects to low-bandwidth peripherals that do not require the high performance of the AXI protocol.

Accomplishments:

- ***Verification plan, Assertion plan, Coverage plan*** development.
- Developed the testbench architecture which is mapped onto the ***emulator*** as well.
- Created the HDL Top, interface, monitor BFMs (master and slave).

- Implemented ***memory-mapping*** to store data and added constraints in ***post randomize*** method.
- Developed ***testcases*** and ***scoreboard.***

Project 2: **IOT BASED SMART JACKET FOR WOMEN SAFETY**

College: sri venkateswara university
Duration: November 2021 - June 2022
Role: Individual Contributor
Tools: Arduino IDE software,Hardware components
Description: In this embedded project a wearable jacket is designed which includes mainly sensors and switches with IOT technology. The main aim of this project is to give the location of the particular women whenever they attacked by others through GSM module as an SMS. The hardware components like vibration sensor, temperature sensor, NodeMCU, GPS module and GSM module are inbuilt into the jacket. Each switch is placed in the jacket with equal space to cover total jacket. This project requires internet for accessing the Google assistance in their mobile.

Accomplishments:
• Provides location of women through GPS module

• Sends the SMS to recipient of women through GSM module

• Women can protect herself even without internet through sensor and switch mode

Project 3: **UVM FRAMEWORK (UVMF)**
Company: Mirafra Technologies Pvt. Ltd.
Duration: December 2022 - Present
Role: Individual Contributor
Tools: Questasim
Languages: System Verilog (UVM based)
Description: UVMF is a open source package provided by siemens, the overview of the concept is we can able to generate a uvm testbench code for any given architecture blocks diagrams by knowing the yaml language. The yaml files is the input and python is able to convert the yaml files in to the UVM testbench code. An advantage of this project is that a single person can develop the testbench code in a single day.

Accomplishments:
- Understood how UVMF propagates using YAML inputs.
- created the YAML files for testbench, Environment, Interface and Util components and was able to generate the complete testbench code for the given testbench architecture.

- Compiled and Simulated generated UVM testbench code successfully.

WORKSHOPS and AWARDS

- Certificate completion of “VLSI systems on SOC” by “MAVEN SILICON “.
- Completion of "CCNA routing and switching" under "cisco" certification.
- Participated in "IOT "workshop conducted at SV University.
- Participated in cybersecurity conducted by e Saksham with AICTE.