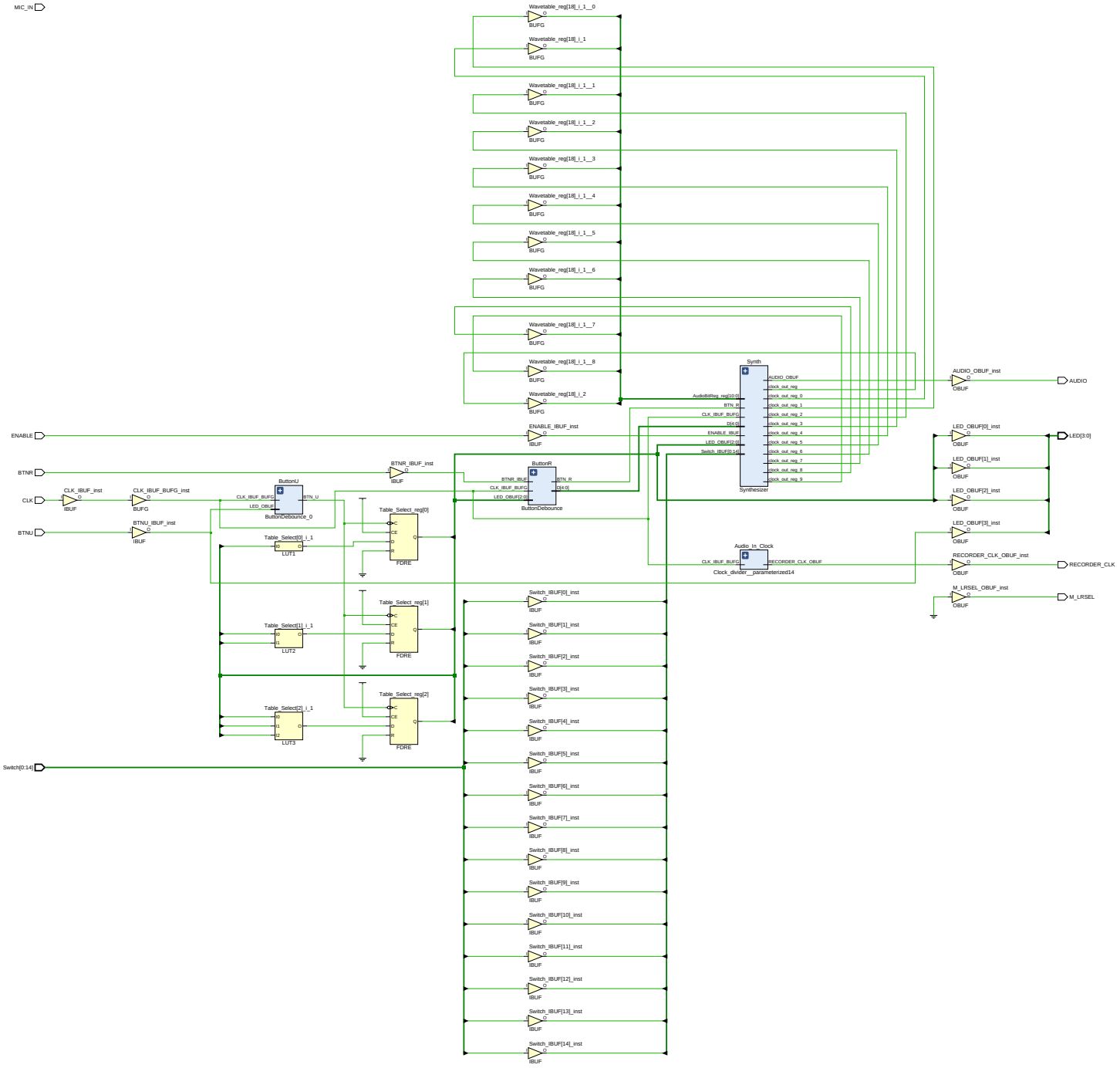
MIC_IN
Wavetable_reg[18]_i_1__0
BUFG
Wavetable_reg[18]_i_1
BUFG
Wavetable_reg[18]_i_1__1
BUFG
Wavetable_reg[18]_i_1__2
BUFG
Wavetable_reg[18]_i_1__3
BUFG
Wavetable_reg[18]_i_1__4
BUFG
Wavetable_reg[18]_i_1__5
BUFG
Wavetable_reg[18]_i_1__6
BUFG
Wavetable_reg[18]_i_1__7
BUFG
Wavetable_reg[18]_i_1__8
BUFG
Wavetable_reg[18]_i_2
BUFG
Synth
AUDIO_OBUF
clock_out_reg
clock_out_reg_0
clock_out_reg_1
clock_out_reg_2
clock_out_reg_3
clock_out_reg_4
clock_out_reg_5
clock_out_reg_6
clock_out_reg_7
clock_out_reg_8
clock_out_reg_9
AudioBitReg_reg[10:0]
BTN_R
CLK_IBUF_BUFG
D[4:0]
ENABLE_IBUF
LED_OBUF[2:0]
Switch_IBUF[0:14]
Synthesizer
AUDIO_OBUF_inst
OBUF
AUDIO
ENABLE
ENABLE_IBUF_inst
IBUF
LED_OBUF[0]_inst
OBUF
LED[3:0]
BTNR
BTNR_IBUF_inst
IBUF
ButtonR
BTNR_IBUF
CLK_IBUF_BUFG
LED_OBUF[2:0]
BTN_R
D[4:0]
ButtonDebounce
LED_OBUF[1]_inst
OBUF
CLK
CLK_IBUF_inst
IBUF
CLK_IBUF_BUFG_inst
BUFG
ButtonU
CLK_IBUF_BUFG
LED_OBUF
BTN_U
ButtonDebounce_0
LED_OBUF[2]_inst
OBUF
BTNU
BTNU_IBUF_inst
IBUF
Table_Select_reg[0]
C
CE
D
R
Q
FDRE
Table_Select[0]_i_1
I0
O
LUT1
LED_OBUF[3]_inst
OBUF
Audio_In_Clock
CLK_IBUF_BUFG
RECORDER_CLK_OBUF
Clock_divider__parameterized14
RECORDER_CLK_OBUF_inst
OBUF
RECORDER_CLK
Table_Select_reg[1]
FDRE
Table_Select[1]_i_1
I0
I1
LUT2
M_LRSEL_OBUF_inst
OBUF
M_LRSEL
Table_Select_reg[2]
FDRE
Table_Select[2]_i_1
I0
I1
I2
LUT3
Switch[0:14]
Switch_IBUF[0]_inst
IBUF
Switch_IBUF[1]_inst
IBUF
Switch_IBUF[2]_inst
IBUF
Switch_IBUF[3]_inst
IBUF
Switch_IBUF[4]_inst
IBUF
Switch_IBUF[5]_inst
IBUF
Switch_IBUF[6]_inst
IBUF
Switch_IBUF[7]_inst
IBUF
Switch_IBUF[8]_inst
IBUF
Switch_IBUF[9]_inst
IBUF
Switch_IBUF[10]_inst
IBUF
Switch_IBUF[11]_inst
IBUF
Switch_IBUF[12]_inst
IBUF
Switch_IBUF[13]_inst
IBUF
Switch_IBUF[14]_inst
IBUF