MULTIPLEXED STOPWATCH

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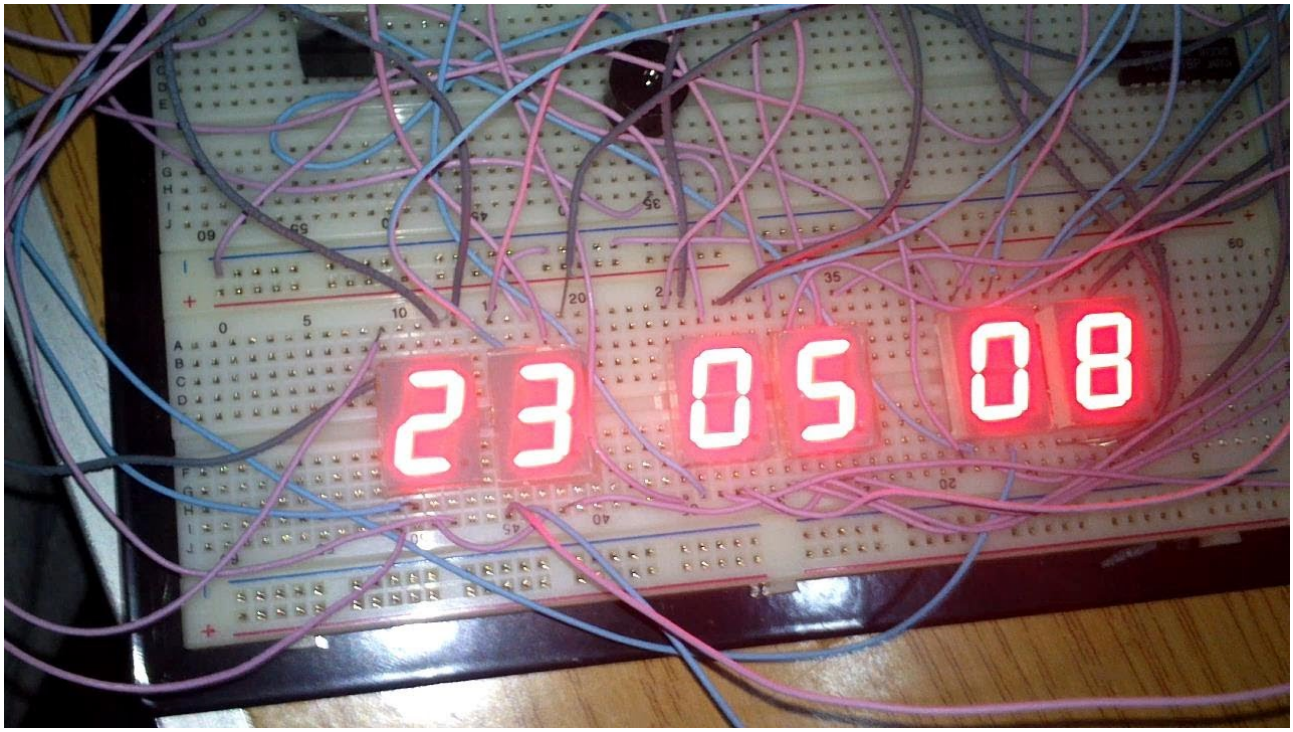
ABSTRACT:

The goal of this mini-project is to get insight view on how complex designs are realized in industry and acquire knowledge about the design process.

In this project, we aimed at implementing a STOPWATCH with the help of FPGA (ZYBO board) and HDL(Verilog).



DESIGN OBJECTIVE:

The time format for our Stopwatch M:SS
(i.e Minutes:Seconds)

For displaying the time, we will use 3 seven segment displays.

As an interface to the user, the stopwatch will include:

- ➔ START/STOP push button : To stop or resume the time.
- ➔ RESET push button: To reset the counter to 0:00.
- ➔ LAP push button: To record the count at different time instants.

When powering up the device the display should show 0.00, where the digits before the decimal points are minutes and after are tens and units of a second.

This means that the maximum count of our stop watch is 9.59 minutes. If the stop watch reaches this value it should wrap and continue counting from zero.

In the initial state the start button starts the stop watch and the current value is displayed on the display whereas the stop button is not supposed to have any function.While the stop watch is running a press of the stop button pauses the stop watch. A press of reset button resets the counter to 0. Pressing the Lap push button records and displays the time at that instant on another set of 3 seven segment displays.

To reduce the number of connections required for each seven segment display, we are planning to multiplex the seven segment displays.

Hoping to hit the bulls eye.....

The block diagram is given below: