

SWL-2480 Datasheet

Marvell 88W8686 WLAN Solution

REV 2

Samsung Electro-Mechanics

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Summary

This datasheet presents the general performance and specifications of SWL-2480 IEEE 802.11b/g Wireless LAN module.

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1 General Description

1.1 Functional Description

SWL-2480 is the IEEE 802.11b/g compliant embedded wireless LAN (WLAN) module for handheld mobile devices.

1.2 Features

- IEEE 802.11b/g standard compliant
- Operating on 2.4GHz Unlicensed ISM band
- Low Power consumption
- Compact size (8.9mm*8.9mm*1.4mm)
- Supported Encryption and Security : WEP, TKIP, AES, and CCMP
- Supported Operating Systems : Linux, WinCE, Windows XP
- Wi-Fi compliant
- RoHS compliant

1.3 Applications

- Consumer electronic devices requiring low power wireless network connectivity
- Handheld devices such as PDA
- Personal computer systems that needs wireless Internet access
- Smart phone/feature phones with embedded WLAN connectivity

1.4 Block Diagram

- SWL-2480 supports SDIO and Generic SPI for host interfaces.
- EEPROM contains MAC address of the device and information such as RF calibration.

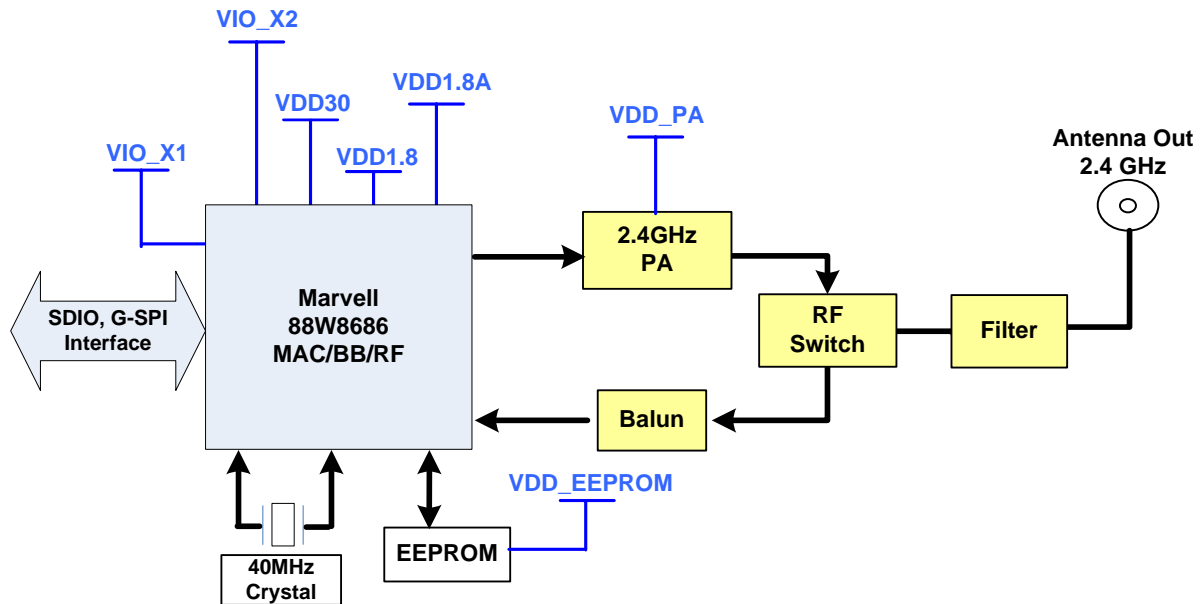


Figure 1-1 SWL-2480 Hardware Block Diagram

2 Dimension and Pin Assignments

2.1 Mechanical Dimension

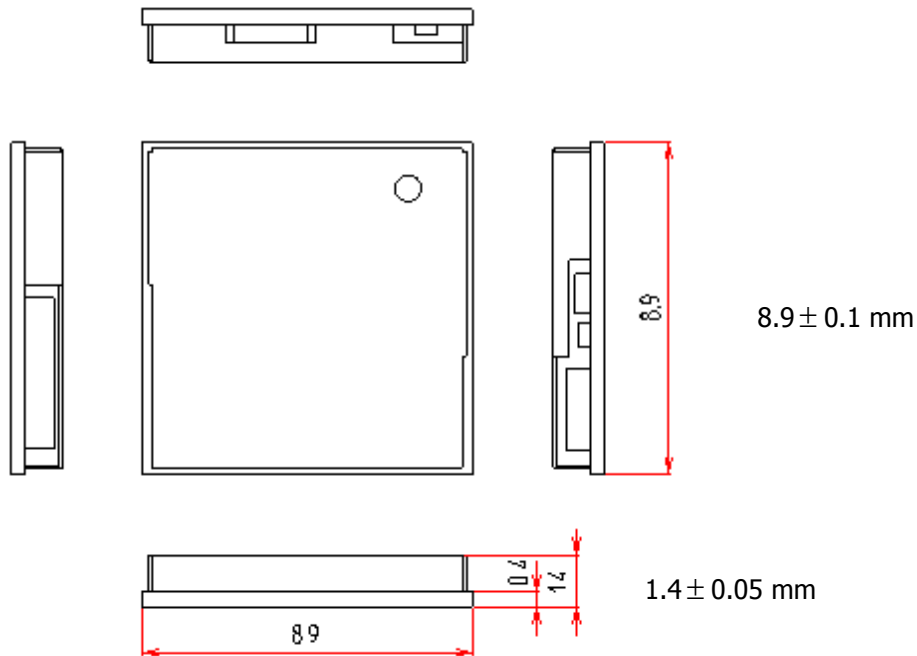


Figure 2-1 SWL-2480 Mechanical Dimension (unit: mm)

2.2 Pad Land Dimension

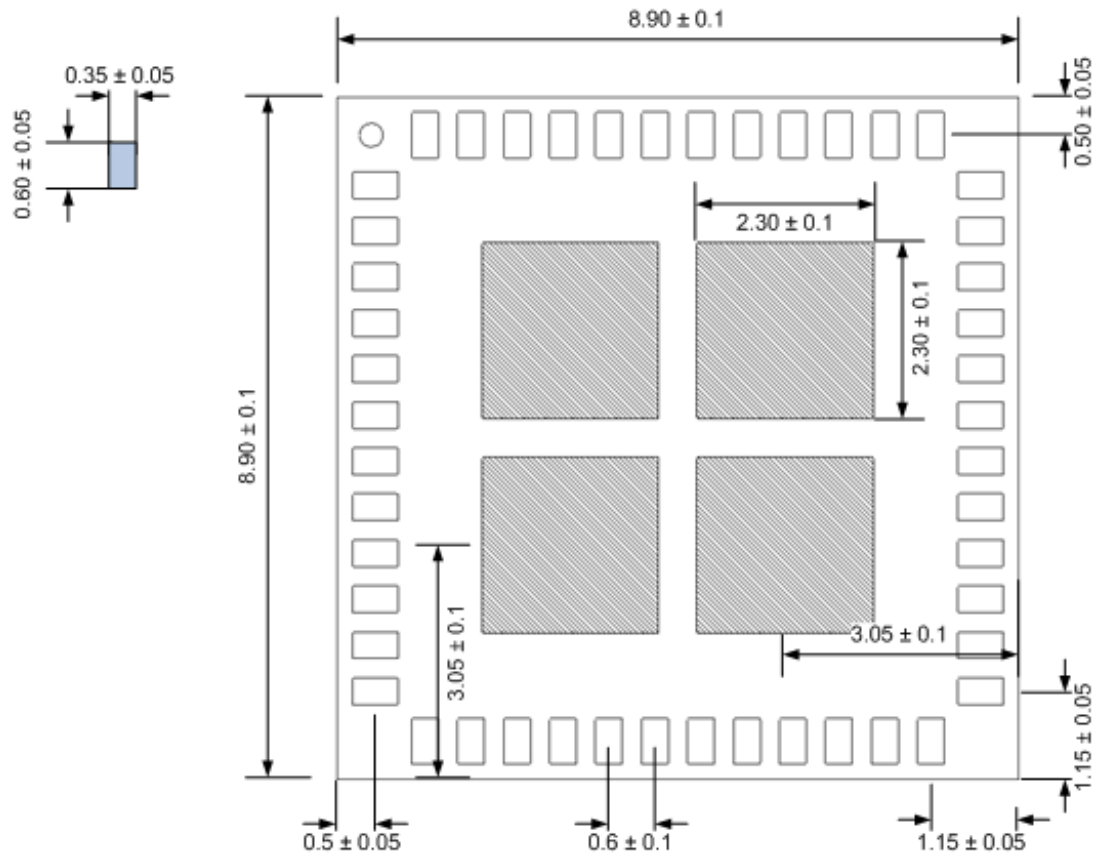


Figure 2-2 Pad Land Dimension (unit: mm)

2.3 Pin Assignments

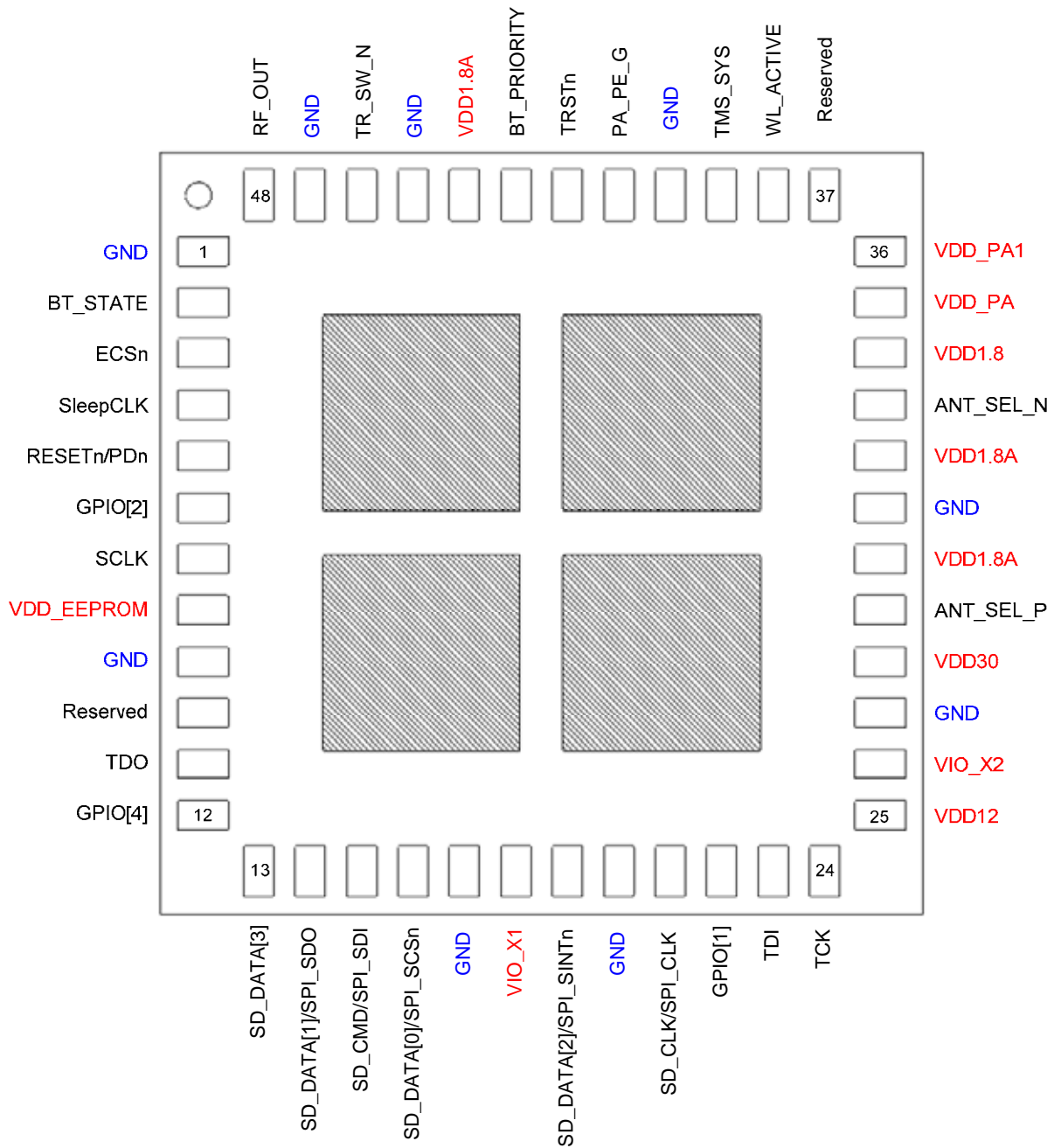


Figure 2-3 Bottom Pad Layout (Top View)

3 Pin Descriptions

NO	SDIO	G-SPI	Type	Description
1	GND	GND	Ground	Ground
2	BT_STATE	BT_STATE	I	Bluetooth State 0 = normal priority, Rx 1 = high priority, Tx Priority is signaled after BT_PRIORITY has been asserted. After priority signaling, BT_STATE indicates the Tx/Rx mode of Bluetooth radio
3	ECSn	ECSn	O	Boot Mode Select Internally Pull-up. With SCLK, can select boot option. Refer to the Table. Boot option
4	SleepCLK	SleepCLK	I	Sleep Clock Mode: Clock Input for External Sleep Clock, If only use external 32.768KHz. Default : using internal clock
5	PDn	PDn	I	Internal Pull-up. Full Power down(Active low) When use it as a purpose of power down, connect to any GPIO pin of host
6	GPIO[2]	GPIO[2]	I/O	JTAG Mode Select Internally Pull-up. Enable : Tied to GND with 100Kohm Disable : Floating
7	SCLK	SCLK	I	Boot Mode Select Internally Pull-up. With ECSn, can select boot option. Refer to the Table. Boot option
8	VDD_EEPROM	VDD_EEPROM	Power	Typical 1.8V/3.3V EEPROM Power Supply Should match with VIO_X2
9	GND	GND	Ground	Ground
10	Reserved	Reserved	-	Reserved
11	TDO	TDO	O	JATG and Test Interface JTAG Mode : JTAG Test Data Output
12	GPIO[4]	GPIO[4]	I/O	General Purpose Input/Output Internal pull-up
13	SD_DATA[3]	NC	I/O	SDIO 4 bit Mode : Data line bit [3] SDIO 1 bit Mode : Reserved SDIO SPI Mode : Card select (Active low)
14	SD_DATA[1]	SPI_SDO	I/O	G-SPI Mode : G-SPI Data Output SDIO 4 bit Mode : Data line bit [1] SDIO 1 bit Mode : Interrupt SDIO SPI Mode : Reserved
15	SD_CMD	SPI_SDI	I/O	G-SPI Mode : G-SPI Data Input SDIO 4 bit Mode : Command/Response SDIO 1 bit Mode : Command Line SDIO SPI Mode : Data Input
16	SD_DATA[0]	SPI_SCSn	I	G-SPI Mode : G-SPI Chip Select Input (Active low) SDIO 4 bit Mode : Data Line Bit [0] SDIO 1 bit Mode : Data Line SDIO SPI Mode : Data Output
17	GND	GND	Ground	Ground

18	VIO_X1	VIO_X1	Power	1.8V/3.3V Host Supply Connect directly to Host supply.
19	SD_DATA[2]	SPI_SINTn	I/O	G-SPI Mode : G-SPI Interrupt Output (Active low) SDIO 4 bit Mode : Data Line Bit [2] or Read Wait(optional) SDIO 1 bit Mode : Read Wait(optional) SDIO SPI Mode : Reserved
20	GND	GND	Ground	Ground
21	SD_CLK	SPI_CLK	I	G-SPI Mode : G-SPI Clock Input SDIO 4 bit Mode : Clock Input SDIO 1 bit Mode : Clock Input SDIO SPI Mode : Clock Input
22	GPIO[1]	GPIO[1]	I/O	LED Output Tx power or Rx ready LED
23	TDI	TDI	I	JATG and Test Interface Internal Pull-up JTAG Mode : JTAG Test Data Input UART Mode : UART SINT Input
24	TCK	TCK	I	JATG and Test Interface Internal Pull-up JTAG Mode : JTAG Test Clock UART Mode : UART CTS Input
25	VDD12	VDD12	Power	1.2V Digital Core Power Supply If Pin #46 (TR_SW_N) is tied with 100Kohm to GND, leave this pin floating. If Pin #46 (TR_SW_N) is floating, connect to external 1.2V Power supply. Tied to the GND with 1uF and 0.1uF capacitor under all conditions
26	VIO_X2	VIO_X2	Power	1.8V/3.3V Digital Power Supply
27	GND	GND	Ground	Ground
28	VDD30	VDD30	Power	3.0V Digital I/O Power Supply
29	ANT_SEL_P	ANT_SEL_P	O	Differential Antenna Select Positive Output
30	VDD1.8A	VDD1.8A	Power	1.8V Analog Power Supply
31	GND	GND	Ground	Ground
32	VDD1.8A	VDD1.8A	Power	1.8V Analog Power Supply
33	ANT_SEL_N	ANT_SEL_N	O	Differential Antenna Select Negative Output Host Interface Selection Internally Pull-up. With Pin #41 (PA_PE_G), can select Host Interface SDIO : Floating G-SPI : Tied to GND with 100Kohm
34	VDD1.8	VDD1.8	Power	1.8V Digital I/O and Internal Voltage Regulator Power Supply
35	VDD_PA	VDD_PA	Power	3.3V Power AMP Power Supply
36	VDD_PA1	VDD_PA1	Power	3.3V First stage amp. Of Power AMP Power Supply
37	Reserved	Reserved	-	Reserved

38	WL_ACTIVE	WL_ACTIVE	O	<p>Bluetooth WLAN Active</p> <p>2-Wire BCA Mode : When high, WLAN is transmitting or Receiving packets</p> <p>3-Wire BCA Mode :</p> <p> 0 = Bluetooth device allowed to transmit</p> <p> 1 = Bluetooth device not allowed to transmit</p> <p>Internal pull-down</p> <p>This pin drives low when PDn is asserted.</p> <p>In WLAN Sleep mode, all I/O pads are powered down.</p> <p>This pad must stay at a low state even in power down mode.</p>
39	TMS_SYS	TMS_SYS	I	<p>JATG and Test Interface</p> <p>Internal Pull-down</p> <p>JTAG Test Mode Select 1</p> <p>This input selects the system JTAG controller</p>
40	GND	GND	Ground	Ground
41	PA_PE_G	PA_PE_G	O	<p>Host Interface Selection</p> <p>Internally Pull-up. With Pin #33 (ANT_SEL_N), can select Host Interface</p> <p>SDIO : Floating</p> <p>G-SPI : Tied to GND with 100Kohm</p>
42	TRSTn	TRSTn	I	<p>JATG and Test Interface</p> <p>Internal Pull-up</p> <p>JTAG Test Mode : JTAG Test Reset (Active low)</p> <p>Functional Mode : External LNA Output</p>
43	BT_PRIORITY	BT_PRIORITY	I	<p>Bluetooth Priority</p> <p>2-Wire BCA Mode : When high, Bluetooth is transmitting or Receiving high priority packets</p> <p>3-Wire BCA Mode : When high, Bluetooth is transmitting or Receiving packets</p>
44	VDD1.8A	VDD1.8A	Power	1.8V Analog Power Supply
45	GND	GND	Ground	Ground
46	TR_SW_N	TR_SW_N	O	<p>1.2V Core Voltage Supply Selection</p> <p>Using Internal Reg. : Tied to GND with 100Kohm</p> <p>Using external Reg. : Floating</p>
47	GND	GND	Ground	Ground
48	RF_INOUT	RF_INOUT	Analog	RF Input/Output

4 Electrical Characteristics

4.1 DC Characteristics

Item	Conditions	Min	Nom.	Max	Unit
Operating Voltage of VDD1.8A		1.7	1.8	1.9	V
Operating Voltage of VIO_X1* ¹	Connect directly to Host supply.	1.62	1.8	1.98	
		2.97	3.3	3.63	
Operating Voltage of VIO_X2		1.62	1.8	1.98	
Operating Voltage of VDD18		1.62	1.8	1.98	
Operating Voltage of VDD30		2.7	3.0	3.3	
Operating Voltage of VDD_PA/PA1		3.05	3.3	3.5	
Operating Voltage of VDD_EEPROM	Comply with VIO_X2	1.62	1.8	1.98	
Operating Voltage of VDD12	If only use ext. Reg.	1.14	1.2	1.32	

Note: *¹ VIO_X1 should match with the host interface signal voltage level.

4.2 Power Consumption

Item			Conditions	Min.	Nom.	Max.	Unit
Power Consumption	Tx (Continuous)	11 Mbps	Continuous Tx @ 16dBm for 11Mbps @ 14dBm for 54Mbps		750	850	mW
		54 Mbps			700	800	mW
	Rx	11 Mbps	Rx sensitivity 11Mbps @-85dBm 54Mbps @-71dBm		280	330	mW
		54 Mbps			305	355	mW
	Deep Sleep				600		uW
	Idle		T/Rx Standby state		280	330	mW

4.3 Environmental Characteristics

Item	Conditions	Min.	Nom.	Max.	Unit
Operating Temperature		-20		70	°C
Storage Temperature		-30		85	°C
Operating Relative Humidity		0		85	% RH

5 RF Specifications

All measurements are made under room temperature 25 °C unless specified.

5.1 Operating Channels

Item	Min	Max	Unit
Center Frequency	2.412	2.472	MHz
Channel	1	13	Channel numbers

Note: Operating frequency range is subject to local regulation.

5.2 Receiver RF Specifications

Item	Conditions	Specification			Unit
		Min	Nom.	Max	
Receiver Minimum Input Level Sensitivity	Data Rate =1 Mbps, PER<8%		-90	-88	dBm
	Data Rate =2 Mbps, PER<8%		-89	-87	
	Data Rate =5.5 Mbps, PER<8%		-88	-86	
	Data Rate =11 Mbps, PER<8%		-84	-82	
	Data Rate =6 Mbps, PER<10%		-87	-85	dBm
	Data Rate =9 Mbps, PER<10%		-86	-84	
	Data Rate =12 Mbps, PER<10%		-84	-82	
	Data Rate =18 Mbps, PER<10%		-83	-81	
	Data Rate =24 Mbps, PER<10%		-79	-77	
	Data Rate =36 Mbps, PER<10%		-76	-74	
	Data Rate =48 Mbps, PER<10%		-72	-70	
	Data Rate =54 Mbps, PER<10%		-70	-68	
Receiver Maximum Input Level	Data Rate =11Mbps, PER<8%	-10			dBm
	Data Rate =54Mbps, PER<10%	-20			dBm

$$PER(\%) = \frac{(\text{the number of all transmitted packets} - \text{the number of received packets})}{\text{the number of all transmitted packets}} \times 100$$

All max values of Rx minimum input level sensitivity meet or exceed IEEE802.11b/g standard specifications.

5.3 Transmitter RF Specifications

Item	Conditions		Specification			Unit
			Min.	Nom.	Max.	
Transmit Power Levels	11b		14.0	16.0	18.0	dBm
	11g		12.0	14.0	16.0	dBm
Transmit Spectrum Mask	11b	fc±11MHz to ±22MHz		-39	-30	dBr
		fc±22MHz or more		-54	-50	dBr
	11g	fc±11MHz		-29	-20	dBr
		fc±20MHz		-37	-28	dBr
		fc±30MHz		-49	-40	dBr
Transmit Center Frequency Tolerance	Temperature=25 °C		-25	-4	+25	ppm
Tx modulation Accuracy	11Mbps		0	15	35	%
	54Mbps			-28	-25	dB
Occupied bandwidth	11b		22			MHz
	11g		16.6			MHz
Transmission Spurious Emission	11b/g	0 ~ 1 GHz			-36	dBm
		1GHz ~ 12.75 GHz			-30	
Adjacent Channel rejection	11Mbps		35			dB
	54Mbps		-1			
Receiver Spurious Emission	11b/g	Less than 1 GHz			-54	dBm
		1GHz or more			-47	

6 Assembly Recommendations

6.1 Printed Circuit Board and Stencil Design

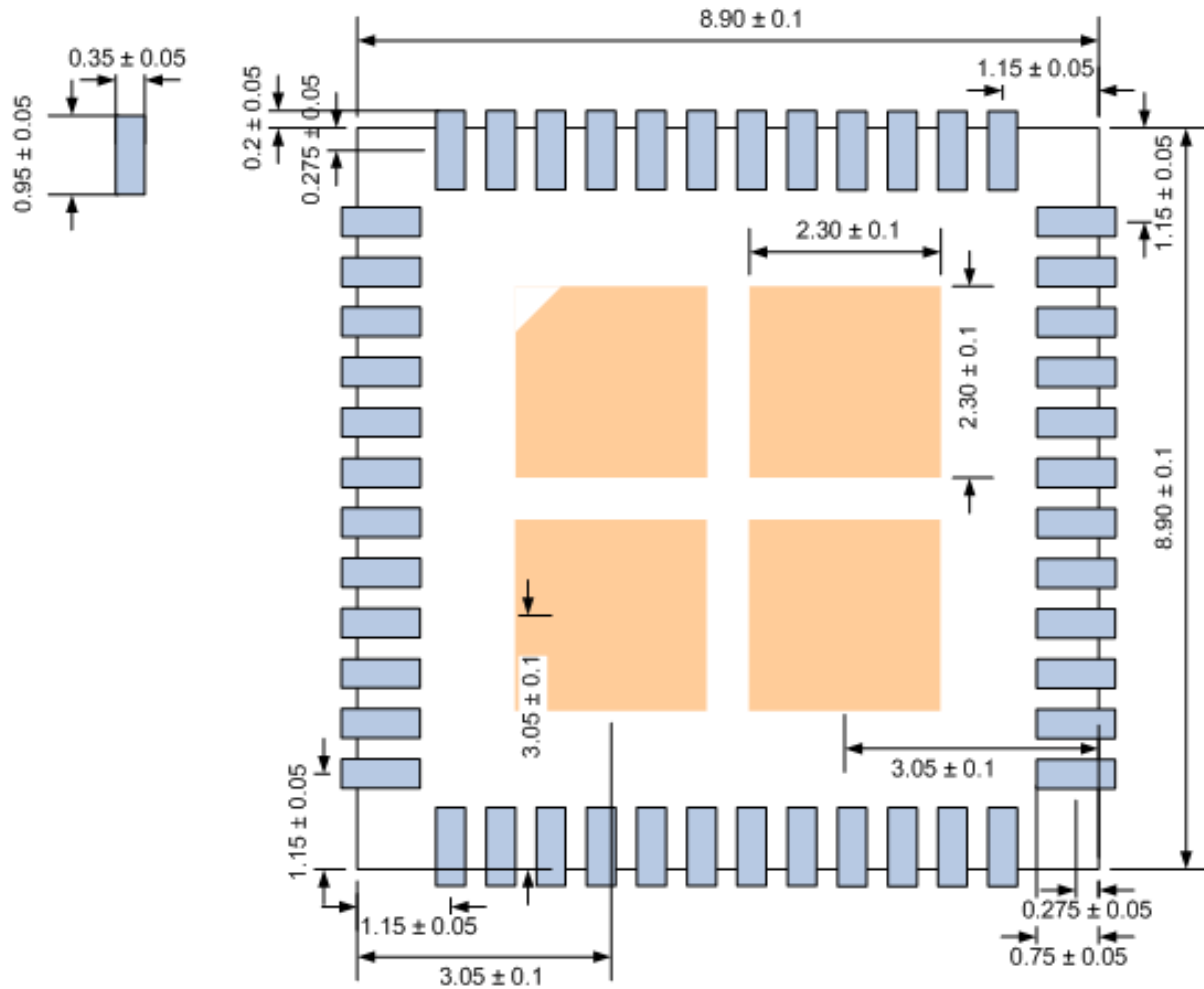
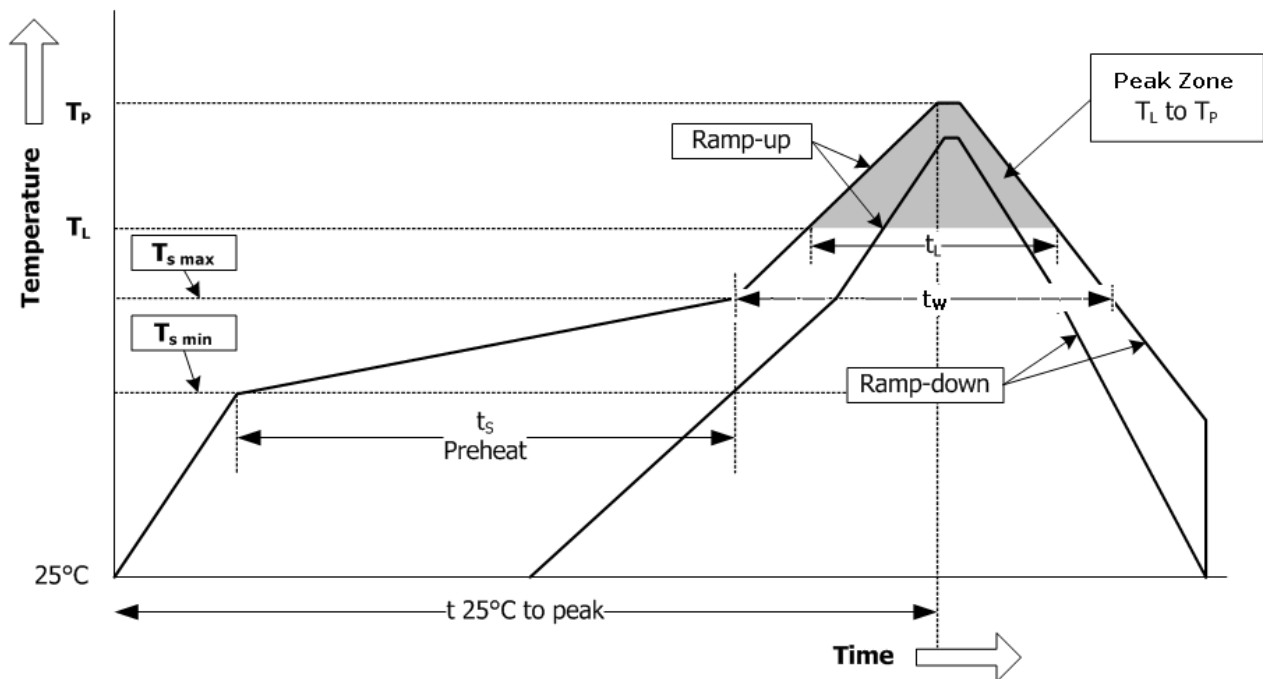


Figure 6-1 Host PCB a Design Recommendations

6.2 Recommended Reflow Profile



T_p : Peak temperature (Measured value, 245 °C)

T_L : 235 °C

$T_{s\ max}$: 217 °C

$T_{s\ min}$: 125 °C

	Temperature Zone			
	25 °C to Peak	Preheat Zone (t_s)	Wetting Zone (t_w)	Peak Zone (t_L)
Temperature range	25~Peak °C	125~217 °C	217~Peak~217 °C	235~Peak~235 °C
Recommend time	240~360 sec	150~210 sec	60~90 sec	10~30 sec
Measured time	321 sec	165 sec	87 sec	41 sec
Remark	Preheat Ramp-up Rate: Less than 1 °C/sec Cooling Ramp-down Rate: Less than 1 °C/sec			

7 Additional Information

7.1 Host Interface Configurations

7.1.1 Host Interface Selection

Pin #33 (ANT_SEL_N) and Pin #41 (PA_PE_G) are used as host interface selection pins.

Pin #33 (ANT_SEL_N)	Pin #41 (PA_PE_G)	Host Interface
Tied to GND with 100Kohm	Tied to GND with 100Kohm	Generic SPI
Tied to GND with 100Kohm	Floating	Reserved
Floating	Tied to GND with 100Kohm	Reserved
Floating	Floating	SDIO

7.1.2 Boot Mode Options

Pin #7 (SCLK) and Pin # 3 (ECSn) are used as boot mode selection pins.

Pin #7 (SCLK)	Pin #3 (ECSn)	Boot from
Tied to GND with 100Kohm	Tied to GND with 100Kohm	UART
Tied to GND with 100Kohm	Floating	Memory test
Floating	Tied to GND with 100Kohm	SPI EEPROM
Floating	Floating	Host Interface

7.1.3 Special Notes for Host Interface Configurations

For **GSPI I/F** selection, use **host Interface boot option**. For **SDIO I/F** selection, however, it is strongly recommended to load a 100kΩ pull-down resistor on pin 33 ANT_SEL_N and use **SPI EEPROM boot option** instead of host interface boot option.

Host Interface	Pin 33 ANT_SEL_N	Pin 41 PA_PE_G	Pin 7 SCLK	Pin 3 ECSn
GSPI	100kΩ pull-down	100kΩ pull-down	Floating	Floating
SDIO	100kΩ pull-down	Floating	Floating	100kΩ pull-down

7.2 Internal or External Source for 1.2V Core Voltage

Pin 46 TR_SW_N strap option is no longer used as internal or external source indicator for 1.2V core voltage. The internal 1.2V LDO is always on regardless of TR_SW_N option. Firmware also does not use TR_SW_N to determine internal LDO state. It is up to the host to call a Firmware API command to turn off the internal LDO when the external power source is supplied to **pin 25 VDD12**.

7.3 RESETn/PDn Control

PDn is tied to RESETn together on SWL-2480. For host control of pin 5 PDn, refer to Marvell application note 88W8686 B1/B2 Power-on Reset Sequence for more detail information. Note that SWL-2480 adopts 88W8686 B1 revision.

7.4 Reliability Test Items, Conditions

Test Item	Condition	Remarks
Normal Temperature Stability Test	24 °C , 4Hr, PCMCIA Interface Jig Type FTP File Size 11b:Get/Put 30Mbyte, Ping 1024byte	
High Temperature Operating Test	80 °C, 48Hr, PCMCIA Interface Jig Type FTP File Size 11b:Get/Put 30Mbyte, Ping 1024byte	
Low Temperature Operating Test	-20 °C, 48Hr, PCMCIA Interface Jig Type FTP File Size 11b:Get/Put 30Mbyte, Ping 1024byte	
High Temperature Storage Test	Max Storage Temperature Spec. 120Hr, Recovery Time 2Hr	
Low Temperature Storage Test	Min Storage Temperature Spec. 120Hr, Recovery Time 2H	
High Temp./Humidity Storage Test	85 °C,85%RH, 120Hr, Recovery Time 4Hr	
Thermal Shock Storage Test	-40 °C (30min) ~ 85 °C (30min), x Cycle , Recovery Time 4Hr	On cycle count, not yet fixed
Pressure Cooker Test	121 °C, 100%RH, 2Kf/ cm^2 , 24Hr, Recovery Time 24Hr	
Vibration Test	Random:20~2000Hz, PSD 0.053g ² /Hz, X,Y,Z 15min/direction Sine wave:10~55Hz, Sweep Time 1min X,Y,Z 2Hr/direction	
Drop Test	Module:152Cm, Steel floor, 12 times, Free Drop Jig:120Cm (12 times), 152Cm (19 times) Total 31 times Free Drop	
ESD Test	HBM Class 1C :100pF, 1500Ω, ~2000V, Contact 5 times	
Soldering Heat Resistance Test	260±5 °C, 10sec (PB Free Special) 3 times	
Packing Vibration Test (Tray & Reel)	5~55Hz, Amplitude:2mm(p-p) X,Y,Z Each Axis/1Hr	
Packing Drop Test (Tray & Reel)	150 cm, 1 Corner, 3 edges, 6 faces 1 time Drop	
Moisture Sensitivity Level	LEVEL 3 (J-STD-020B)	

8 Application Reference Design

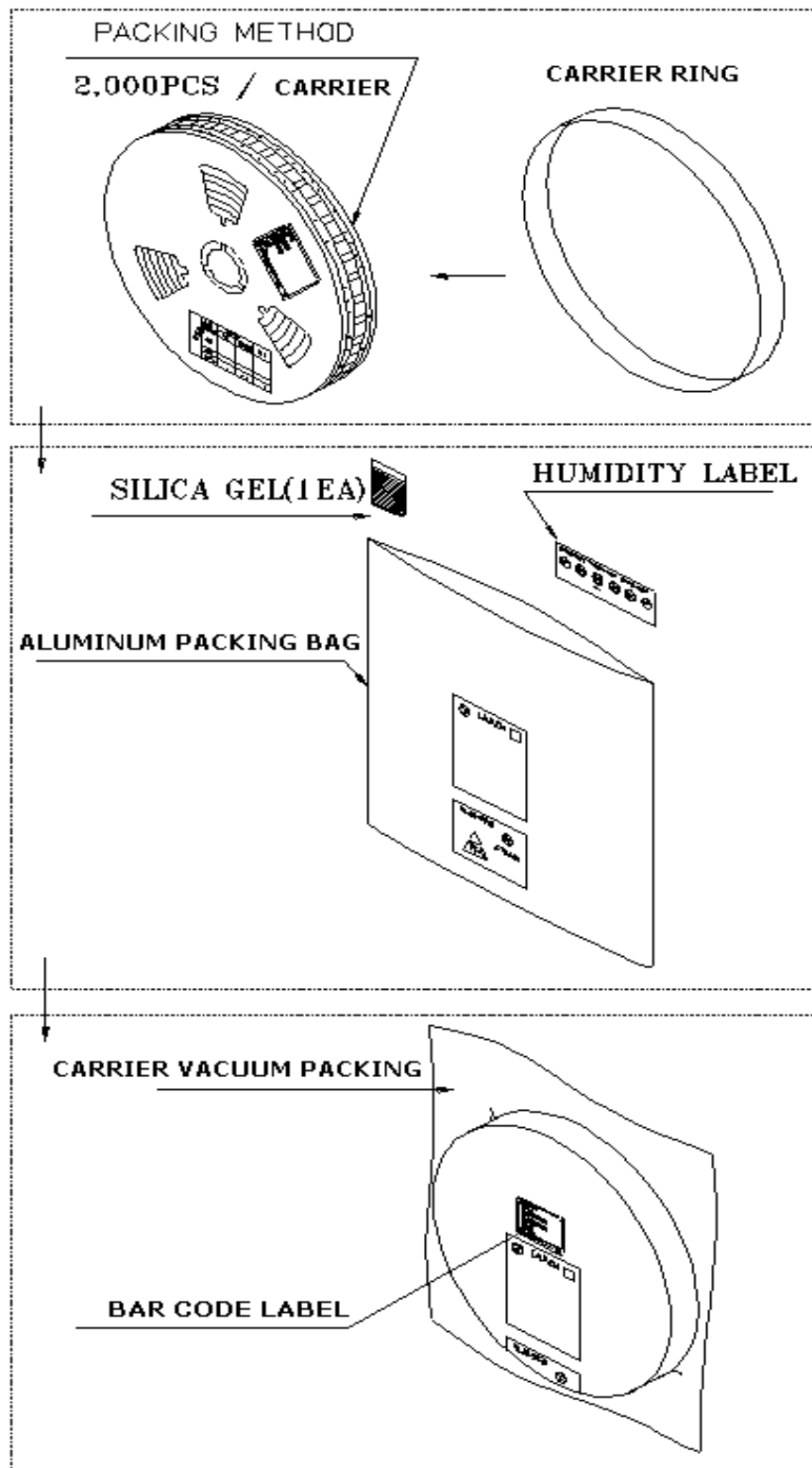
The evaluation board design schematic is provided for application reference design.

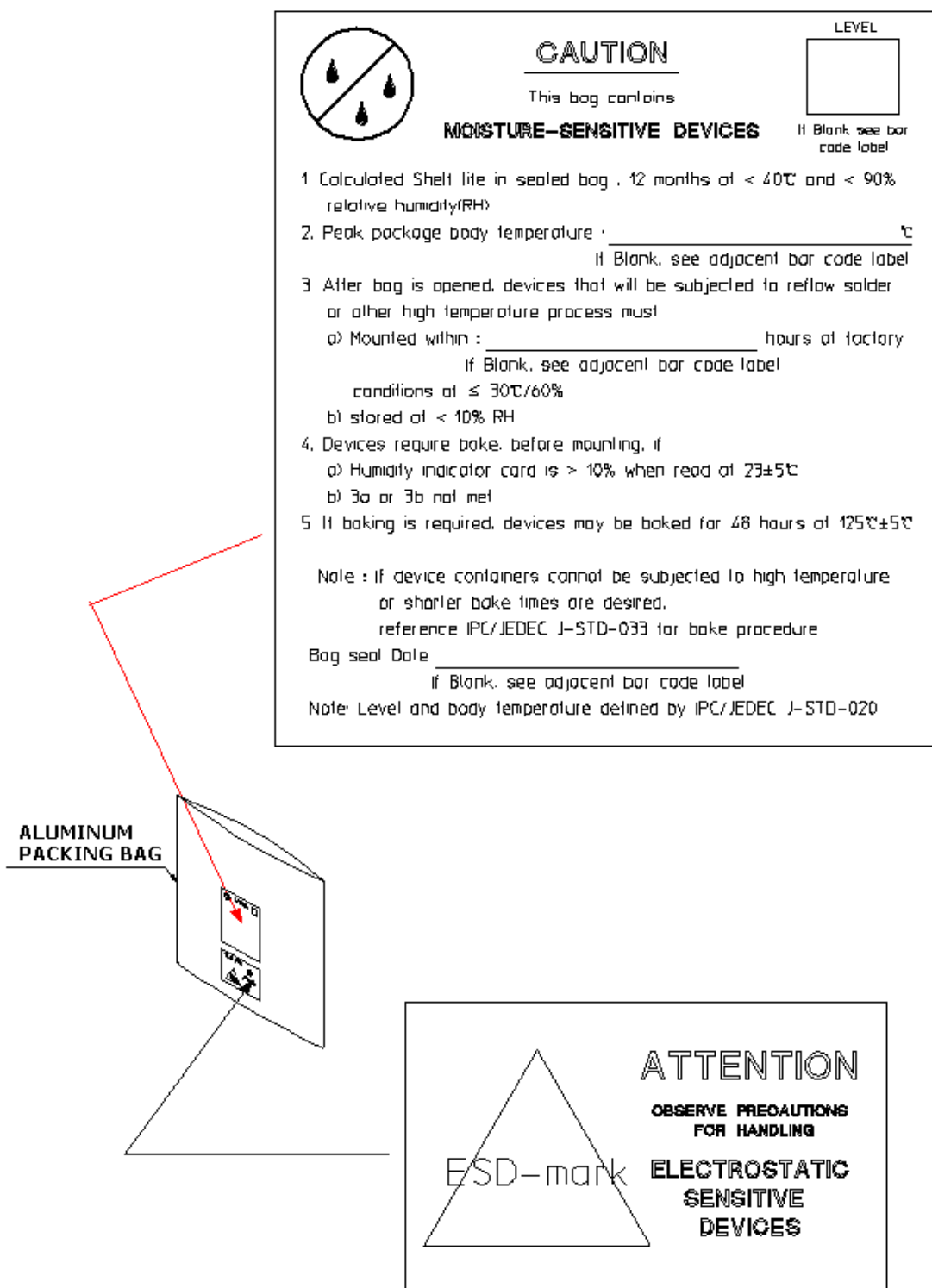
9 Package Information

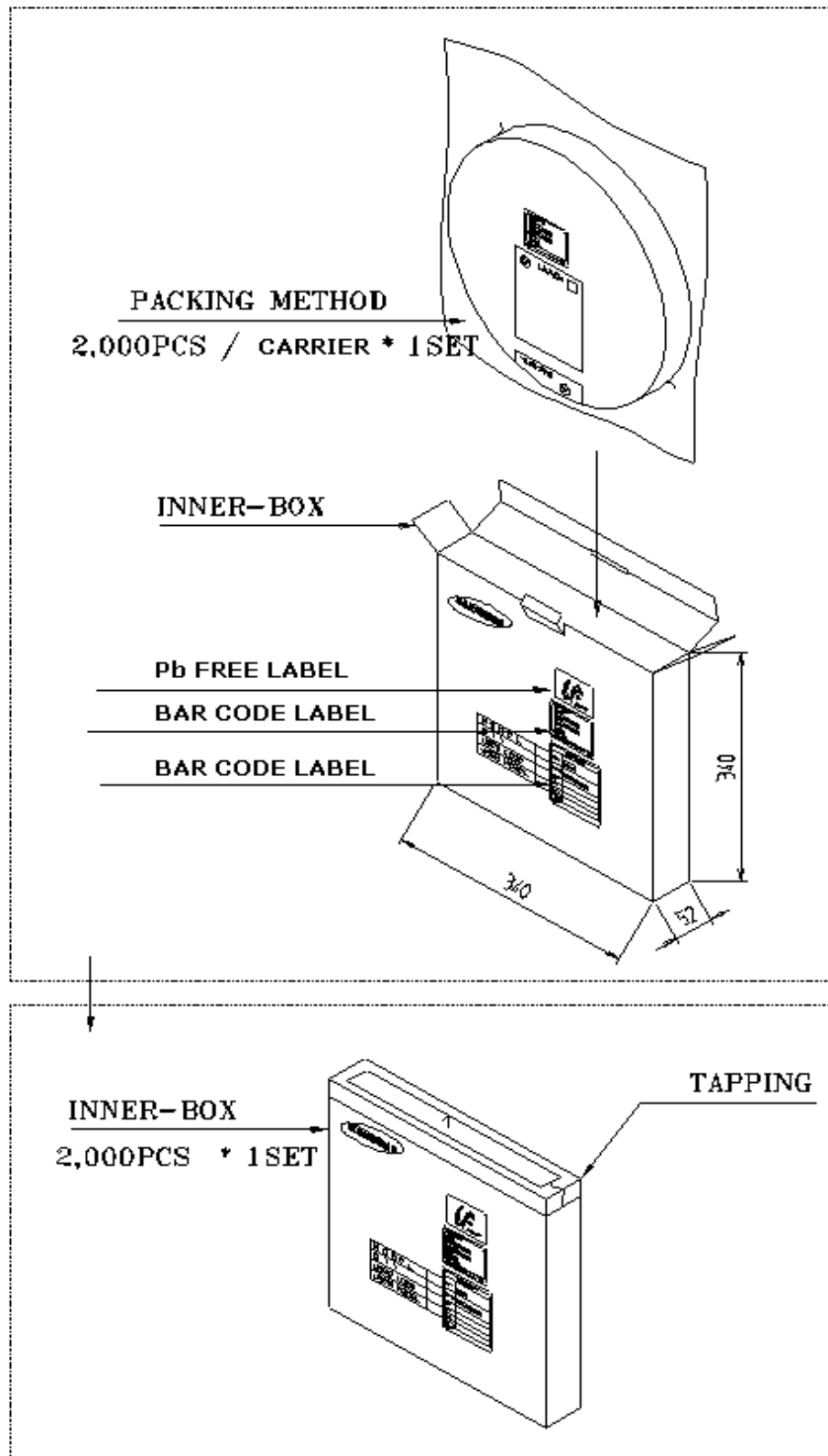
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<p>1 THE TAPE END WILL HAVE A EMPTY POCKET AT THE LEADER AND TRAILER OF CARRIER TAPE.</p> <p>2 THE TAPE END WILL NOT BE STICKED BY GLUE IN ORDER TO MAKE IT EASIER TO PEEL OFF FROM REEL</p> <p>3. THE FEEDING ROUND HOLE WILL BE ON THE RIGHT SIDE AGAINST THE LEADING DIRECTION</p>																																															
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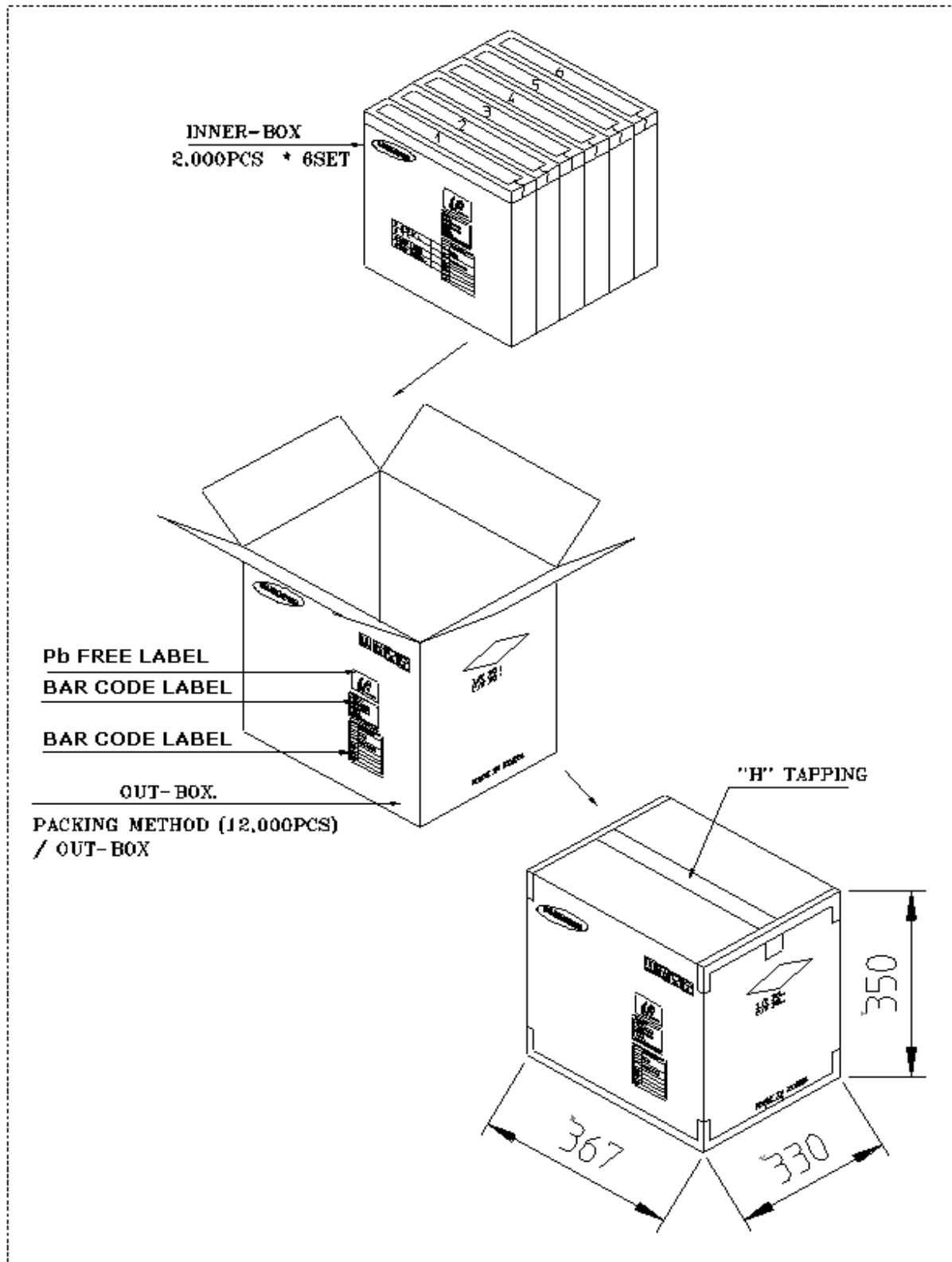
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Revision History

Revision	Date	Descriptions
1	2007-10-22	Created with the new datasheet template.
2	2008-01-16	Figure 2-3 Bottom Pad Layout corrected