正基科技股份有限公司

SPECIFICATION

SPEC. NO.：_____   REV：_____1.2_____

DATE：_____06. 04. 2012_____

PRODUCT   NAME：_____GB86302I_____

	APPROVED	CHECKED	PREPARED	DCC ISSUE
NAME				

AMPAK

GB86302I

WiFi+Bluetooth 4.0(HS)+FM Tx/Rx
SIP Module

Spec Sheet

Revision History

Date	Revision Content	Revised By	Version
2012/03/06	- Initial released	Bart	1.0
2012/03/23	- Initial released WiFi RF Specification	Bart	1.1
2012/06/04	- Modify Chapter 9. Dimensions	Bart	1.2

Contents

1. Introduction

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the WiFi, Bluetooth and FM functionalities. The highly integrated GB86302I module makes the possibilities of web browsing, VoIP, Bluetooth headsets, FM radio functional applications and other applications. With seamless roaming capabilities and advanced security, GB86302I can also interact with different vendors' 802.11a/b/g/n Access Points in the wireless LAN.

The wireless module complies with IEEE 802.11 a/b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11a, 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO (4bit/1bit) / gSPI interface for WiFi, UART / I2S / PCM interface for Bluetooth and UART / I2S / PCM interface for FM.

This compact module is a total solution for a combination of WiFi + BT + FM technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

- 802.11a/b/g/n dual-band radio — non-simultaneous dual-band operation
- Bluetooth V4.0(HS) with integrated Class 1 PA and Low Energy (BLE) support
- Concurrent Bluetooth, FM (RX) RDS/RBDS, and WLAN operation
- Single- and dual-antenna support
    - Simultaneous BT/WLAN receive with single antenna
    - Support for a 2×1 dual receiver system
- WLAN host interface options:
    - SDIO v2.0x (1-bit/4-bit) — up to 50 MHz clock rate
    - gSPI — up to 48 MHz clock rate
- BT host digital interface:
    - UART (up to 4 Mbps)
- FM multiple audio routing options: I2S, PCM, eSCO, A2DP
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives
- Lead Free design which is compliant with ROHS requirements.

A simplified block diagram of the module is depicted in the figure below.
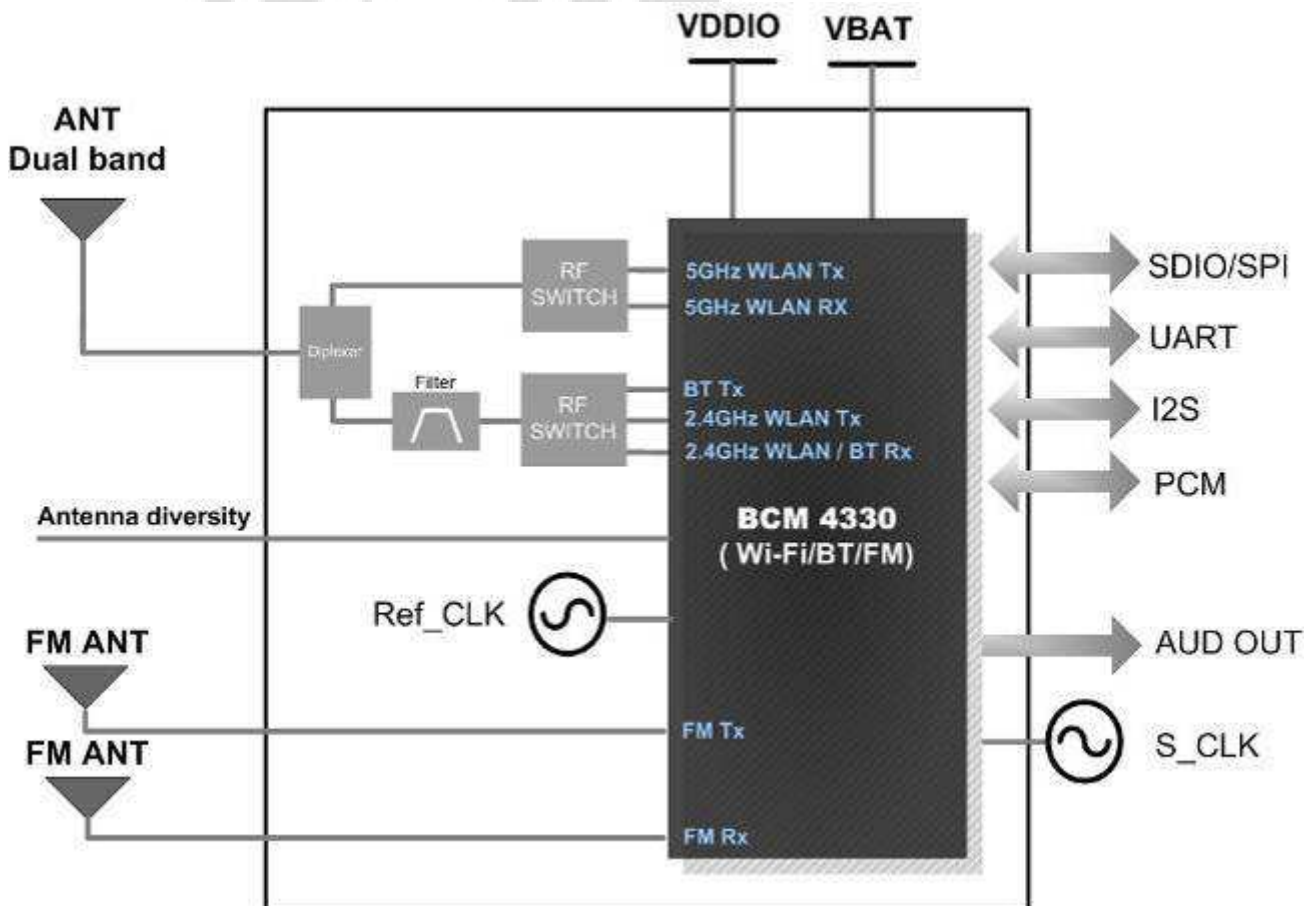
3. Deliverables

3.1 Deliverables

The following products and software will be part of the product.

- Module with packaging
- Evaluation Kits
- Software utility for integration, performance test.
- Product Datasheet.
- Agency certified pre-tested report with the adapter board.

3.2 Regulatory certifications

The product delivery is a pre-tested module, without the module level certification. For module approval, the platform's antennas are required for the certification.

4. General Specification

4.1 General Specification

Model Name	GB86302I
Product Description	Support WiFi/Bluetooth/FM functionalities
Module Pin Connection	65Pin LGA
Dimension	10 mm x 10 mm x 1.5 mm (W*L*T) ±0.1mm
WiFi Interface	SDIOV2.0 (4bit/1bit) / gSPI
BT Interface	UART/ I2S / PCM
FM Interface	UART / I2S / PCM / Audio OUT
Operating temperature	-30℃ to 85℃
Storage temperature	-40℃ to 85℃
Humidity	Operating Humidity 10% to 95%

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	6	V
VDDIO	Digital/Bluetooth/SDIO/SPI I/O Voltage	-0.5	2.98	V

4.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

	Min.	Typ.	Max.	Unit
Operating Temperature	-30	25	85	deg.C
VBAT	3	3.6	4.8	V
VDDIO	1.2	1.8	2.9+/-3%	V

5. WiFi RF Specification

5.1 2.4GHz & 5GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp:25℃

Feature	Description
WLAN Standard	IEEE 802.11a/b/g/n, WiFi compliant
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band) 4.900 GHz ~ 5.845 GHz (5.0 GHz ISM Band)
Number of Channels	2.4GHz：Ch1 ~ Ch14 5.0GHz：Please see the table[1]
Modulation	802.11a : OFDM /64-QAM,16-QAM, QPSK, BPSK 802.11b : DQPSK, DBPSK, CCK 802.11 g/n : OFDM /64-QAM,16-QAM, QPSK, BPSK
Output Power	802.11a /54Mbps : 13 dBm ± 1.5 dB @ EVM ≤ -25dB 802.11b /11Mbps : 16 dBm ± 1.5 dB @ EVM ≤ -9dB 802.11g /54Mbps : 15 dBm ± 1.5 dB @ EVM ≤ -25dB 802.11n /65Mbps : 14 dBm ± 1.5 dB @ EVM ≤ -28dB
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -89 dBm, typical - MCS=1 PER @ -85 dBm, typical - MCS=2 PER @ -84 dBm, typical - MCS=3 PER @ -80 dBm, typical - MCS=4 PER @ -77 dBm, typical - MCS=5 PER @ -75 dBm, typical - MCS=6 PER @ -72 dBm, typical - MCS=7 PER @ -71 dBm, typical
Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -90 dBm, typical - 9Mbps PER @ -88 dBm, typical - 12Mbps PER @ -87 dBm, typical - 18Mbps PER @ -85 dBm, typical - 24Mbps PER @ -83 dBm, typical - 36Mbps PER @ -80 dBm, typical - 48Mbps PER @ -76 dBm, typical - 54Mbps PER @ -74 dBm, typical
Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -96 dBm, typical - 2Mbps PER @ -90 dBm, typical - 5.5Mbps PER @ -88 dBm, typical

	- 11Mbps	PER @ -87 dBm, typical
Receive Sensitivity (11a) @10% PER	- 6Mbps	PER @ -81 dBm, typical
	- 9Mbps	PER @ -80 dBm, typical
	- 12Mbps	PER @ -79 dBm, typical
	- 18Mbps	PER @ -77 dBm, typical
	- 24Mbps	PER @ -76 dBm, typical
	- 36Mbps	PER @ -73 dBm, typical
	- 48Mbps	PER @ -69 dBm, typical
	- 54Mbps	PER @ -68 dBm, typical
Data Rate	802.11a : 6, 9, 12, 18, 24, 36, 48, 54Mbps	
	802.11b : 1, 2, 5.5, 11Mbps	
	802.11g : 6, 9, 12, 18, 24, 36, 48, 54Mbps	
Data Rate (20MHz ,Long GI,800ns)	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps	
Data Rate (20MHz ,short GI,400ns)	802.11n : 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps	
Maximum Input Level	802.11b : -10 dBm	
	802.11a/g/n : -20 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

[1]5GHz Channel table

Band (GHz)	Operating Channel Numbers	Channel center frequencies(MHz)
U-NII lower band (5.15GHz~5.25GHz)	36	5180
	40	5200
	44	5220
	48	5240
U-NII middle band (5.25GHz~5.35GHz)	52	5260
	56	5280
	60	5300
	64	5320
U-NII upper band (5.725GHz~5.825GHz)	149	5745
	153	5765
	157	5785
	161	5805

6. Bluetooth Specification

6.1 Bluetooth Specification

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp:25℃

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V4.0 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2.400 GHz ~ 2483.5 GHz		
Number of Channels	79 channels		
Modulation	FHSS, GFSK, DPSK, DQPSK		
RF Specification			
	Min.	**Typical.**	**Max.**
Output Power (Class-1.5)		10 dBm	
Output Power (Class-2)		2 dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-90 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-91 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-86 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

7. FM Specification

7.1 FM Specification (TBD)

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp:25℃

Feature	Description				
General Specification					
Frequency Band	76MHz-108MHz				
Host Interface	HCI UART, I2S/PCM				
Channel step	50 KHz				
Analog Audio output load	R_L>30$K\Omega$, C_L>20pF				
Characteristics	**Condition**	**MIN**	**TYP**	**MAX**	**UNIT**
Transmitter (FM Tx load = 120nH, Q>30)	Output Power Level				dBuV
	Audio harmonic distortion (fmod=1KHz, △f=75KHz, Pilot △f=6.75KHz)				%
	Audio SNR (△f=22.5KHz, I2S audio in SNR ≧ 57dB) — MONO				dB
	Audio SNR — Stereo				
Receiver (FM Tx Antenna = 120nH, Q>30)	RDS Sensitivity				dBm
	Audio harmonic distortion (Vin=1mV, △f=75KHz) — fmod=1KHz				%
	Audio harmonic distortion — fmod=3KHz				
	Maximum SNR (fmod=1KHz,△f=22.5 KHz, BW=300Hz to 15KHz) — MONO				dB
	Maximum SNR — Stereo				
	RF input power level				dBuV

8. Pin Assignments

8.1 Pin Outline

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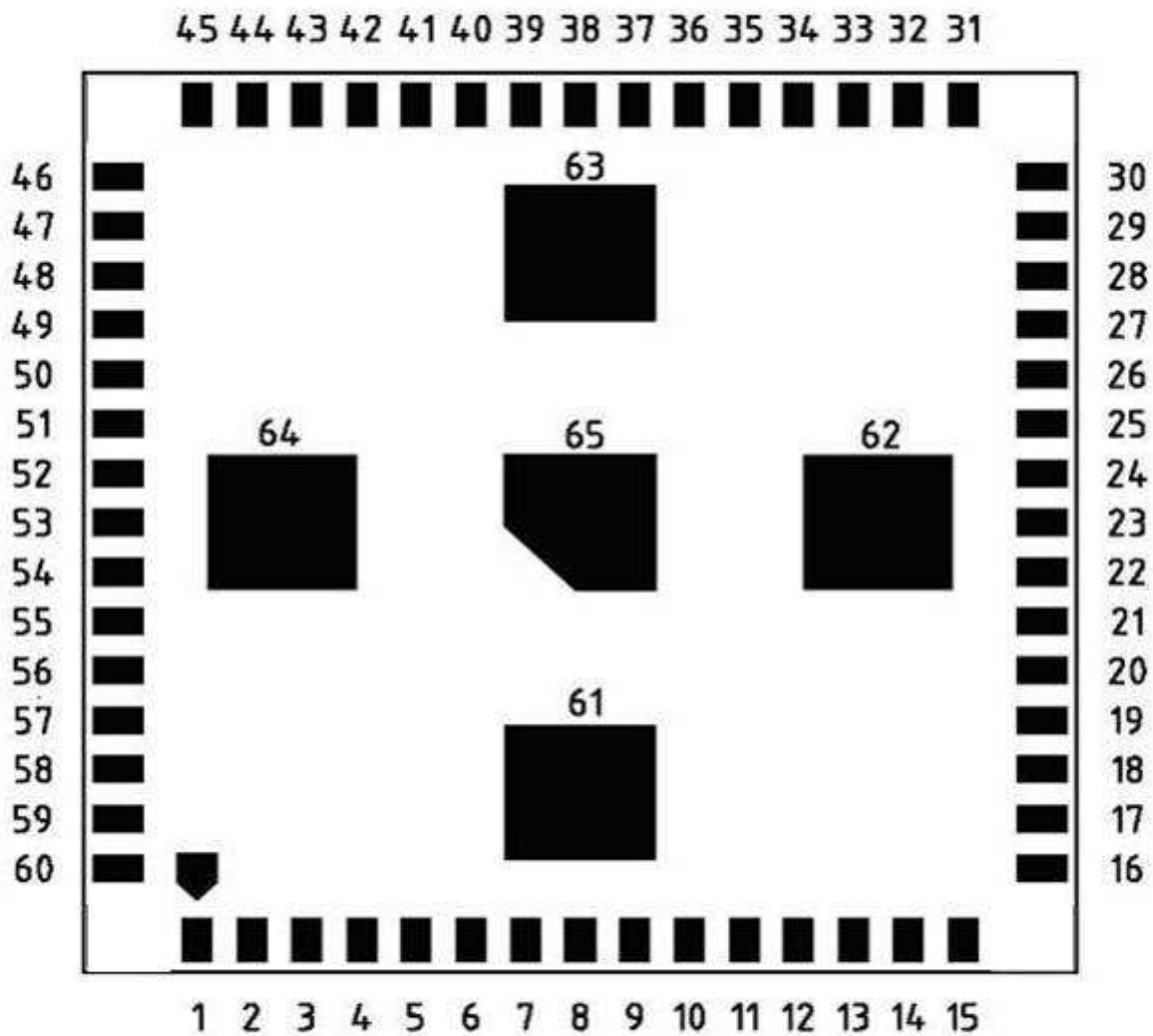
8.2 Pin Definition

NO	Name	Type	Description
1	GND	—	Ground connections
2	ANT	I/O	RF I/O port
3	GND	—	Ground connections

4	BT_RST_N	I	Low asserting reset for Bluetooth core
5	BT_REG_ON	I	Internal regulators power enable/disable
6	BT_HOST_WAKE	O	Bluetooth wake-up output
7	BT_WAKE	I	Bluetooth wake-up input
8	BT_UART_TXD	O	Bluetooth UART interface
9	BT_UART_RXD	I	Bluetooth UART interface
10	BT_UART_RTS_N	O	Bluetooth UART interface
11	BT_UART_CTS_N	I	Bluetooth UART interface
12	I2S_WS	I	I2S word select
13	I2S_CLK	I	I2S clock
14	I2S_DI	I	I2S data input
15	I2S_DO	O	I2S data output
16	NC	—	Floating
17	BT_PCM_CLK	I/O	PCM Clock
18	BT_PCM_IN	I/O	PCM data input
19	BT_PCM_SYNC	I/O	PCM sync signal
20	BT_PCM_OUT	I/O	PCM Data output
21	GND	—	Ground connections
22	VDD_TCXO	I	1.7V to 3.3V supply for the GB86302I TCXO driver. If not used, this pin must be connected to ground
23	TCXO_IN	I	External TCXO input
24	NC	—	Floating
25	NC	—	Floating
26	WL_HOST_WAKE	O	WLAN wake-up output
27	RF_SW_ANT_DIVER_1	O	Antenna diversity control line
28	RF_SW_ANT_DIVER_2	O	Antenna diversity control line
29	NC	—	Floating
30	NC	—	Floating
31	NC	—	Floating
32	VDD_IO	P	Digital/Bluetooth/SDIO/SPI I/O Voltage
33	CLK_REQ_OUT	O	clock request out
34	GND	—	Ground connections
35	NC	—	Floating
36	WL_GPIO_6	I/O	WL_GPIO_6 is select WLAN mode. Pull high for SPI mode, pull low for SDIO mode
37	SDIO_D2	I/O	SDIO data line 2
38	SDIO_DO	I/O	SDIO data line 0
39	SDIO_CLK	I/O	SDIO CLK line

40	SDIO_CMD	I/O	SDIO command line
41	SDIO_D1	I/O	SDIO data line 1
42	SDIO_D3	I/O	SDIO data line 3
43	WL_REG_ON	I	Internal regulators power enable/disable
44	GND	—	Ground connections
45	S_CLK_IN	I	External Low Power Clock input (32.768KHz)
46	VIN_1P2LDO	I	Input supply pin
47	GND	—	Ground connections
48	SR_VLX1	O	Core buck regulator: output to inductor
49	GND	—	Ground connections
50	NC	—	Floating
51	VBAT	P	BUCK regulator: Battery voltage input
52	VBAT	P	BUCK regulator: Battery voltage input
53	NC	—	Floating
54	VOUT_2V5	O	Internal 2.5V LDO output
55	FM_TX	O	FM radio RF output antenna port
56	FM_RX	I	FM radio RF input antenna port
57	GND	—	Ground connections.
58	FM_AUDOUT2	O	FM_AUDIO output
59	FM_AUDOUT1	O	FM_AUDIO output
60	GND	—	Ground connections.
61	GND	—	Ground pad inside Bottom
62	GND	—	Ground pad inside Bottom
63	GND	—	Ground pad inside Bottom
64	GND	—	Ground pad inside Bottom
65	GND	—	Ground pad inside Bottom

9. Dimensions

9.1 Physical Dimensions

(Unit: mm)
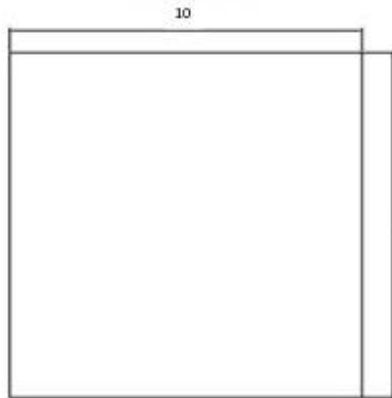
< TOP VIEW >   < Side View >
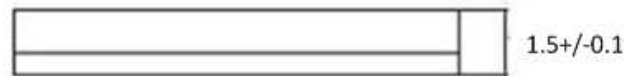
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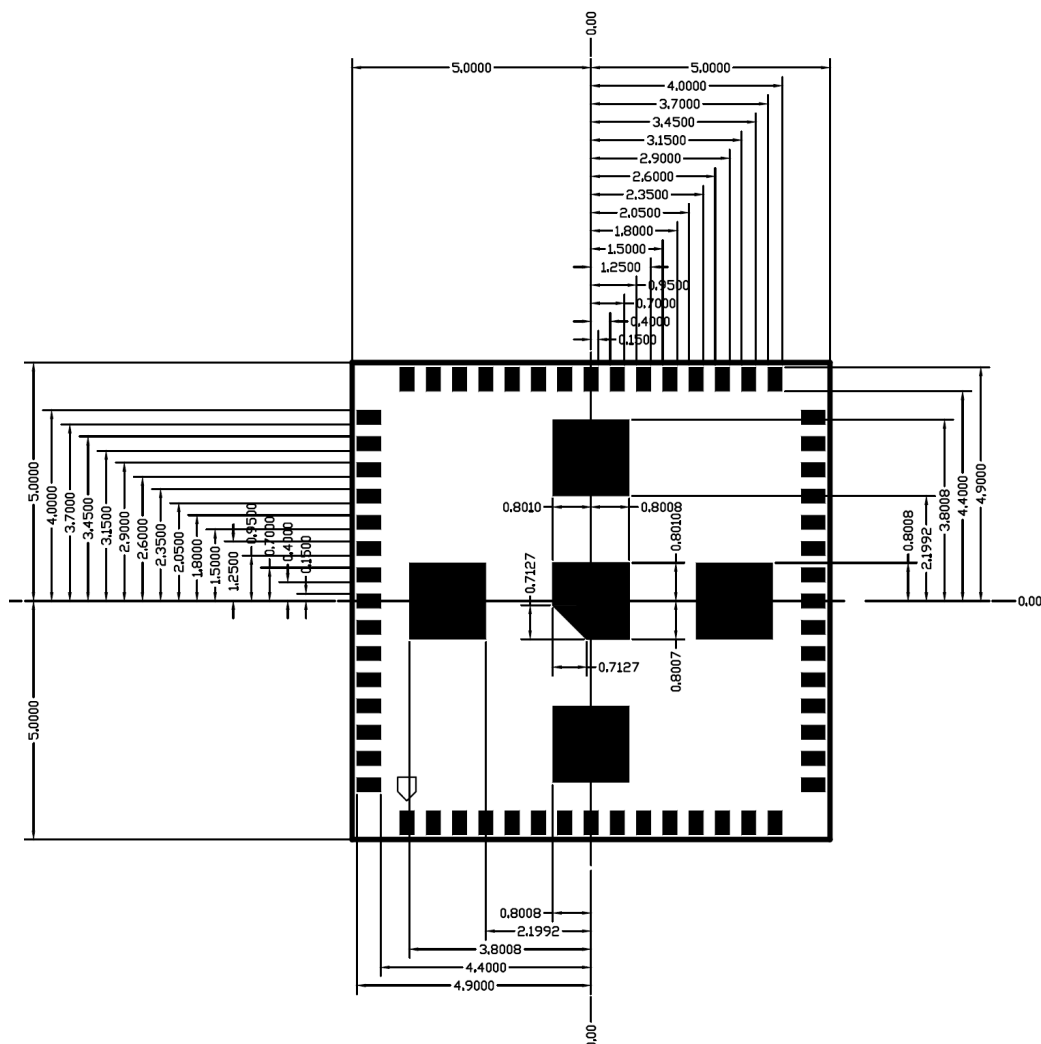
9.2 Layout Recommendation

(Unit: mm)

< TOP VIEW >
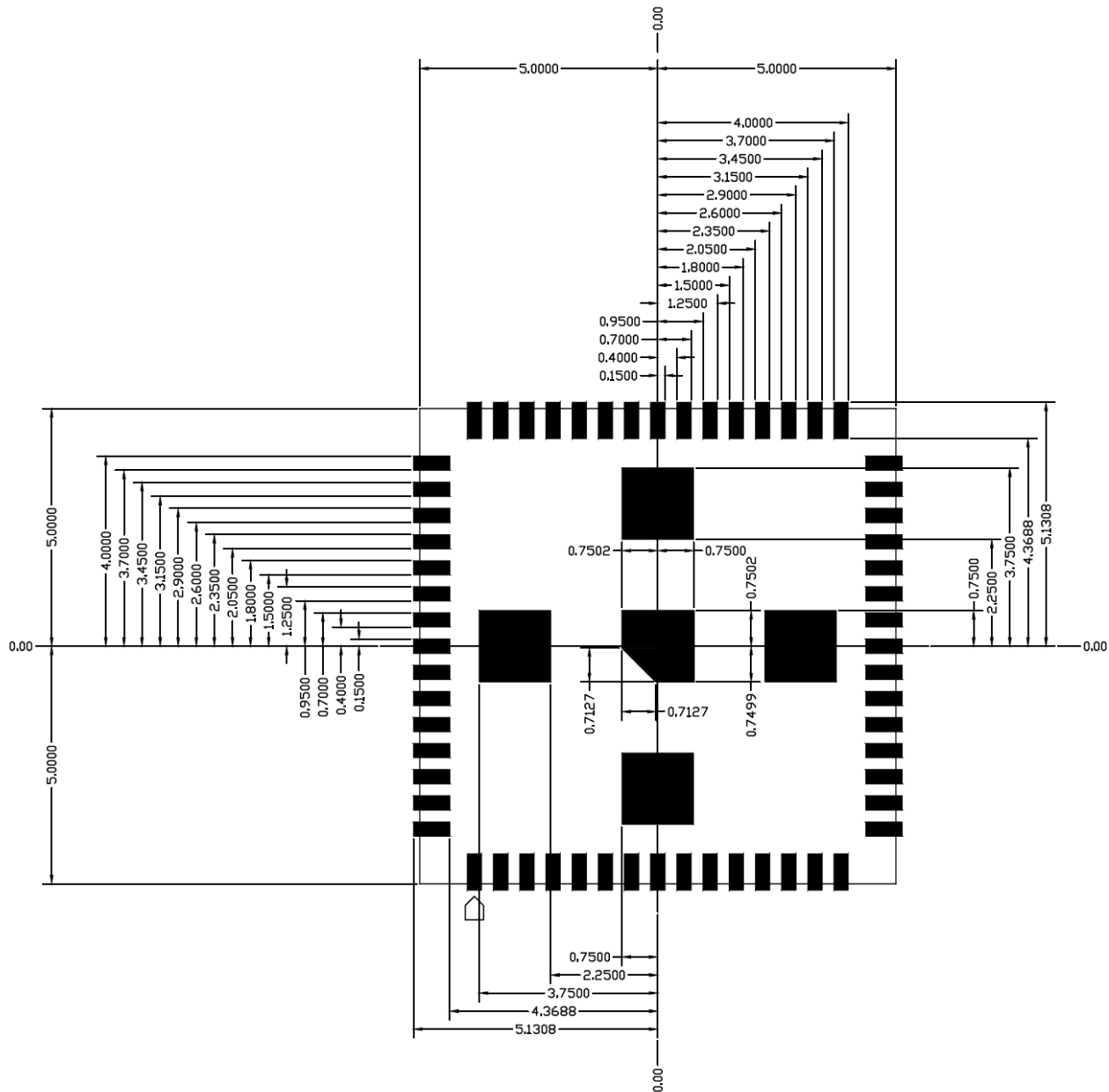
9.3 Form factor
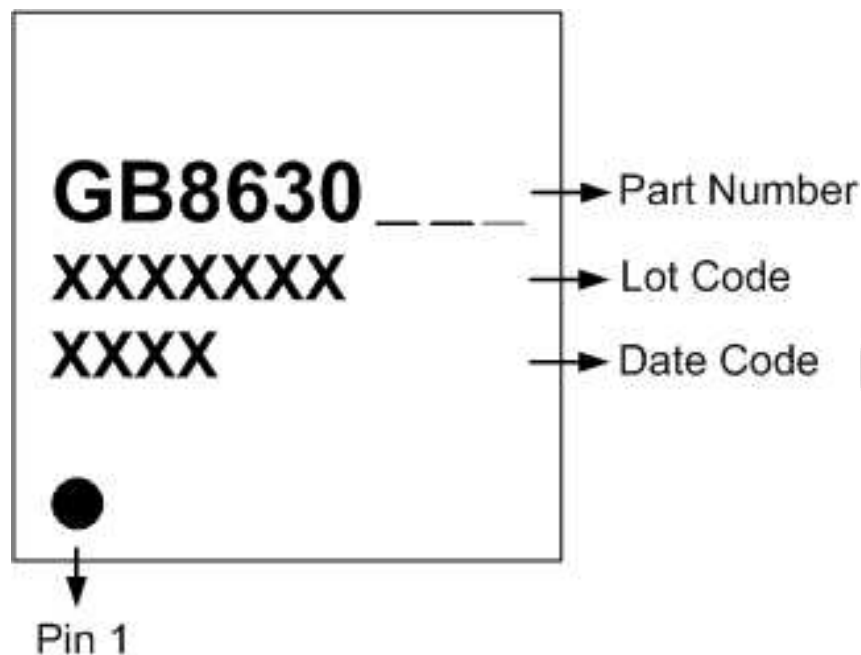
9.4 Part number description:
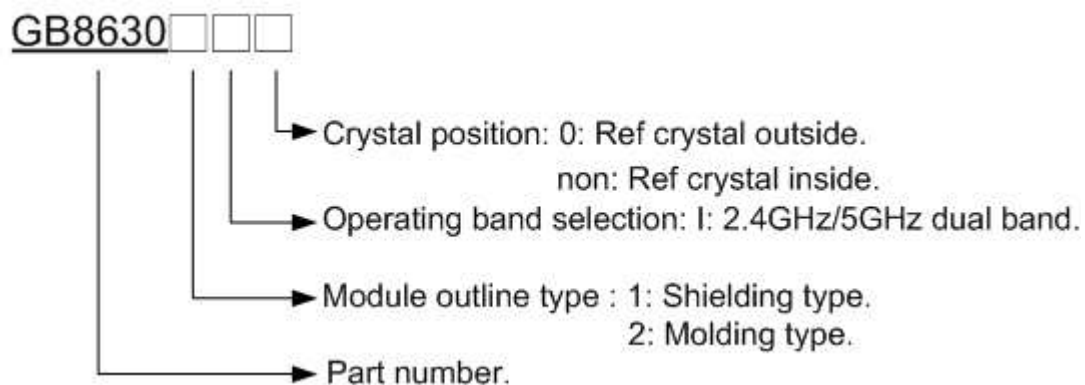
10. External clock reference

External LPO signal characteristics

Parameter	LPO Clock	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	± 200	ppm
Duty cycle	30 - 70	%
Input signal amplitude	200 to 1800	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz

10.1 SDIO Pin Description

The GB86302I supports SDIO version 2.0 for both 1-bit (25 Mbps), 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- ❖ Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- ❖ Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- ❖ Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode		SD 1-Bit Mode		g-SPI Mode	
DATA0	Data Line 0	DATA	Data Line	DO	Data Output
DATA1	Data Line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
DATA2	Data Line 2 or Read Wait	RW	Read Wait	NC	Not Used
DATA3	Data Line 3	NC	Not Used	CS	Card Select
CLK	Clock	CLK	Clock	SCLK	Clock
CMD	Command Line	CMD	Command Line	DI	Data Input

11. Host Interface Timing Diagram

11.1 Power-up Sequence Timing Diagram

The GB86302I has three signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

Note that the WL_REG_ON and BT_REG_ON are ORed in the GB86302I. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (on for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the GB86302I regulators.

- ※ WL_REG_ON: Used by the PMU to power up the WLAN section. It is also OR-gated with the BT_REG_ON input to control the internal GB86302I regulators. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset. A "warm" WLAN reset can be initiated by driving WL_REG_ON low for at least 10 microseconds. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.

- ※ BT_REG_ON: Used by the PMU (OR-gated with WL_REG_ON) to power up the internal GB86302I regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators are disabled.

- ※ BT_RST_N: Low asserting reset for Bluetooth and FM only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).
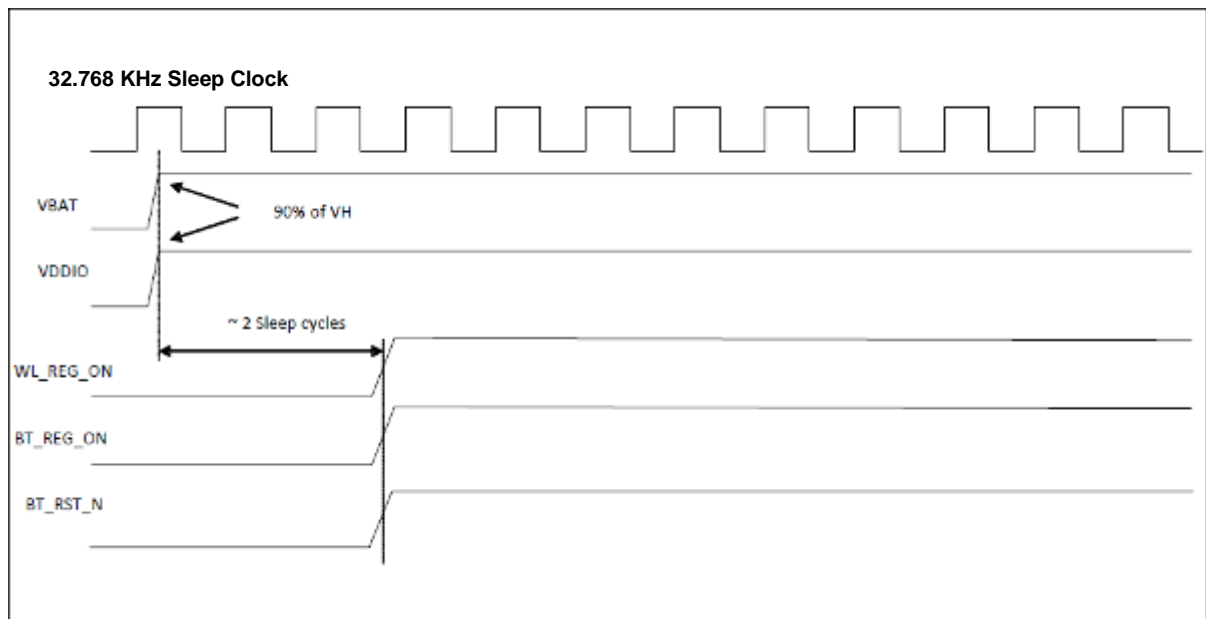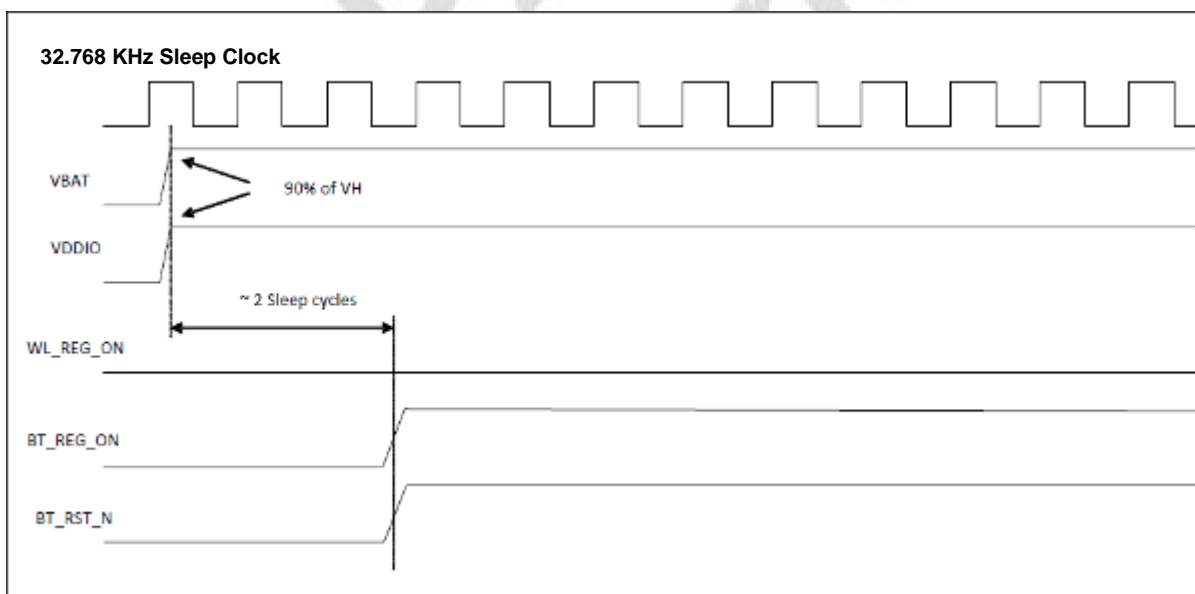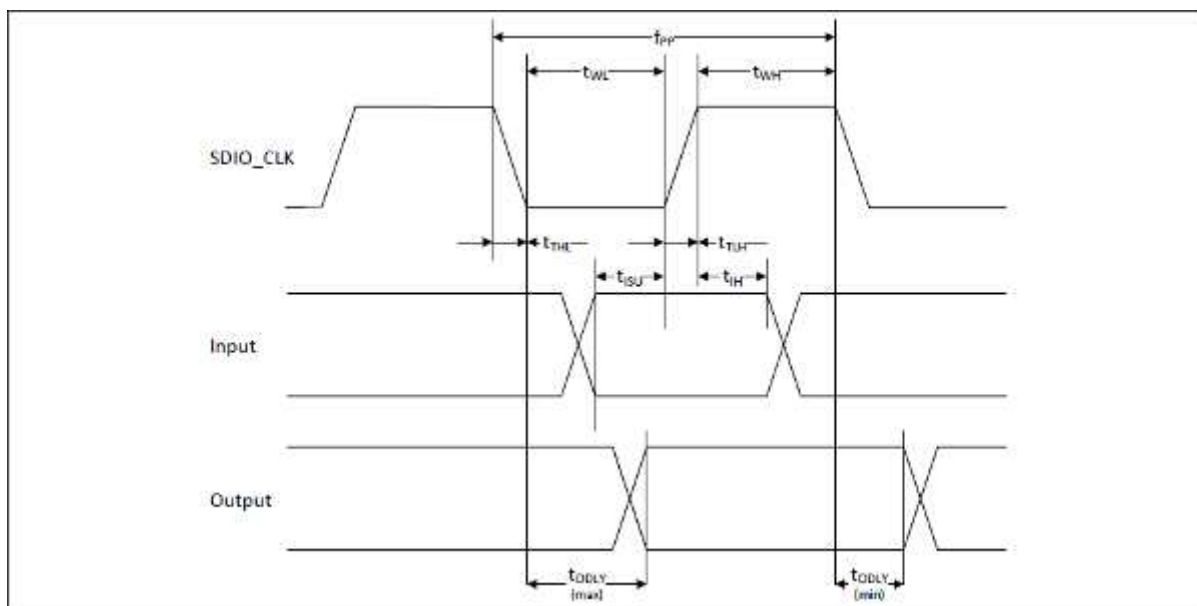
WLAN=ON, Bluetooth=ON
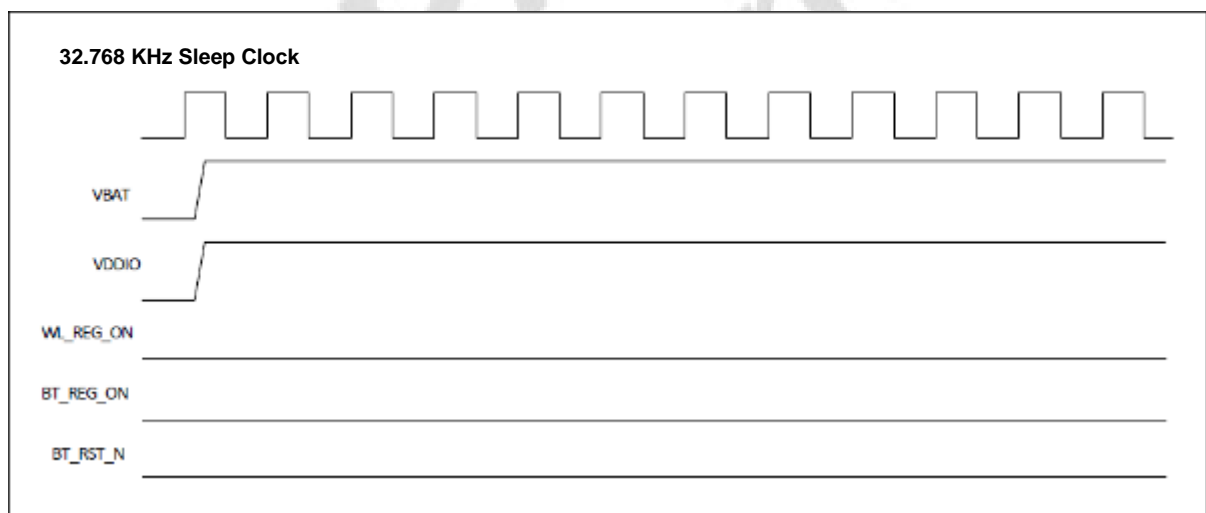
WLAN=OFF, Bluetooth=OFF
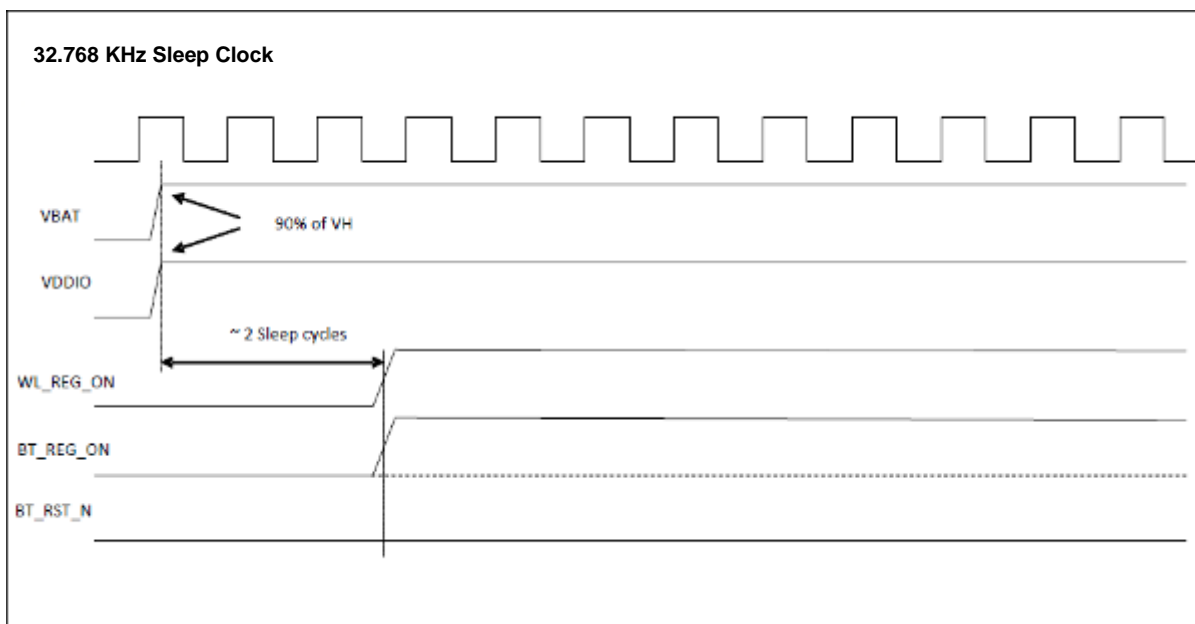
WLAN=ON, Bluetooth=OFF

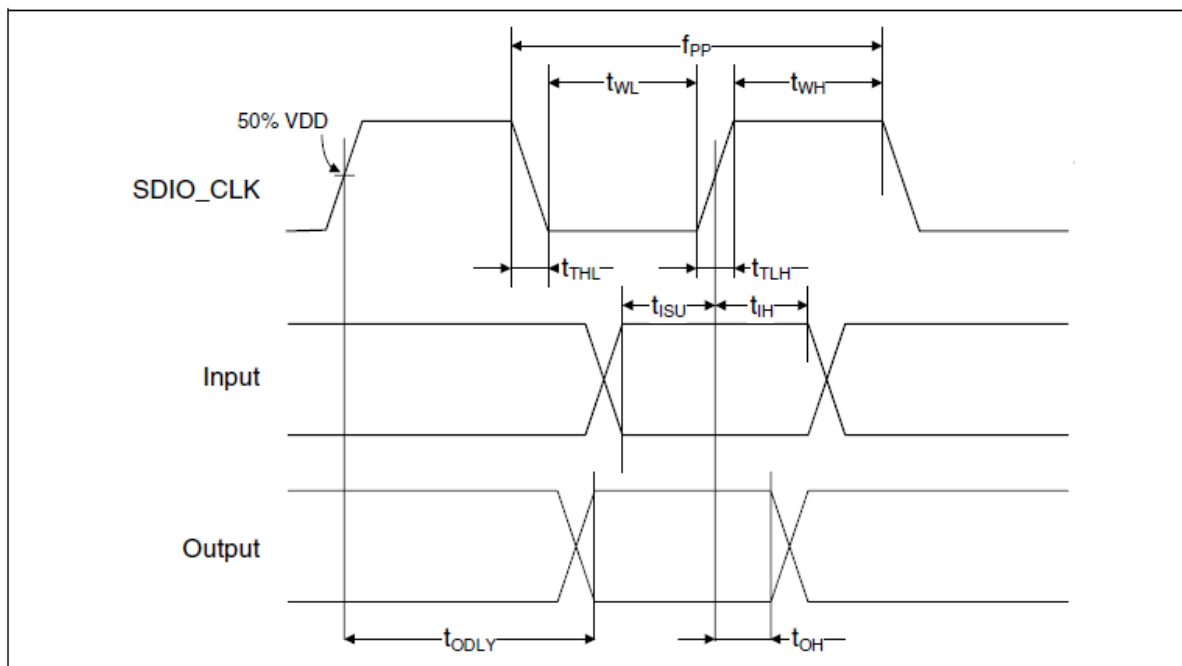WLAN=OFF, Bluetooth=ON

11.2 SDIO Default Mode Timing Diagram

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

11.3 SDIO High Speed Mode Timing Diagram

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL^b)					
Frequency-Data Transfer mode	fPP	0	-	50	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.

b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

12. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250℃

Number of Times : ≤2 times
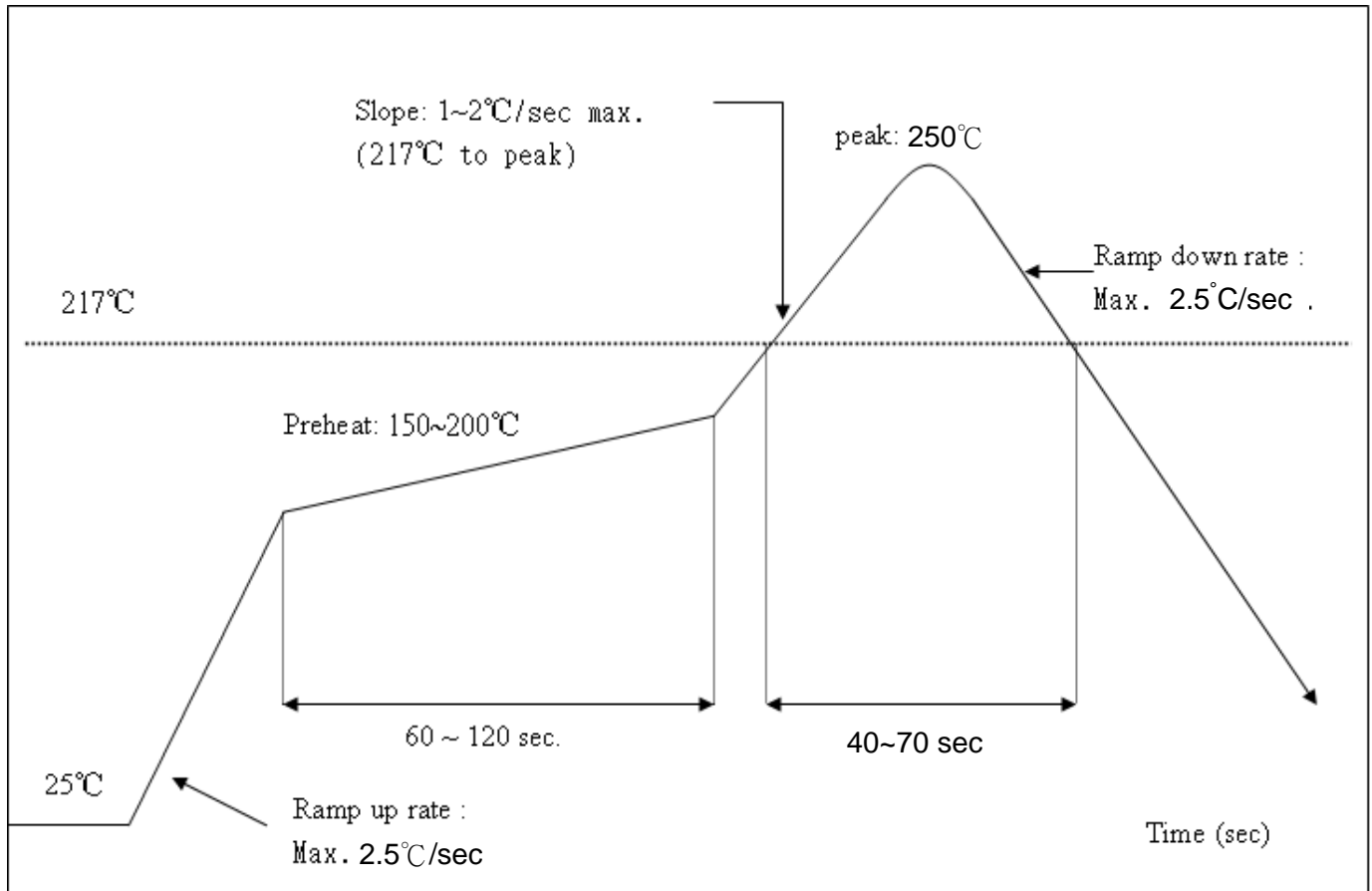
13. Package Information

13.1 Label

Label A ➝ Anti-static and humidity notice
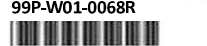
Label B ➝ MSL caution / Storage condition

Label C ➝ Inner box label

Model:	GB86302I
P/N :	99P-W01-0068R
Qty :	1500
Date Code :	1205
Lot Code :	T0B8022

Label D ➝ Carton box label

AMPAK Technology

PO No.	KL94106
Part No.	99P-W01-0068R
Quantity	7500
Lot.No	0000
Manufacture	2003/10/21

13.2 Dimension

1.75±0.10   2.00±0.10   4.00±0.10   16.00±0.10 $\varnothing 1.50^{+0.1}_{-0}$
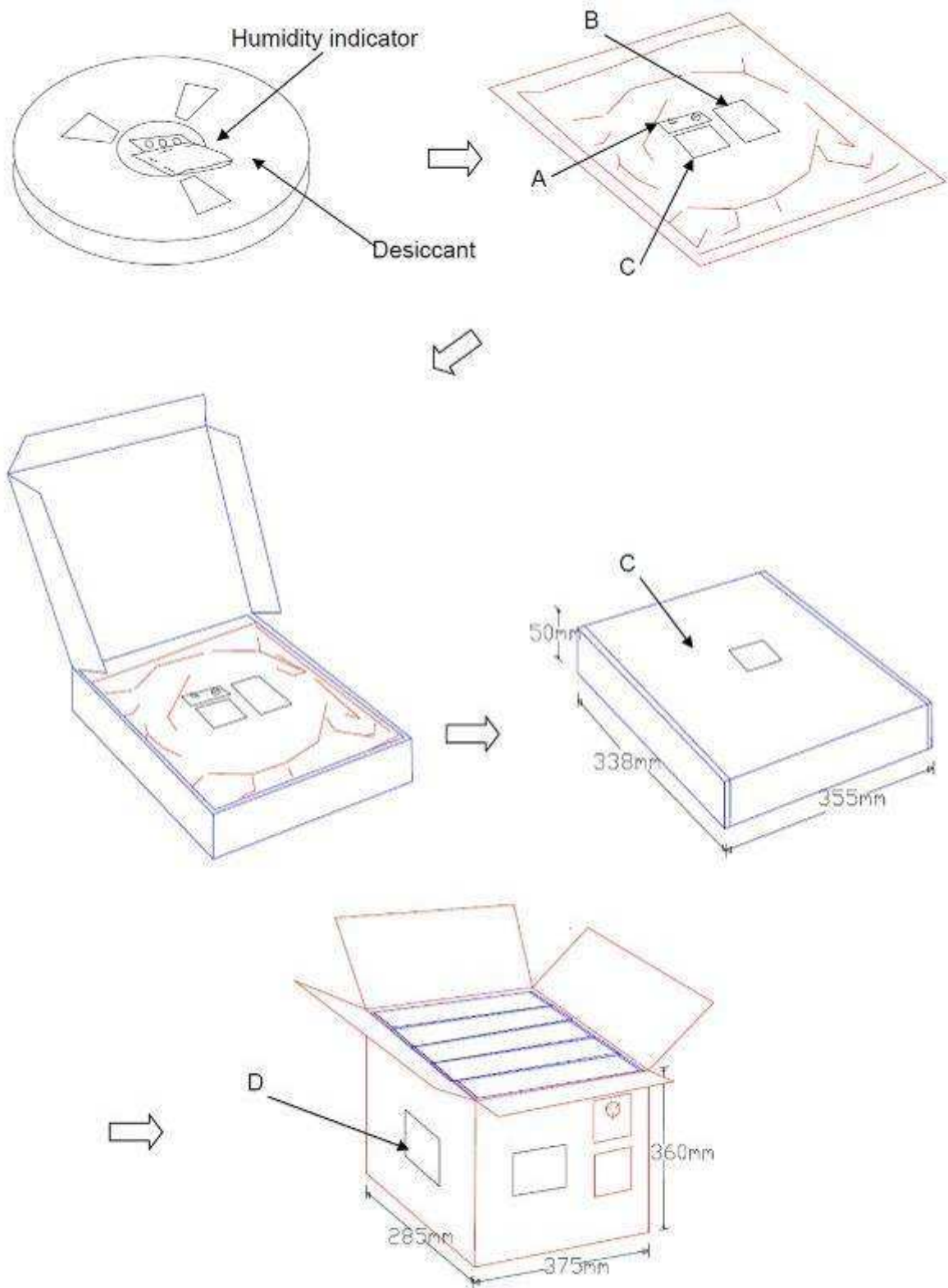
24.00±0.30

11.50±0.10

10.3

10.3

1.7

$\varnothing 1.50$ MIN

1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Component load per 13" reel : 1500 pcs.

Unit:mm

"A"

330.0
REF

100.0
REF
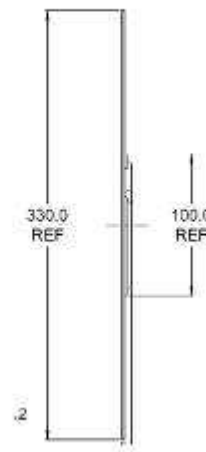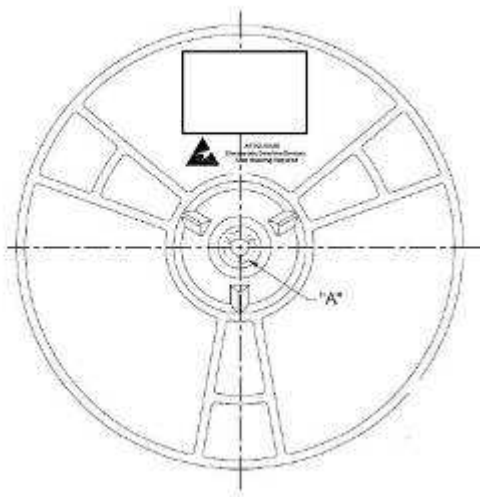
13.3 MSL Level / Storage Condition

LEVEL
4

Caution
This bag contains
MOISTURE-SENSITIVE DEVICES
Do not open except under controlled conditions

1. Calculated shelf life in sealed bag: 12 months at< 40℃ and
   < 90% relative humidity(RH)

2. Peak package body temperature:

225℃	240℃	250℃	260℃
☐	☐	☑	☐

3. After bag is opened, devices that will be subjected to reflow
   solder or other high temperature process must
   a) Mounted within: 48 hours of factory conditions
      <30℃/60% RH, OR
   b) Stored at <10% RH

4. Devices require bake, before mounting, if:
   a)Humidity Indicator Card is>10%when read at 23±5℃
   b)3a or 3b not met

5. If baking is required, devices may be baked for 24 hours
   at 125±5℃

   Note : If device containers cannot be subjected to high
   temperature or shorter bake times are desired,
   reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: _____ **See-SEAL DATELABEL** _____

Note:Level and body temperature defined by IPC/JEDED J-STD-020

※NOTE : Accumulated baking time should not exceed 96hrs