The due date is usually Mondays but since this is getting posted late, please just try to get it in sometime next week. By Valentines Day if you can so I can read over the weekend.

Please update your report so that it includes:

- Information on the complete adder
- An explanation of the computer we built in class including the instruction set and program.

LTspice - [Computer.asc]

File   Edit   Hierarchy   View   Simulate   Tools   Window   Help

Computer.asc   Computer.raw   ComputerForClass.asc   DataMem.asc -- Instance: X6   TestDMz.asc   TestDMz.raw

X2 PC Addr[2:0]   Sel[2:0]   X1 Sel[2:0]   Instruction Memory SRAM   INSTR[7:0]   INSTR[7:0]

.ic V(Clk)=5V V(x)=5

X11 Bufi   Bufo   Clk

x

V2

.ic V(Clk)=5V V(x)=5
.tran 7m
.inc ModelSp2025.txt

PULSE(0 5 0.5m 1n 1n 0.5m 1m)

Formats:
ADD, SUB: Dest=A+B, Dest=A-B
  2-bits | 2-bits | 2-bits | 2-bits
  instr[7:6] | instr[5:4] | instr[3:2] | instr[1:0]
  op-code | Destination | A | B
LOAD, STORE: Register put into or read from DataMem addr
  2-bits | 3-bits | 1-bit | 2-bits
  instr[7:6] | instr[5:3] | instr[2] | instr[1:0]
  op-code | DataMem Address | Not used | Register

Op-codes:
ADD: 00
SUB: 01
STORE: 10
LOAD: 11

X6 Data Memory
Clk   Clk
B[3:0]   Data[3:0]
INSTR[4:3]   SelOut[1:0]   Out[3:0]   DataO[3:0]
WMem   We
WrAdd[1:0]

-3 DM0
5 DM1
1 DM2
0 DM3

X5 MUX4
A[3:0]
B[3:0]   Out[3:0]   WDataReg[3:0]
Sel

X3 Register File
Clk   Clk
D[3:0]
INSTR[3:2]   SelA[1:0]   A[3:0]   A[3:0]
INSTR[1:0]   SelB[1:0]   B[3:0]   B[3:0]
WReg   We
INSTR[5:4]   WrAdd[1:0]

INSTR[6]

X4 ALU
A[3:0]
Add0Sub1   Sum[3:0]   Sum[3:0]
B[3:0]

Sum[3:0]
INSTR[7]

X7
INSTR[7]   X9   A   A
INSTR[6]   A   A   NA   B   NAND   WReg   X8   A   NA   WMem

Program:
LOAD R0 0   --> 11 000 X 00 --> 0xC0
LOAD R1 1   --> 11 001 X 01 --> 0xC9
LOAD R2 2   --> 11 010 X 10 --> 0xD2
ADD R3 R0 R1 --> 00 10 00 01 --> 0x21
SUB R3 R3 R2 --> 01 11 11 10 --> 0x7E
STORE R3 1   --> 10 001 X 11 --> 0x8B