Write a comparison note and how and when to adopt which modelling style.

Three types of modelling:

1. Gate level modelling :

The Circuit diagram of a digital circuit shows the logic gates present in it. Likewise in Structural modelling, we model a circuit by using **Primitive gates**, and predefined modules.When we design a Verilog code entirely using Primitive Logic Gates, it is called "**Gate Level Modelling**". This is Lowest level abstraction, and it is hard to understand the intent of the code by the human, but is easy and guaranteed for machine compiling and logical synthesis.

If we create smaller modules using Logic gates, and then we use those small modules to create a big circuit, it is called "**Structural Modelling**". We connect Gates and modules using wires here.

2. Data flow modelling :

Dataflow modelling is completely done by the logical expression of the digital circuit. We have logical and arithmetic operators in Verilog, which we can use to create logical expressions of the digital circuit.

This is a medium level abstraction. This type of modelling along with structural modelling is **Highly Recommended in ASIC design**.

3. Behavioral modelling :

The behavioural modelling completely depends on the truth table or behaviour of the circuit. In this modelling, we can design hardware without even knowing the components present in it, because it doesn’t care.

If we know the behaviour of the circuit, we can design it. This is the **highest level abstraction**. This modelling is recommended for FPGA prototyping and other Reconfigurable devices.