

# 11

## D-A AND A-D CONVERTERS

### 11.1 INTRODUCTION

Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superim-position of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion.

Figure 11.1 highlights a typical application within which A/D and D/A conversion is used. The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit. The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

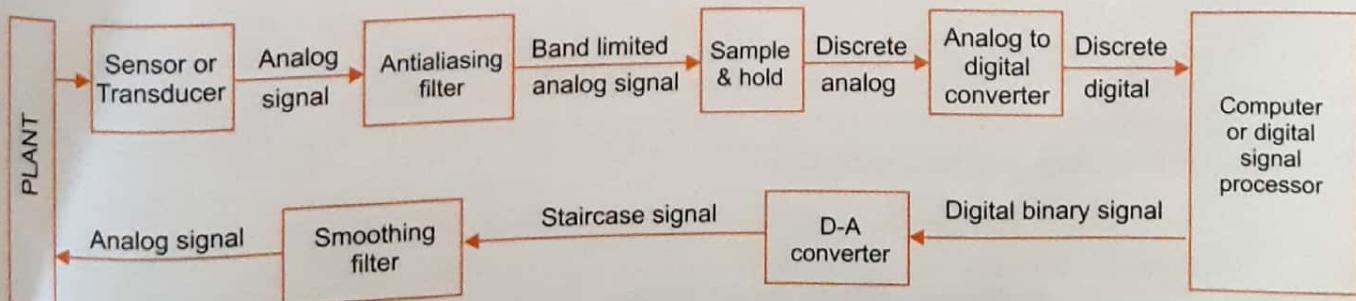


Fig. 11.1 Circuit showing application of A/D and D/A converter

The scheme given in Fig. 11.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

Both ADC and DAC are also known as data converters and are available in IC form. It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error. The A-D conversion usually makes use of a D-A converter so we shall first discuss DAC followed by ADC.

## 11.2 BASIC DAC TECHNIQUES

The schematic of a DAC is shown in Fig. 11.2. The input is an  $n$ -bit binary word  $D$  and is combined with a reference voltage  $V_R$  to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = K V_{FS} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}) \quad (11.1)$$

where,  $V_o$  = output voltage

$V_{FS}$  = full scale output voltage

$K$  = scaling factor usually adjusted to unity

$d_1 d_2 \dots d_n$  =  $n$ -bit binary fractional word with the decimal point located at the left

$d_1$  = most significant bit (MSB) with a weight of  $V_{FS}/2$

$d_n$  = least significant bit (LSB) with a weight of  $V_{FS}/2^n$

There are various ways to implement Eq. (11.1). Here we shall discuss the following resistive techniques only:

Weighted resistor DAC

R-2R ladder

Inverted R-2R ladder

### 11.2.1 Weighted Resistor DAC

One of the simplest circuits shown in Fig. 11.3 (a) uses a summing amplifier with a binary weighted resistor network. It has  $n$ -electronic switches  $d_1, d_2, \dots, d_n$  controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ( $-V_R$ ). And if the input bit is 0, the switch connects the resistor to the ground. From Fig. 11.3 (a), the output current  $I_o$  for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + \dots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \dots + \frac{V_R}{2^n R} d_n$$

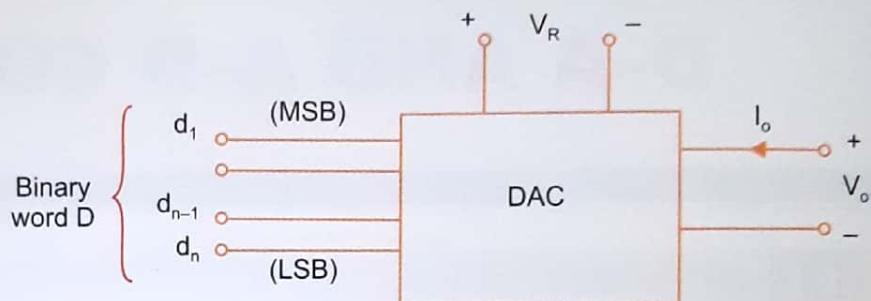
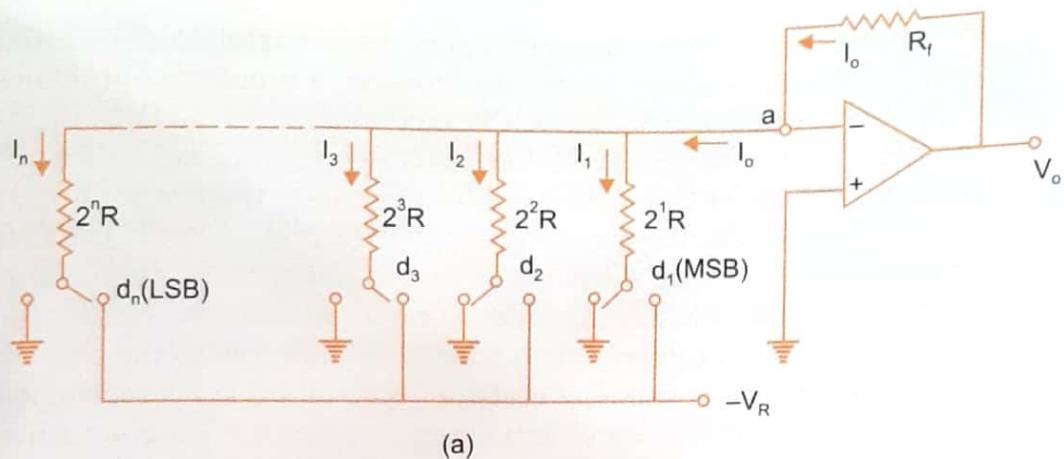
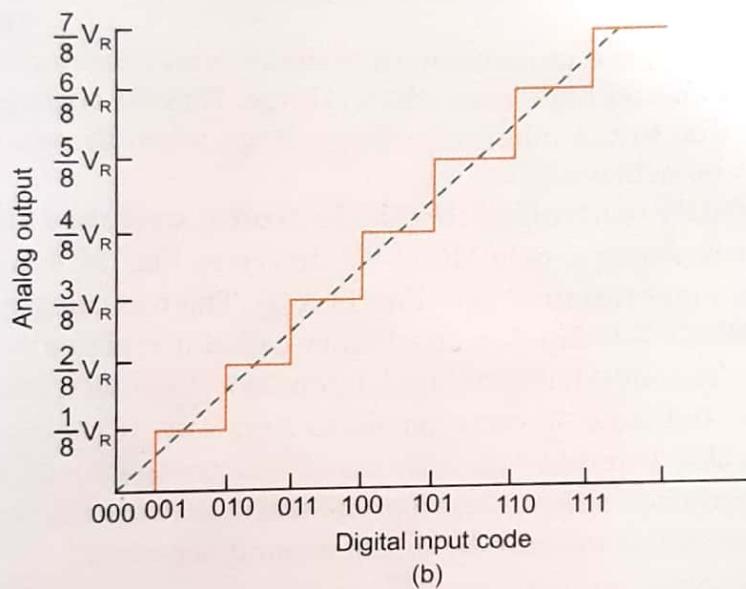


Fig. 11.2 Schematic of a DAC



(a)



(b)

**Fig. 11.3** (a) A simple weighted resistor DAC, (b) Transfer characteristics of a 3-bit DAC

$$= \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n})$$

The output voltage

$$V_o = I_o R_f = V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}) \quad (11.2)$$

Comparing Eq. (11.1) with Eq. (11.2), it can be seen that if  $R_f = R$  then  $K = 1$  and  $V_{FS} = V_R$ .

The circuit shown in Fig. 11.3 (a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 11.3 (b) for a 3-bit weighted resistor DAC. It may be noted that

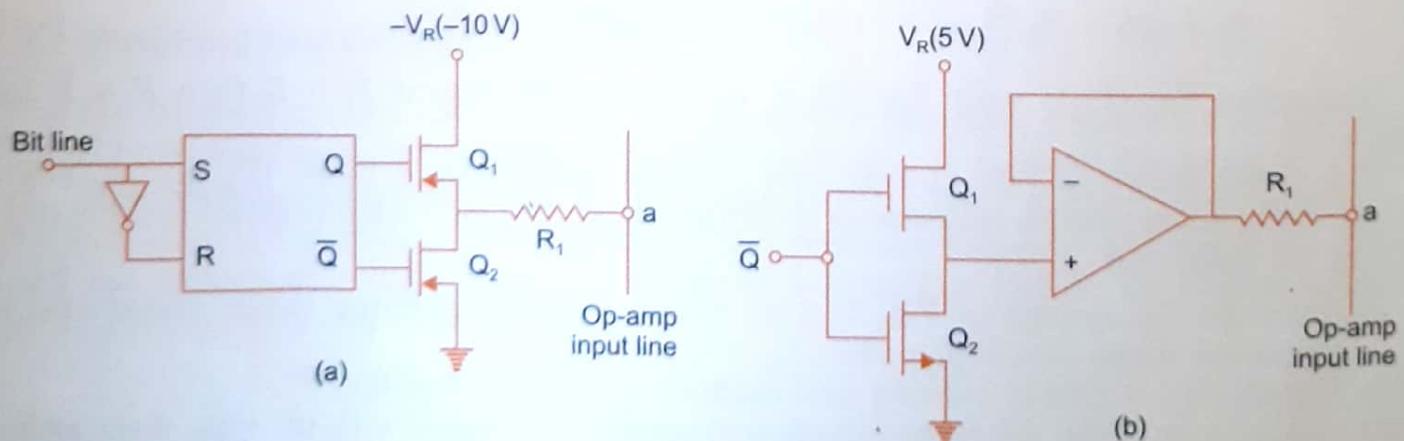
- (i) Although the op-amp in Fig. 11.3 (a) is connected in inverting mode, it can also be connected in non-inverting mode.
- (ii) The op-amp is simply working as a current to voltage converter.
- (iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be +5 V and the output will be negative.

The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature. There are however a number of problems associated with this type of DAC. One of the disadvantages of binary weighted type DAC is the wide range of resistor values required. It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bit increases, the range of resistance value increases. For 8-bit DAC, the resistors required are  $2^0R$ ,  $2^1R$ ,  $2^2R$ , ...,  $2^7R$ . The largest resistor is 128 times the smallest one for only 8-bit DAC. For a 12-bit DAC, the largest resistance required is  $5.12\text{ M}\Omega$  if the smallest is  $2.5\text{ k}\Omega$ . The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy. The choice of smallest resistor value as  $2.5\text{ k}\Omega$  is reasonable; otherwise loading effect will be there. The difficulty of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8-bits.

The switches in Fig. 11.3 (a) are in series with resistors and therefore, their ***on*** resistance must be very low and they should have zero offset voltage. Bipolar transistors do not perform well as voltage switches, due to the inherent offset voltage when in saturation. However, by using MOSFET, this can be achieved.

Different types of ***digitally controlled SPDT electronic switches*** are available of which two are shown in Fig. 11.4. A totem-pole MOSFET driver in Fig. 11.4 (a) feeds each resistor connected to the inverting input terminal 'a' of Fig. 11.3 (a). The two complementary gate inputs  $Q$  and  $\bar{Q}$  come from MOSFET S-R flip-flop or a binary cell of a register which holds one bit of the digital information to be converted to an analog number. Assume a negative logic, i.e. logic '1' corresponds to  $-10\text{ V}$  and logic '0' corresponds to zero volt. If there is '1' in the bit line,  $S = 1$  and  $R = 0$  so that  $Q = 1$  and  $\bar{Q} = 0$ . This drives the transistor  $Q_1$  ***on***, thus connecting the resistor  $R_1$  to the reference voltage  $-V_R$  whereas the transistor  $Q_2$  remains ***off***. Similarly a '0' at the bit line connects the resistor  $R_1$  to the ground terminal.

Another SPDT switch of Fig. 11.4(b) consists of CMOS inverter feeding an op-amp voltage follower which drives  $R_1$  from a very low output resistance. The circuit is using a positive logic with  $V(1) = V_R = +5\text{ V}$  and  $V(0) = 0\text{ V}$ . The complement  $\bar{Q}$  of the bit under consideration is applied at the input. Thus  $\bar{Q} = 0$  makes transistor  $Q_1$  ***off*** and  $Q_2$  ***on***. The output of the CMOS inverter is at logic 1, that is,  $5\text{ V}$  is applied to resistor  $R_1$  through the voltage follower. And if  $\bar{Q} = 1$  the output of the CMOS inverter is  $0\text{ V}$  connecting the resistance  $R_1$  to ground.



**Fig. 11.4 (a)** A totem pole MOSFET switch **(b)** CMOS inverter as switch

### 11.2.2 R-2R Ladder DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of  $R$  ranges from  $2.5 \text{ k}\Omega$  to  $10 \text{ k}\Omega$ .

For simplicity, consider a 3-bit DAC as shown in Fig. 11.5 (a), where the switch position  $d_1 d_2 d_3$  corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 11.5 (b) and finally to Fig. 11.5 (c). Then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R \left( \frac{2}{3} R \right)}{2R + \frac{2}{3} R} = -\frac{V_R}{4}$$

The output voltage is

$$V_o = \frac{-2R}{R} \left( -\frac{V_R}{4} \right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

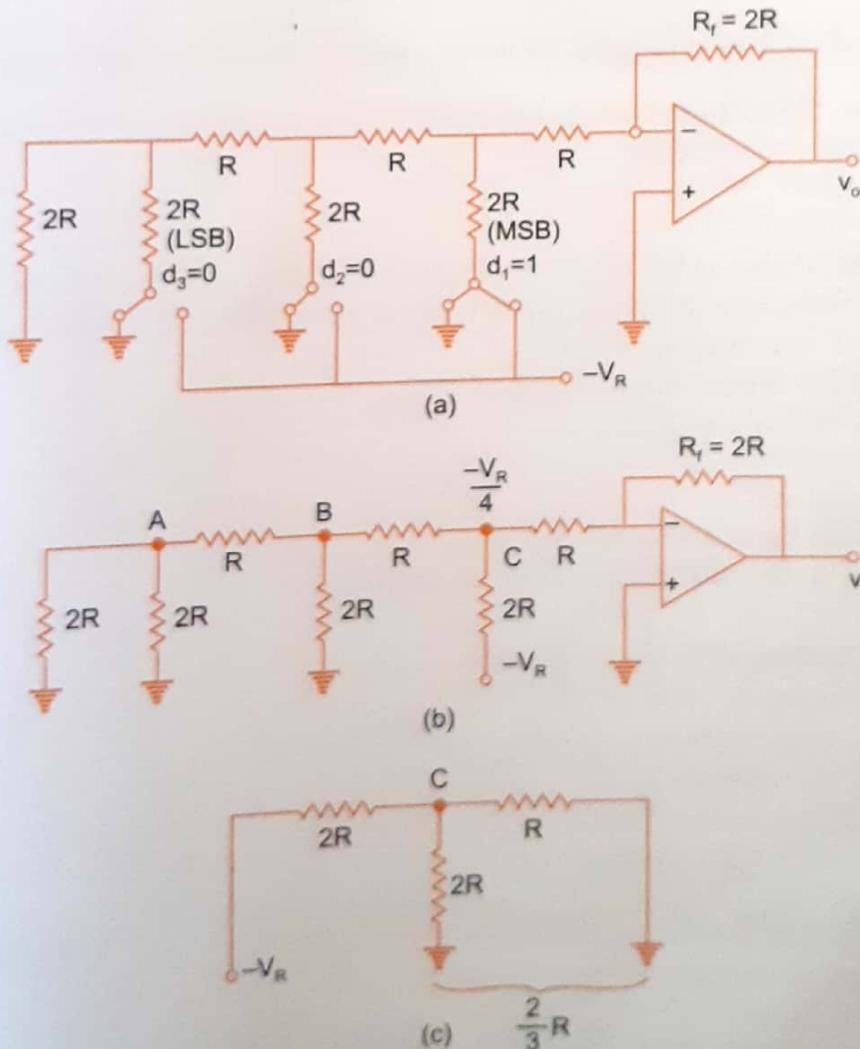
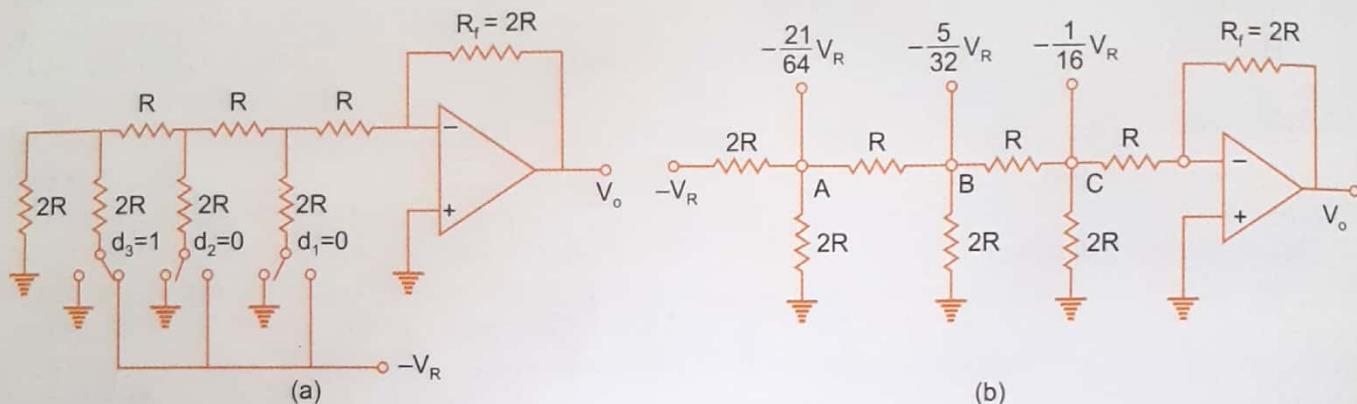


Fig. 11.5 (a) R-2R ladder DAC, (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 11.6 (a). The circuit can be simplified to the equivalent form of Fig. 11.6 (b). The voltages at the nodes (A, B, C) formed by resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_o = \left( -\frac{2R}{R} \right) \left( -\frac{V_R}{16} \right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$



**Fig. 11.6 (a)** R-2R ladder DAC for switch positions 001, **(b)** Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

### Example 11.1

Consider a 4 bit  $R-2R$  ladder DAC of the type shown in Fig 11.5 (a). Given  $R = 10 \text{ k}\Omega$  and  $V_R = 10 \text{ V}$ . Determine the value of the feedback resistance  $R_f$  for the following output conditions.

- (i) value of 1 LSB at the output is 0.5V
- (ii) analog output is 6V for a binary input of 1000
- (iii) full scale output voltage is 10 V

### Solution

- (i) Given  $R = 10 \text{ k}\Omega$ ,  $V_R = 10 \text{ V}$  and  $n = 4$

The resolution of a  $R - 2R$  ladder DAC is given by

$$\text{Resolution, } V = \frac{1}{2^n} \times \frac{V_R}{R} \times R_f$$

$$\text{Thus } 0.5V = \frac{1 \times 10V \times R_f}{2^4 \times 10 \times 10^3}$$

or

$$R_f = 8 \text{ k}\Omega$$

- (ii) For binary digital input 1000, setting  $d_1 = 1$  and  $d_2 = d_3 = d_4 = 0$  in Fig 11.3(a), we can write

$$V_o = V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4})$$

$$6 = \frac{R_f \times 10V \times 2^{-1}}{10 \times 10^3} \text{ (as } d_2 = d_3 = d_4 = 0\text{)}$$

Therefore,

$$R_f = 12 \text{ K}\Omega$$

(iii) Now  $d_1 = d_2 = d_3 = d_4 = 1$ . Thus for getting the full scale voltage of 10V,

$$R_f \times \frac{10}{10 \times 10^3} (2^{-1} + 2^{-2} + 2^{-3} + 2^{-4}) = 10$$

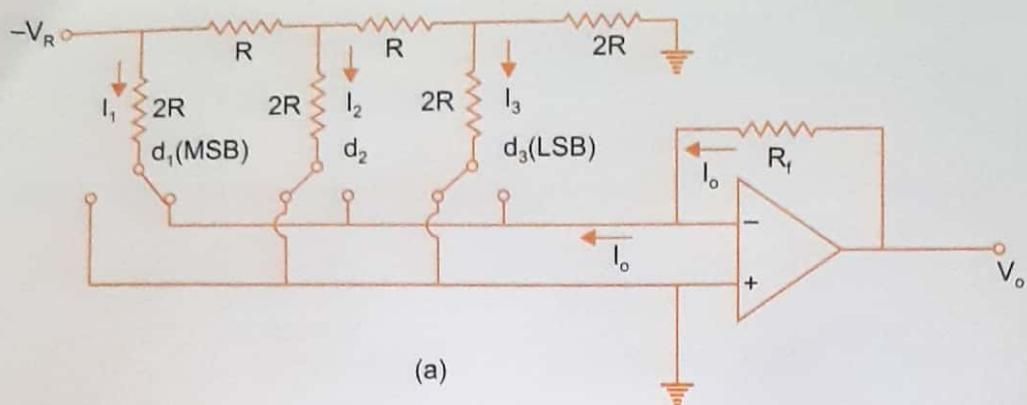
Thus

$$R_f = 10.667 \text{ K}\Omega$$

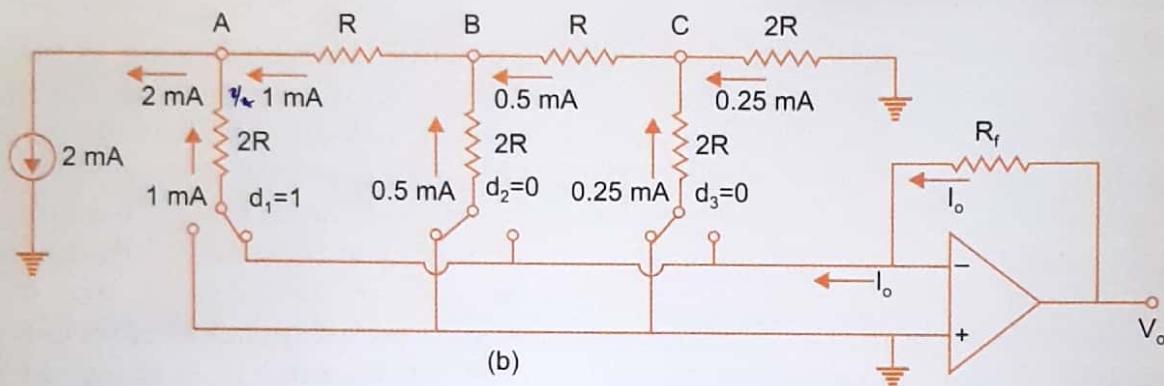
### 11.2.3 Inverted R-2R Ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. More power dissipation causes heating, which in turn, creates non-linearity in DAC. This is a serious problem and can be avoided completely in 'Inverted R-2R ladder type DAC'. A 3-bit Inverted R-2R ladder type DAC is shown in Fig. 11.7 (a) where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground. Since both the terminals of switches  $d_i$  are at ground potential, current flowing in the resistances is constant and independent of switch position, i.e. independent of input binary word. In Fig. 11.7 (a), when switch  $d_i$  is at logical '0' i.e., to the left, the current through 2R resistor flows to the ground and when the switch  $d_i$  is at logical '1' i.e., to the right, the current through 2R sinks to the virtual ground. The circuit has the important property that the current divides equally at each of the nodes. This is because the equivalent resistance to the right or to the left of any node is exactly 2 R. The division of the current is shown in Fig. 11.7 (b). Consider a reference current of 2 mA. Just to the right of node A, the equivalent resistor is 2 R. Thus 2 mA of reference input current divides equally to value 1 mA at node A. Similarly to the right of node B, the equivalent resistor is 2 R. Thus 1 mA of current further divides to value 0.5 mA at node B. Similarly, current divides equally at node C to 0.25 mA. The equal division of current in successive nodes remains the same in the 'inverted R-2R ladder' irrespective of the input binary word. Thus the currents remain constant in each branch of the ladder. Since constant current implies constant voltage, the ladder node voltages remain constant at  $V_R/2^0$ ,  $V_R/2^1$ ,  $V_R/2^2$ . The circuit works on the principle of summing currents and is also said to operate in the current mode. The most important advantage of the current mode or inverted ladder is that since the ladder node voltages remain constant even with changing input binary words (codes), the stray capacitances are not able to produce slow-down effects on the performance of the circuit.

It may be noted that the switches used in Fig. 11.7 (a) are the SPDT switches discussed earlier. According to bit  $d_i$ , the corresponding switch gets connected either to ground for  $d_i = 0$  or to  $-V_R$  for  $d_i = 1$ . The current flows from inverting input terminal to  $-V_R$  for  $d_i = 1$  and from ground to  $-V_R$  for  $d_i = 0$ . Regardless of the binary input word, the current in the resistive branches of the inverted ladder circuit remains always constant as explained in Fig. 11.7(b). However, the current through the feedback resistor  $R$  is the summing current depending upon the input binary word. It may further be mentioned that, Fig. 11.7 (b) shows only the current division for making the analysis simple, though it is a voltage driven DAC.



(a)



(b)

**Fig. 11.7** (a) Inverted  $R - 2R$  ladder DAC, (b) Inverted  $R - 2R$  ladder DAC showing division of current for digital input word 001

### Example 11.2

Consider the inverted  $R - 2R$  ladder DAC shown in Fig 11.7 (a) Given  $R = R_f = 10 \text{ k}\Omega$  and  $V_R = 10\text{V}$ . Calculate the output voltage for the binary input of 1110.

### Solution

In Fig 11.7 (a),

$$I_1 = \frac{V_R}{2R} = \frac{10\text{V}}{2 \times 10 \times 10^3} = 0.5 \text{ mA}$$

$$I_2 = \frac{I_1}{2} = 0.25 \text{ mA}$$

$$I_3 = \frac{I_2}{2} = 0.125 \text{ mA}$$

and

$$\begin{aligned} I_o &= I_1 + I_2 + I_3 \\ &= 0.5 + 0.25 + 0.125 \text{ mA} \\ &= 0.875 \text{ mA} \end{aligned}$$

Therefore, current

$$\begin{aligned} V_o &= I_o \times R_f \\ &= 0.875 \times 10^{-3} \times 10 \times 10^3 \\ &= 8.75 \text{ V} \end{aligned}$$

The output voltage,

### 11.2.4 Multiplying DACs

A digital to analog converter which uses a varying reference voltage  $V_R$  is called a multiplying D/A converter (MDAC). Thus if in the Eq. (11.1), the reference voltage  $v_R$  is a sine wave given by

$$v_R(t) = V_{im} \cos 2\pi ft$$

Then,  $v_o(t) = V_{om} \cos (2\pi ft + 180^\circ)$

where  $V_{om}$  will vary from 0V to  $(1 - 2^{-n}) V_{im}$  depending upon the input code. When used like this, MDAC behaves as a digitally controlled audio attenuator because the output  $V_o$  is a fraction of the voltage representing the input digital code and the attenuator setting can be controlled by digital logic. If followed by an op-amp integrator, the MDAC provides digitally programmable integration which can be used in the design of digitally programmable oscillators, filters.

### 11.2.5 Monolithic DAC : 1408 DAC

Monolithic DACs consisting of R-2R ladder, switches and the feedback resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers. The MC 1408L is a 8-bit DAC with a current output. The SE/NE 5018 is also a 8-bit DAC but with a voltage output. There are hybrid D/A converters available in DATEL DAC-HZ series for current as well as voltage output.

A typical 8-bit DAC 1408 compatible with TTL and CMOS logic with settling time around 300 ns is shown in Fig. 11.8 (a). It has eight input data lines  $d_1$  (MSB) through  $d_8$  (LSB). It requires 2 mA reference current for full scale input and two power supplies  $V_{CC} = +5$  V and  $V_{EE} = -5$  V ( $V_{EE}$  can range from -5 V to -15 V). The total reference current source is determined by resistor  $R_{14}$  and voltage reference  $V_R$  and is equal to  $V_R/R_{14} = 5$  V/2.5 k $\Omega$  = 2 mA. The resistor  $R_{15} = R_{14}$  match the input impedance of the reference source. The output current  $I_o$  is calculated as

$$I_o = \frac{V_R}{R_{14}} \left( \sum_{i=1}^8 d_i 2^{-i} \right); d_i = 0 \text{ or } 1$$

For full scale input (i.e.  $d_8$  through  $d_1 = 1$ )

$$I_o = \frac{5 \text{ V}}{2.5 \text{ k}\Omega} \left( \sum_{i=1}^8 1 \times 2^{-i} \right) = 2 \text{ mA} (255/256) = 1.992 \text{ mA}$$

The output is 1 LSB less than the full scale reference current of 2 mA. So, the output voltage  $V_o$  for the full scale input is

$$V_o = 2 \text{ mA} (255/256) \times 5 \text{ k}\Omega = 9.961 \text{ V}$$

In general, the output voltage  $V_o$  is given by

$$V_o = \frac{V_R}{R_{14}} R_f \left[ \frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \dots + \frac{d_8}{256} \right]$$

The 1408 DAC can be calibrated for bipolar range from -5 V to +5 V by adding resistor  $R_B$  (5 k $\Omega$ ) between  $V_R$  and output pin 4 as shown in Fig. 11.8 (b). The resistor  $R_B$  supplies 1 mA ( $= V_R/R_B$ ) current to the output in the opposite direction of the current generated by the input signal. Therefore the output current for the bipolar operation  $I'_o$  is

$$I'_o = I_o - (V_R/R_B) = (V_R/R_{14}) \left( \sum_{i=1}^8 d_i 2^{-i} \right) - (V_R/R_B)$$

For binary input word = 00000000, i.e. zero input, the output becomes,

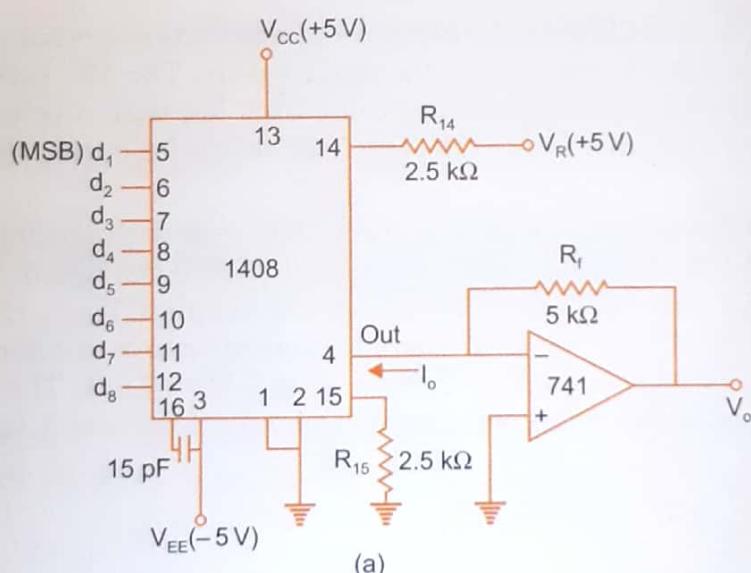
$$V_o = I'_o R_f = (I_o - V_R/R_B) R_f = (0 - 5 \text{ V}/5 \text{ k}\Omega) \times 5 \text{ k}\Omega = -5 \text{ V}$$

For binary input word = 10000000, output  $V_o$  becomes

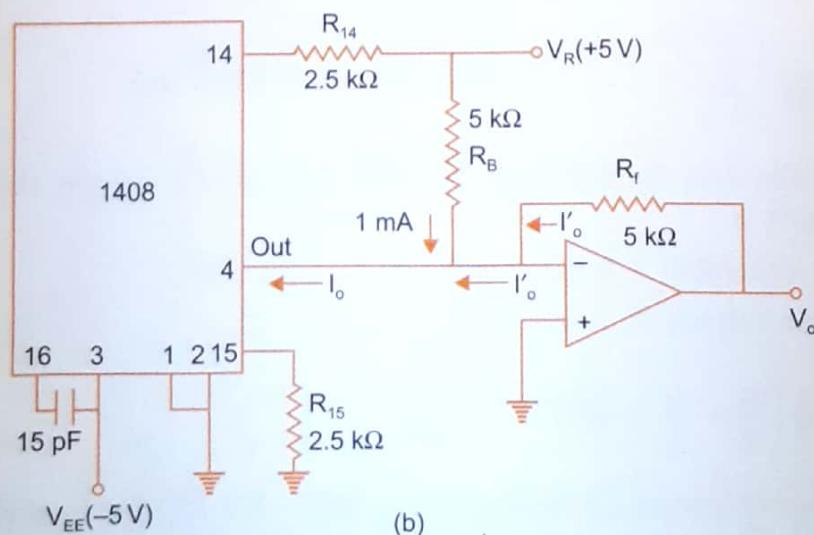
$$\begin{aligned} V_o &= (I_o - V_R/R_B) R_f = [(V_R/R_{14}) (d_1/2) - (V_R/R_B)] R_f \\ &= [(5 \text{ V}/2.5 \text{ k}\Omega) (1/2) - (5 \text{ V}/5 \text{ k}\Omega)] 5 \text{ k}\Omega = (1 \text{ mA} - 1 \text{ mA}) \times 5 \text{ k}\Omega = 0 \text{ V} \end{aligned}$$

For binary input word = 11111111, output  $V_o$  becomes

$$\begin{aligned} V_o &= [(V_R/R_{14}) (255/256) - (V_R/R_B)] R_f = (1.992 \text{ mA} - 1 \text{ mA}) \times 5 \text{ k}\Omega \\ &= 0.992 \text{ mA} \times 5 \text{ k}\Omega = +4.960 \text{ V} \end{aligned}$$



(a)



(b)

**Fig. 11.8** 1408 D/A converter (a) Voltage output in unipolar range (b) Modified circuit for bipolar output

**Example 11.3**

The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0 V, what output is produced if the input is 101101111?

**Solution**

The output voltage for input 101101111 is

$$\begin{aligned} &= 10.3 \text{ mV} (1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0) \\ &= 10.3 \text{ mV} (367) = 3.78 \text{ V} \end{aligned}$$

**Example 11.4**

Calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10 V range.

**Solution**

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

$$\text{For } 10 \text{ V range, } \text{LSB} = \frac{10 \text{ V}}{256} = 39 \text{ mV}$$

and

$$\text{MSB} = \left(\frac{1}{2}\right) \text{ full scale} = 5 \text{ V}$$

$$\text{Full scale output} = (\text{Full scale voltage} - 1 \text{ LSB})$$

$$= 10 \text{ V} - 0.039 \text{ V} = 9.961 \text{ V}$$

**Example 11.5**

What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is

- (i) 10 (for a 2-bit D/A converter)
- (ii) 0110 (for a 4-bit DAC)
- (iii) 10111100 (for a 8-bit DAC)

**Solution**

$$(i) V_o = 10 \text{ V} \left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = 5 \text{ V}$$

$$\begin{aligned} (ii) V_o &= 10 \text{ V} \left(0 \times \frac{1}{2} + 1 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 0 \times \frac{1}{2^4}\right) \\ &= 10 \left(\frac{1}{4} + \frac{1}{8}\right) = 3.75 \text{ V} \end{aligned}$$

$$\begin{aligned} (iii) V_o &= 10 \text{ V} (1 \times 1/2 + 0 \times 1/2^2 + 1 \times 1/2^3 + 1 \times 1/2^4 + 1 \times 1/2^5 \\ &\quad + 1 \times 1/2^6 + 0 \times 1/2^7 + 0 \times 1/2^8) \\ &= 10 \text{ V} (1/2 + 1/8 + 1/16 + 1/32 + 1/64) = 7.34 \text{ V} \end{aligned}$$

**11.3 A-D CONVERTERS**

The block schematic of ADC shown in Fig. 11.9 provides the function just opposite to that of a DAC. It accepts an analog input voltage  $V_a$  and produces an output binary word  $d_1 d_2 \dots d_n$  of

functional value  $D$ , so that

$$D = d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n} \quad (11.3)$$

where  $d_1$  is the most significant bit and  $d_n$  is the least significant bit. An ADC usually has two additional control lines: the START input to tell the ADC when to start the conversion and the EOC (end of conversion) output to announce when the conversion is complete. Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.

ADCs are classified broadly into two groups according to their conversion technique. Direct type ADCs and Integrating type ADCs. Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes

- Flash (comparator) type converter
- Counter type converter
- Tracking or servo converter
- Successive approximation type converter

Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:

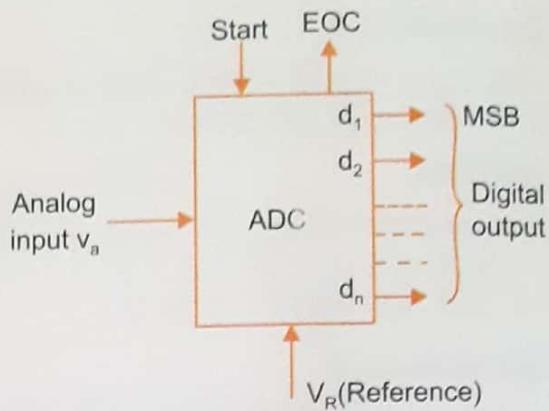
- (i) Charge balancing ADC
- (ii) Dual slope ADC

The most commonly used ADCs are successive approximation and the integrator type. The successive approximation ADCs are used in applications such as data loggers and instrumentation where conversion speed is important. The successive approximation and comparator type are faster but generally less accurate than integrating type converters. The flash (comparator) type is expensive for high degree of accuracy. The integrating type converter is used in applications such as digital meter, panel meter and monitoring systems where the conversion accuracy is critical.

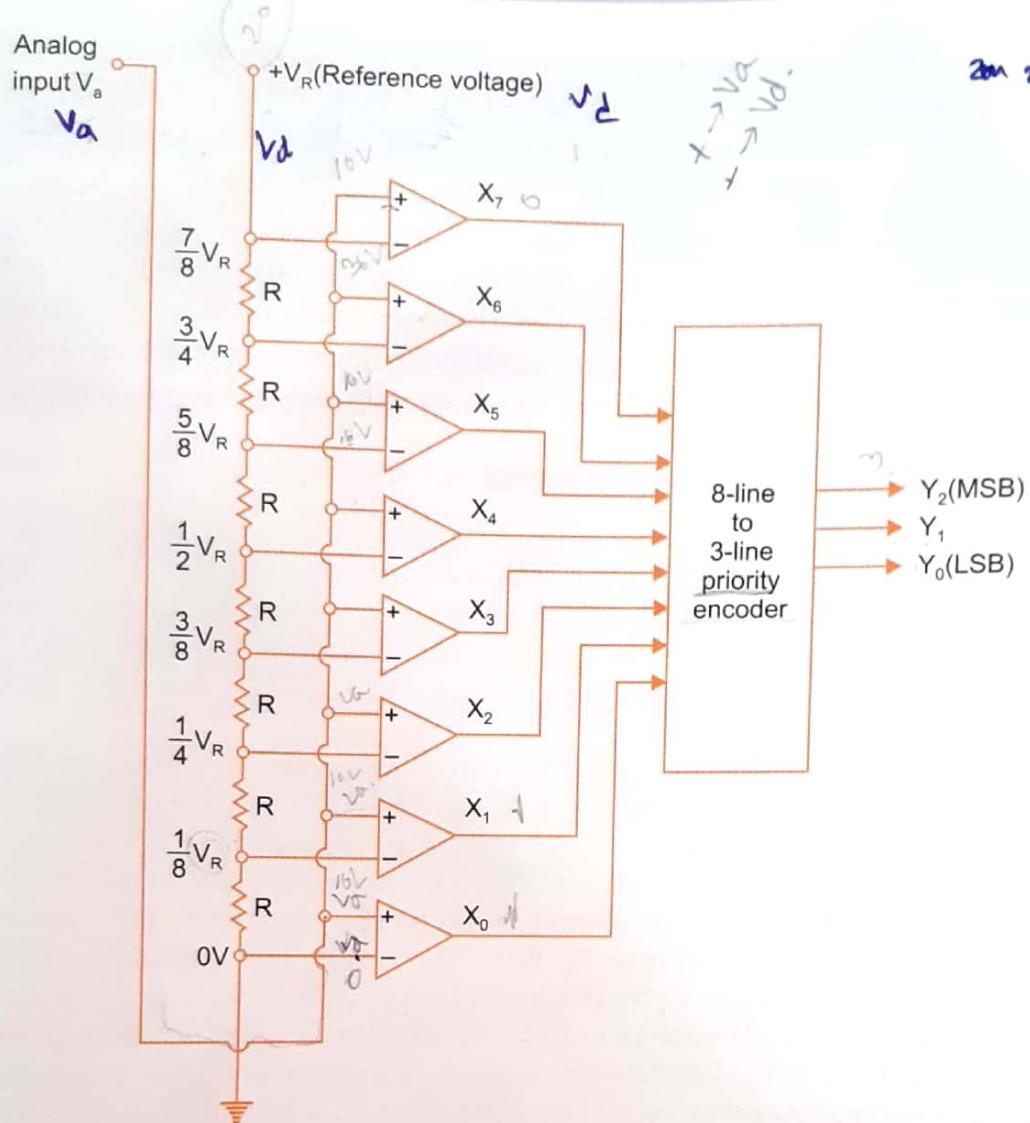
## DIRECT TYPE ADCs

### 11.3.1 The Parallel Comparator (Flash) A/D Converter

This is the simplest possible A/D converter. It is at the same time, the fastest and most expensive technique. Figure 11.10 (a) shows a 3-bit A/D converter. The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder). The comparator and its truth table is shown in Fig. 11.10 (b). A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage as shown in the truth table. Coming back to Fig. 11.10 (a), at each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage  $V_R$  and the ground. The purpose of the circuit is to compare the analog input voltage  $V_a$  with each of the node voltages. The truth table for the flash type AD converter is shown in Fig. 11.10 (c). The circuit has the advantage of high speed as the

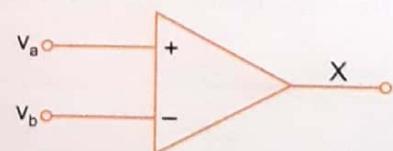


**Fig. 11.9** Functional diagram of ADC



**Fig. 11.10 (a)** Basic circuit of a flash type A/D converter

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value



**Fig. 11.10 (b)** Comparator and its truth table

Input voltage $V_a$	$X_7$	$X_6$	$X_5$	$X_4$	$X_3$	$X_2$	$X_1$	$X_0$	$Y_2$	$Y_1$	$Y_0$
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to $3 V_R/8$	0	0	0	0	0	1	1	1	0	1	0
$3 V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to $5 V_R/8$	0	0	0	1	1	1	1	1	1	0	0
$5 V_R/8$ to $3 V_R/4$	0	0	1	1	1	1	1	1	1	0	1
$3 V_R/4$ to $7 V_R/8$	0	1	1	1	1	1	1	1	1	1	0
$7 V_R/8$ to $V_R$	1	1	1	1	1	1	1	1	1	1	1

**Fig. 11.10 (c)** Truth table for a flash type A/D converter

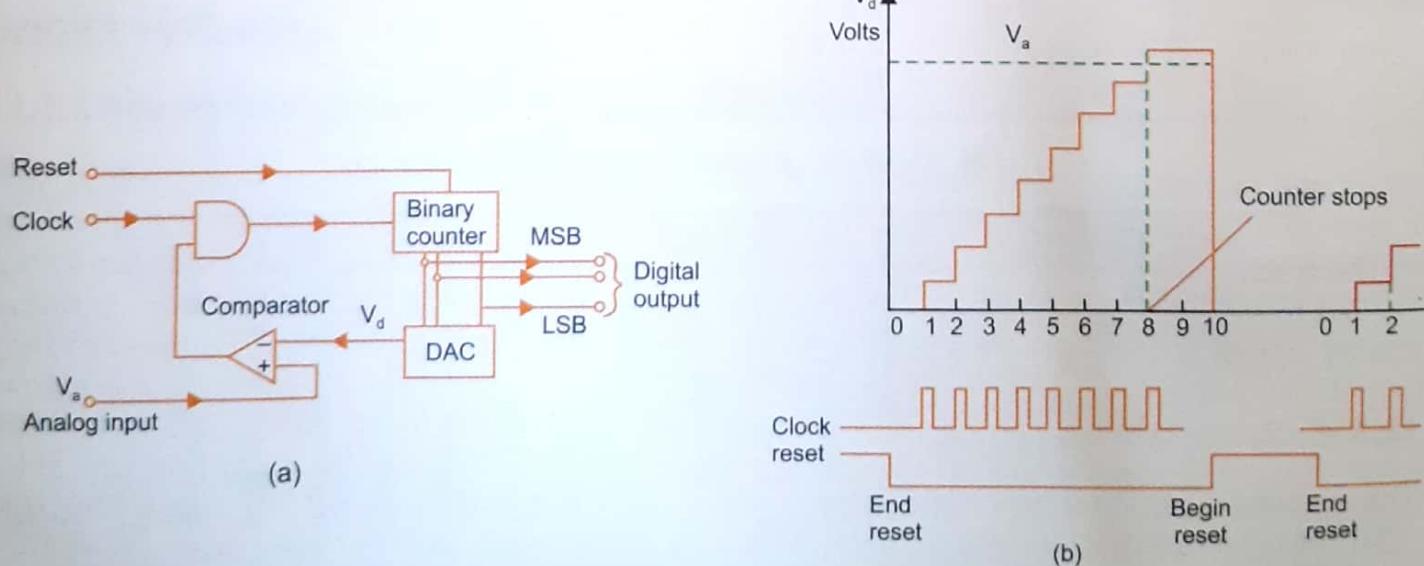
conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro Devices AMD 686A comparator and a T1147 priority encoder, conversion delays of the order of 20 ns can be obtained.

This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit. A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators. In general, the number of comparators required are  $2^n - 1$  where  $n$  is the desired number of bits. Hence the number of comparators approximately doubles for each added bit. Also the larger the value of  $n$ , the more complex is the priority encoder.

### 11.3.2 The Counter Type A/D Converter

The D to A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes within  $\pm (1/2)$  LSB to the analog input  $V_a$  which is to be converted to binary digital form. Thus in addition to the DAC, we need suitable logic circuitry to perform the code search and a comparator of adequate quality to announce when the DAC output has come within  $\pm (1/2)$  LSB to  $V_a$ .

A 3-bit counting ADC based upon the above principle is shown in Fig. 11.11 (a). The counter is reset to zero count by the reset pulse. Upon the release of RESET, the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time. The binary word representing this count is used as the input of a D/A converter whose output is a staircase of the type shown in Fig. 11.11 (b). The analog output  $V_d$  of DAC is compared to the analog input  $V_a$  by the comparator. If  $V_a > V_d$ , the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When  $V_a < V_d$ , the output of the comparator becomes low and the AND gate is disabled. This stops the counting at the time  $V_a \leq V_d$  and the digital output of the counter represents the analog input voltage  $V_a$ . For a new value of analog input  $V_a$ , a second reset pulse is applied to clear the counter. Upon the end of the reset, the counting begins again as shown in Fig. 11.11 (b). The counter frequency must be low enough to give sufficient time



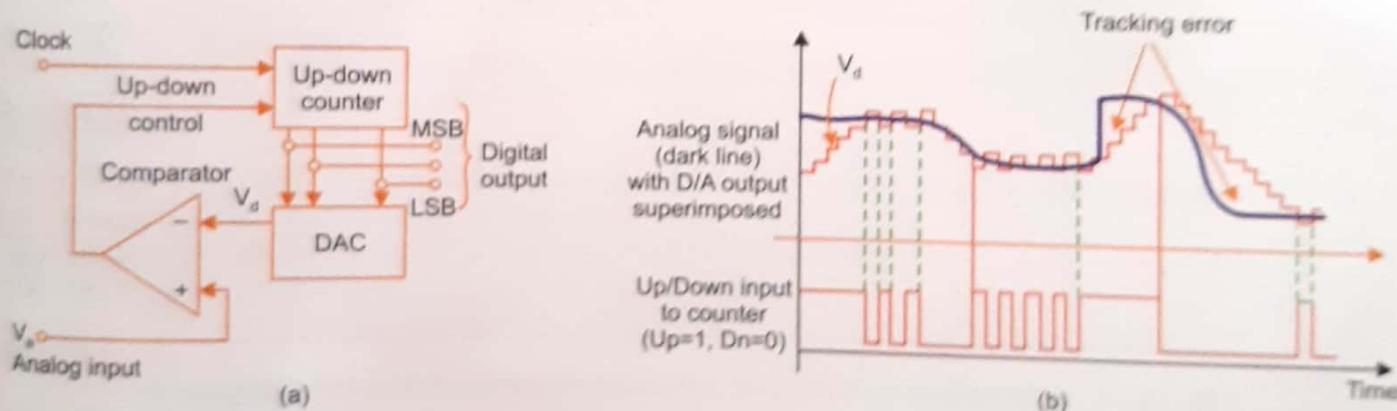
**Fig. 11.11** (a) A counter type A/D converter, (b) D/A output staircase waveform

for the DAC to settle and for the comparator to respond. Low speed is the most serious drawback of this method. The conversion time can be as long as  $(2^n - 1)$  clock periods depending upon the magnitude of input voltage  $V_a$ . For instance, a 12-bit system with 1 MHz clock frequency, the counter will take  $(2^{12} - 1) \mu s = 4.095 \text{ ms}$  to convert a full scale input.

If the analog input voltage varies with time, the input signal is sampled, using a sample and hold circuit before it is applied to the comparator. If the maximum value of the analog voltage is represented by  $n$ -pulses and if the clock period is  $T$  seconds, the minimum interval between samples is  $nT$  seconds.

### 11.3.3 Servo Tracking A/D Converter

An improved version of counting ADC is the tracking or a servo converter shown in Fig. 11.12 (a). The circuit consists of an up/down counter with the comparator controlling the direction of the count. The analog output of the DAC is  $V_d$  and is compared with the analog input  $V_a$ . If the input  $V_a$  is greater than the DAC output signal, the output of the comparator goes high and the counter is caused to count up. The DAC output increases with each incoming clock pulse and when it becomes more than  $V_a$ , the counter reverses the direction and counts down (but only by one count, LSB). This causes the control to count up and the count increases by 1 LSB. The process goes on being repeated and the digital output changes back and forth by  $\pm 1$  LSB around the correct value. As long as the analog input changes slowly, the tracking A/D will be within one LSB of the correct value. However, when the analog input changes rapidly, the tracking A/D cannot keep up with the change and error occurs as shown in Fig. 11.12 (b).



**Fig. 11.12** (a) A tracking A/D converter, (b) Waveforms associated with a tracking A/D converter

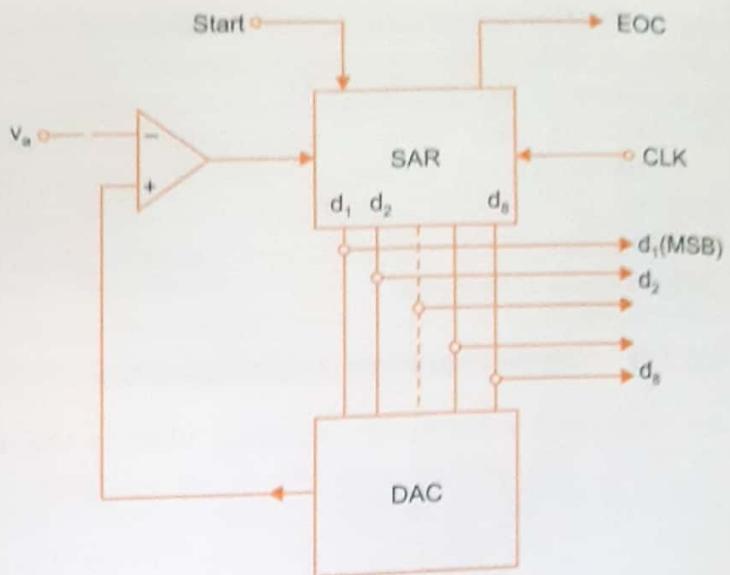
The tracking ADC has the advantage of being simple. The disadvantage, however, is the time needed to stabilize as a new conversion value is directly proportional to the rate at which the analog signal changes.

### 11.3.4 Successive Approximation Converter

The successive approximation technique uses a very efficient code search strategy to complete  $n$ -bit conversion in just  $n$ -clock periods. An eight bit converter would require eight clock pulses to obtain a digital output. Figure 11.13 shows an eight bit converter. The circuit uses a

successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows. With the arrival of the START command, the SAR sets the MSB  $d_1 = 1$  with all other bits to zero so that the trial code is 10000000. The output  $V_d$  of the DAC is now compared with analog input  $V_a$ . If  $V_a$  is greater than the DAC output  $V_d$  then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.

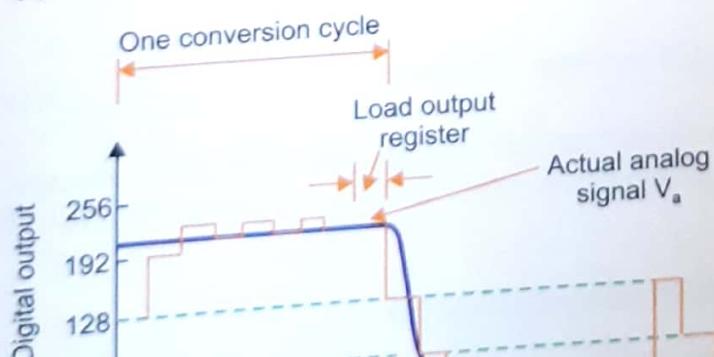
However, if  $V_a$  is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested. Whenever the DAC output crosses  $V_a$ , the comparator changes state and this can be taken as the **end of conversion** (EOC) command. Figure 11.14 (a) shows a typical conversion sequence and Fig. 11.14 (b).



**Fig. 11.13** Functional diagram of the successive approximation ADC

Correct digital representation	Successive approximation register output $V_d$ at different stages in conversion	Comparator output
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

**Fig. 11.14 (a)** Successive approximation conversion sequence for a typical analog input



shows the associated wave forms. It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.

A comparison of the speed of an eight bit tracking ADC and an eight bit successive approximation ADC is made in Fig. 11.15. Given the same clock frequency, we see that the tracking circuit is faster only for small changes in the input. In general, the successive approximation technique is more versatile and superior to all other circuits discussed so far. Successive approximation ADCs are available as self contained ICs. The AD7592 (Analog Devices Co.) a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.

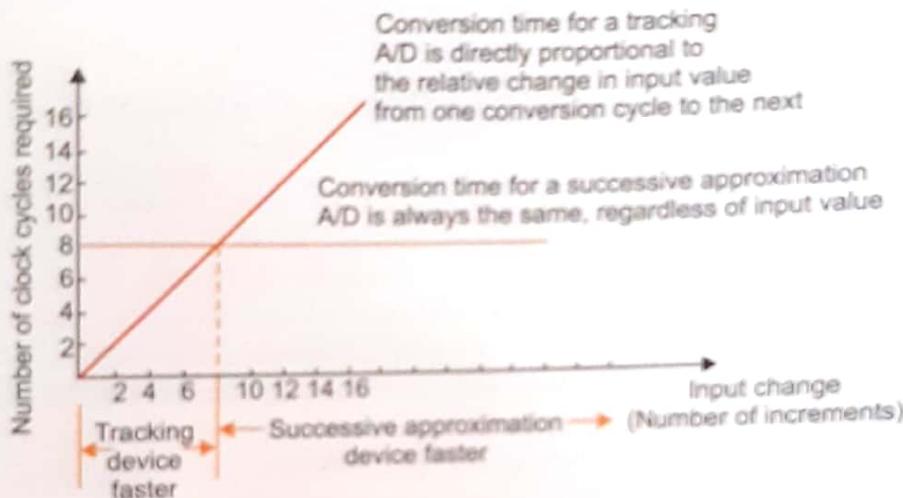


Fig. 11.15 Comparison of conversion times for tracking and successive approximation A/D devices

### Example 11.6

An 8-bit A/D converter is used for converting 0 to 10V input voltage. Determine :

- input voltage required to change by 1 LSB
- input voltage required to generate all 1's at the output
- the digital output for an input voltage of 4.8V

### Solution

$$\text{i) } 1 \text{ LSB} = \frac{10V}{2^8} = 39.1 \text{ mV}$$

(ii) Since digital output starts from 0 in a A/D converter, therefore the maximum full-scale input voltage will produce output less by 1 LSB for all digital output 1's.

$$\text{Thus, } V_{iFS} = 10V - 39.1 \text{ mV} = 9.961 \text{ V.}$$

(iii) The digital output for an input voltage of 4.8V is given by

$$D = \frac{4.8V}{39.1 \text{ mV}} = 122.76$$

$$= 123$$

Converting this to binary gives the digital output as 01111011.

**Example 11.7**

The conversion rate of a 8-bit ADC is  $9 \mu\text{s}$ . Find the maximum frequency of the input sine wave that can be digitized.

**Solution**

The maximum frequency is given by

$$\begin{aligned} f_{\max} &= \frac{1}{2\pi(T_C)2^n} \\ &= \frac{1}{2\pi \times 9 \times 10^{-6} \times 2^8} \\ &= 69.07 \text{ Hz.} \end{aligned}$$

**Integrating Type of ADCs**

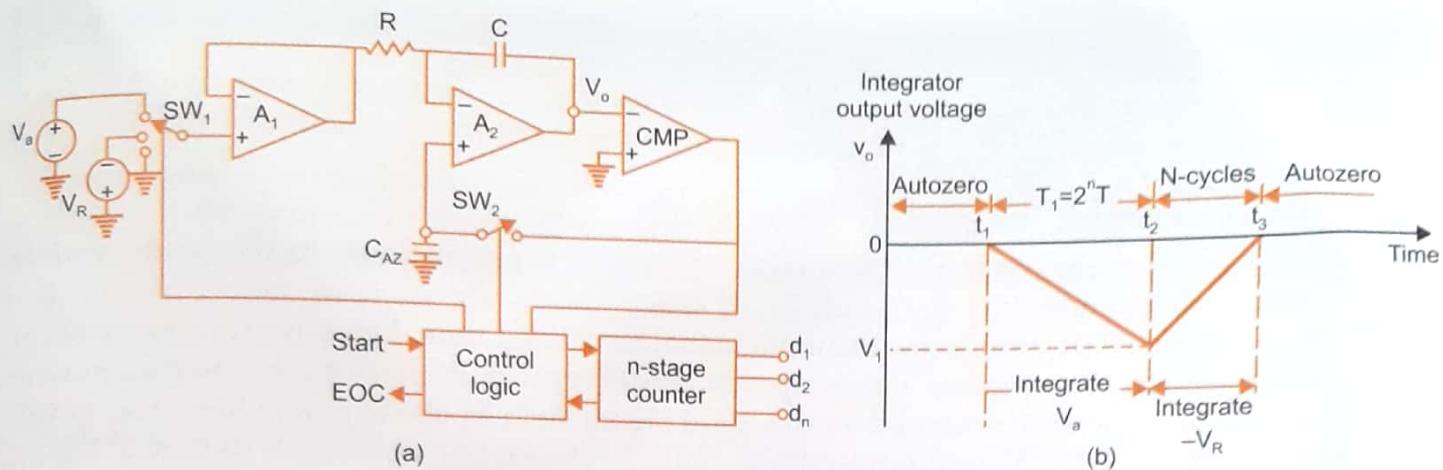
The integrating type of ADCs do not require a S/H circuit at the input. If the input changes during conversion, the ADC output code will be proportional to the value of the input averaged over the integration period.

**11.3.5 Charge Balancing ADC**

The principle of charge balancing ADC is to first convert the input signal to a frequency using a voltage to frequency (V/F) converter. This frequency is then measured by a counter and converted to an output code proportional to the analog input. The main advantage of these converters is that it is possible to transmit frequency even in noisy environment or in isolated form. However, the limitation of the circuit is that the output of V/F converter depends upon an  $RC$  product whose value cannot be easily maintained with temperature and time. The drawback of the charge balancing ADC is eliminated by the dual slope conversion.

**11.3.6 Dual-Slope ADC**

Figure 11.16 (a) shows the functional diagram of the dual-slope or dual-ramp converter. The analog part of the circuit consists of a high input impedance buffer  $A_1$ , precision integrator  $A_2$  and a voltage comparator. The converter first integrates the analog input signal  $V_a$  for a fixed duration of  $2^n$  clock periods as shown in Fig. 11.16 (b). Then it integrates an internal reference voltage  $V_R$  of opposite polarity until the integrator output is zero. The number  $N$  of clock cycles required to return the integrator to zero is proportional to the value of  $V_a$  averaged over the integration period. Hence  $N$  represents the desired output code. The circuit operates as follows:



**Fig. 11.16** (a) Functional diagram of the dual slope ADC (b) Integrated output waveform for the dual slope ADC

Before the START command arrives, the switch \$SW\_1\$ is connected to ground and \$SW\_2\$ is closed. Any offset voltage present in the \$A\_1, A\_2\$, comparator loop after integration, appears across the capacitor \$C\_{AZ}\$ till the threshold of the comparator is achieved. The capacitor \$C\_{AZ}\$ thus provides automatic compensation for the input-offset voltages of all the three amplifiers. Later, when \$SW\_2\$ opens, \$C\_{AZ}\$ acts as a memory to hold the voltage required to keep the offset nulled. At the arrival of the START command at \$t = t\_1\$, the control logic opens \$SW\_2\$ and connects \$SW\_1\$ to \$V\_a\$ and enables the counter starting from zero. The circuit uses an \$n\$-stage ripple counter and therefore the counter resets to zero after counting \$2^n\$ pulses. The analog voltage \$V\_a\$ is integrated for a fixed number \$2^n\$ counts of clock pulses after which the counter resets to zero. If the clock period is \$T\$, the integration takes place for a time \$T\_1 = 2^n \times T\$ and the output is a ramp going downwards as shown in Fig. 11.16 (b).

The counter resets itself to zero at the end of the interval \$T\_1\$ and the switch \$SW\_1\$ is connected to the reference voltage (\$-V\_R\$). The output voltage \$v\_o\$ will now have a positive slope. As long as \$v\_o\$ is negative, the output of the comparator is positive and the control logic allows the clock pulse to be counted. However, when \$v\_o\$ becomes just zero at time \$t = t\_3\$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at \$t\_3\$ is proportional to the analog input voltage \$V\_a\$.

In Fig. 11.16 (b)

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}} \quad (11.4)$$

and

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}} \quad (11.5)$$

For an integrator,

$$\Delta v_o = (-1/RC) V(\Delta t) \quad (11.6)$$

The voltage \$v\_o\$ will be equal to \$v\_1\$ at the instant \$t\_2\$ and can be written as

$$v_1 = (-1/RC) V_a(t_2 - t_1)$$

The voltage \$v\_1\$ is also given by

$$v_1 = (-1/RC) (-V_R) (t_2 - t_3)$$

So,

$$V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

Putting the values of  $(t_2 - t_1) = 2^n$  and  $(t_3 - t_2) = N$ , we get

$$V_a(2^n) = (V_R)N$$

or,

$$V_a = (V_R)(N/2^n)$$

(11.7)

The following important observations can be made:

1. Since  $V_R$  and  $n$  are constant, the analog voltage  $V_a$  is proportional to the count reading  $N$  and is independent of  $R$ ,  $C$  and  $T$ .
2. The dual-slope ADC integrates the input signal for a fixed time, hence it provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time  $T_1$ . Thus ac noise superimposed on the input signal such as 50 Hz power line pick-up will be averaged during the input integration time. So choose clock period  $T$ , so that  $2^n T$  is an exact integral multiple of the line period (1/50) second = 20 ms.
3. The main disadvantage of the dual-slope ADC is the long conversion time. For instance, if  $2^n - T = 1/50$  is used to reject line pick-up, the conversion time will be 20 ms.

Dual-slope converters are particularly suitable for accurate measurement of slowly varying signals, such as thermocouples and weighing scales. Dual-slope ADCs also form the basis of digital panel meters and multimeters.

Dual-slope converters are available in monolithic form and are available both in microprocessor compatible and in display oriented versions. The former provide the digital code in binary form whereas the display oriented versions present the output code in a format suitable for the direct drive of LED displays. The Datel Intersil ICL7109 is a monolithic 12-bit dual-slope ADC with microprocessor compatibility.

### Example 11.8

A dual slope ADC uses a 16-bit counter and a 4 MHz clock rate. The maximum input voltage is +10 V. The maximum integrator output voltage should be -8 V when the counter has cycled through  $2^n$  counts. The capacitor used in the integrator is  $0.1 \mu\text{F}$ . Find the value of the resistor  $R$  of the integrator.

### Solution

$$\text{Time period } (t_2 - t_1) \text{ in Fig. 11.16 (b)} = \frac{2^{16}}{4 \text{ MHz}} = \frac{65536}{4 \text{ MHz}} = 16.38 \text{ ms}$$

For the integrator

$$\Delta v_o = (-1/RC) V_a(t_2 - t_1)$$

$$\text{So, } RC = -(10 \text{ V} - 8 \text{ V}) / 16.3 \text{ ms} = 20.47 \text{ ms}$$

$$R = \frac{20.47 \text{ ms}}{0.1 \mu\text{F}} = 204.7 \text{ k}\Omega = 205 \text{ k}\Omega$$

### Example 11.9

If the analog signal  $V_a$  is +4.129 V in the example 11.4, find the equivalent digital number.

### Solution

$$\text{Since, } V_a = V_R(N/2^n)$$

So the digital count  $N = 2^n$  ( $V_a/V_R$ ) = 65536 (4.129 V/8 V) = 33825 for which the binary equivalent is 1000010000100001.

## 11.4 DAC/ADC SPECIFICATIONS

Both D/A and A/D converters are available with wide range of specifications. The various important specifications of converters generally specified by the manufacturers are analyzed.

**Resolution:** The resolution of a converter is the smallest change in voltage which may be produced at the output (or input) of the converter. For example, an 8-bit D/A converter has  $2^8 - 1 = 255$  equal intervals. Hence the smallest change in output voltage is (1/255) of the full scale output range. In short, the resolution is the value of the LSB.

$$\text{Resolution (in volts)} = \frac{V_{FS}}{2^n - 1} = 1 \text{ LSB increment} \quad (11.8)$$

However, resolution is stated in a number of different ways. An 8-bit DAC is said to have

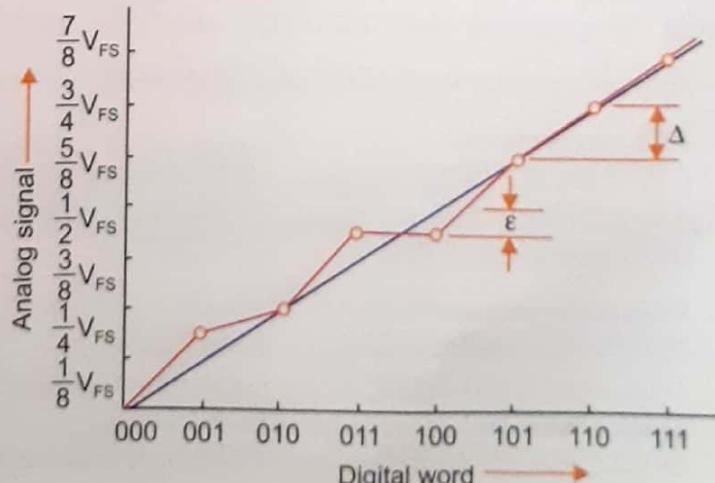
- : 8 bit resolution
- : a resolution of 0.392 of full-scale
- : a resolution of 1 part in 255

Similarly, the resolution of an A/D converter is defined as the smallest change in analog input for a one bit change at the output. As an example, the input range of an 8-bit A/D converter is divided into 255 intervals. So the resolution for a 10 V input range is 39.22 mV (= 10 V/255). Table 11.1 gives the resolution for 6–16 bit DACs.

**Table 11.1** Resolution for 6–16 bit DACs

Bits	Intervals	LSB size (% of Full Scale)	LSB size (10 V Full Scale)
6	63	1.588	158.8 mV
8	256	0.392	39.2 mV
10	1023	0.0978	9.78 mV
12	4095	0.0244	2.44 mV
14	16383	0.0061	0.61 mV
16	65535	0.0015	0.15 mV

**Linearity:** The linearity of an A/D or D/A converter is an important measure of its accuracy and tells us how close the converter output is to its ideal transfer characteristics. In an ideal DAC, equal increment in the digital input should produce equal increment in the analog output and the transfer curve should be linear. However, in an actual DAC, output voltages do not fall on a straight line because of gain and offset errors as shown by the solid line curve in Fig. 11.17. The static performance of a DAC is determined by fitting a straight line through the measured output points. The linearity error measures the deviation of the actual output from the fitted



**Fig. 11.17** Linearity error for 3-bit DAC

line and is given by  $\varepsilon/\Delta$  as shown in Fig. 11.17. The error is usually expressed as a fraction of LSB increment or percentage of full-scale voltage. A good converter exhibits a linearity error of less than  $\pm (1/2)$  LSB.

**Accuracy:** Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output. Relative accuracy is the maximum deviation after gain and offset errors have been removed. Data sheets normally specify relative accuracy rather than absolute accuracy. The accuracy of a converter is also specified in terms of LSB increments or percentage of full scale voltage.

**Monotonicity:** A monotonic DAC is the one whose analog output increases for an increase in digital input. Figure 11.18 represents the transfer curve for a non-monotonic DAC, since the output decreases when input code changes from 001 to 010. A monotonic characteristic is essential in control applications, otherwise oscillations can result. In successive approximation ADCs, a non-monotonic characteristic may lead to missing codes.

If a DAC has to be monotonic, the error should be less than  $\pm (1/2)$  LSB at each output level. All the commercially available DACs are monotonic because the linearity error never exceeds  $\pm (1/2)$  LSB at each output level.

**Settling time:** The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band  $\pm (1/2)$  LSB of its final value following a code change at the input (usually a full scale change). It depends upon the switching time of the logic circuitry due to internal parasitic capacitances and inductances. Settling time ranges from 100 ns to 10  $\mu$ s depending on word length and type of circuit used.

**Stability:** The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges.

A brief overview of ADC and DAC selection guide is given below:

#### A/D converters:

AD 7520/AD 7530	10-bit binary multiplying type
AD 7521/AD 7531	12-bit binary multiplying type
ADC 0800/0801/0802	8-bit ADC

#### D/A converters:

DAC 0800/0801/0802	8-bit DAC
DAC 0830/0831/0832	microprocessor compatible 8-bit DAC
DAC 1200/1201	12-bit DAC
DAC 1208/1209/1210	12-bit microprocessor compatible DAC

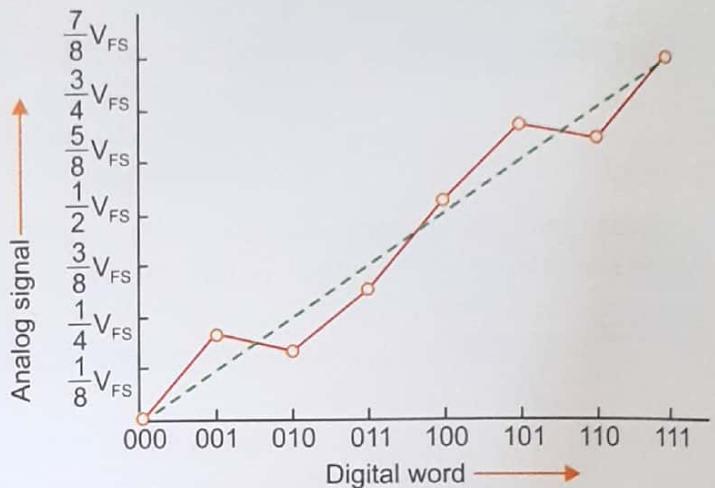


Fig. 11.18 A non-monotonic 3-bit DAC

### Example 11.10

We are familiar with 3½ digit digital voltmeter (DVM) and 4½ digit DVM which are being used regularly in the laboratory. Obviously 3½ digit DVM is less costly as its resolution is poor compared to 4½ digit DVM which is relatively costlier and have better resolution. Let us calculate the resolution of these DVMs.

### Solution

In 3½ digit DVM, the MSB can be either 0 or 1 whereas the 3 digit LSBs can be 000 to 999. Hence in 3½ digit DVM, the reading variation can be from 0000 to 1999, that is 2000. The reference voltage is 2 V. Hence the resolution is  $(2/2000)$  V = 1 mV; that is voltage variation below 1 mV is not detectable. Similarly, in 4½ digit DVM the total variation is from 0 0000 to 1 9999 and reference voltage is 2 V. Hence the resolution is  $(2/20000)$  V = 0.1 mV. Thus, the resolution of a 4½ digit DVM is ten times better than that of 3½ digit DVM.

### Example 11.11

Find the resolution and dynamic range of a D/A converter, if the maximum peak to peak output voltage is 5V and the input signal is a 10 bit word.

### Solution

The 10-bit word represents  $2^{10} = 1024$  levels. The step size is given by

$$= \frac{5V}{1024} = 4.88 \text{ mV}$$

Thus the system can identify input changes as low as 4.88 mv.

The dynamic range is the ratio of the largest value to the smallest value that can be converted. Therefore,

$$\begin{aligned}\text{Dynamic Range} &= \frac{5V}{4.88\text{mv}} \\ &= 1024\end{aligned}$$

The dynamic range is usually given in dBs, so  $20\log_{10}^{1024} = 60$  dB.

### SUMMARY

1. The output of a DAC can be either a voltage or current.
2. A multiplying DAC is the one in which the analog signal is allowed to vary.
3. Three resistive techniques for D/A conversion are: weighted resistor DAC, R-2R ladder and inverter R-2R ladder.
4. DAC essentially requires: resistors, electronics switches and an op-amp.
5. Two types of digitally controlled SPDT electronic switches are in use: a totem-pole MOSFET driver, a CMOS inverter.
6. A weighted resistor DAC requires a wide range of resistor values for better resolution whereas a R-2R ladder type DAC requires only two values of resistors.