9

555 TIMER

9.1 INTRODUCTION

The 555 timer is a highly stable device for generating accurate time delay or oscillation. Signetics Corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8-pin circular style, TO-99 can or 8-pin mini DIP or as 14-pin DIP. The 556 timer contains two 555 timers and is a 14-pin DIP. There is also available counter timer such as Exar's XR-2240 which contains a 555 timer plus a programmable binary counter in a single 16-pin package. A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

The 555 timer can be used with supply voltage in the range of + 5V to + 18V and can drive load upto 200 mA. It is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply voltage, the 555 timer is versatile and easy to use in various applications. Various applications include oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

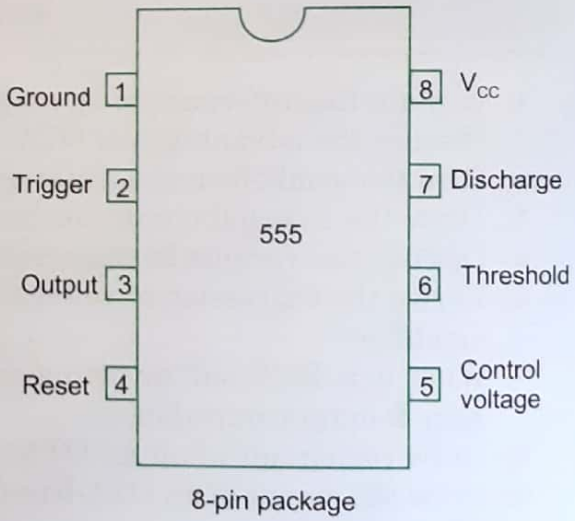

Fig. 9.1 Pin diagram

9.2 DESCRIPTION OF FUNCTIONAL DIAGRAM

Figure 9.1 gives the pin diagram and Fig. 9.2 gives the functional diagram for 555 IC timer. Referring to Fig. 9.2, three 5 kΩ internal resistors act as voltage divider, providing bias voltage of (2/3) V_{CC} to the upper comparator (UC) and (1/3) V_{CC} to the lower comparator (LC), where V_{CC} is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval. It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5). In applications, where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 μF) be connected between control voltage terminal (pin 5) and ground to by-pass noise or ripple from the supply.

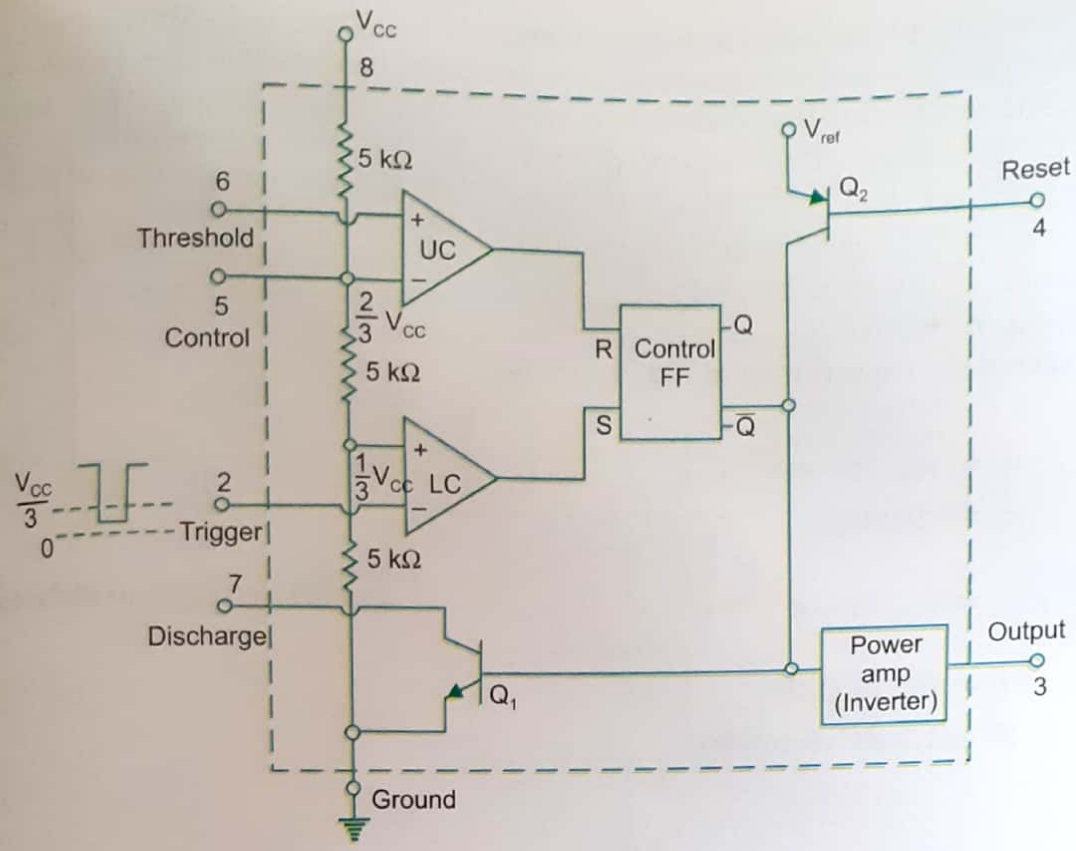

Fig. 9.2 Functional diagram of 555 timer

In the standby (stable) state, the output $\overline{Q}$ of the control flip-flop (FF) is HIGH. This makes the output LOW because of power amplifier which is basically an inverter. A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e. $V_{CC}/3$). At the negative going edge of the trigger, as the trigger passes through ($V_{CC}/3$), the output of the lower comparator goes HIGH and sets the FF ($Q = 1, \overline{Q} = 0$). During the positive excursion, when the threshold voltage at pin 6 passes through (2/3) V_{CC}, the output of the upper comparator goes HIGH and resets the FF ($Q = 0, \overline{Q} = 1$).

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset input is less than about 0.4 V. When this reset is not used, it is returned to V_{CC}. The transistor Q_2 serves as a buffer to isolate the reset input from the FF and transistor Q_1. The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{CC}.

9.3 MONOSTABLE OPERATION

Figure 9.3 shows a 555 timer connected for monostable operation and its functional diagram is shown in Fig. 9.4. In the standby state, FF holds transistor Q_1 ***on***, thus clamping the external timing capacitor C to ground. The output remains at ground potential, i.e. LOW. As the trigger passes through $V_{CC}/3$, the FF is set, i.e. $\overline{Q} = 0$. This makes the transistor Q_1 ***off*** and the short circuit across the timing capacitor C is released. As $\overline{Q}$ is LOW, output goes HIGH (= V_{CC}). The timing cycle now begins. Since C is unclamped, voltage across it rises exponentially through R towards V_{CC} with a time constant RC as in Fig. 9.5 (b). After

a time period T (calculated later), the capacitor voltage is just greater than (2/3) V_{CC} and the upper comparator resets the FF, that is, $R = 1$, $S = 0$ (assuming very small trigger pulse width). This makes $\overline{Q} = 1$, transistor Q_1 goes **on** (i.e. saturates), thereby discharging the capacitor C rapidly to ground potential. The output returns to the standby state or ground potential as shown in Fig. 9.5 (c).

The voltage across the capacitor as in Fig. 9.5 (b) is given by

$$v_c = V_{CC}\,(1 - e^{-t/RC}) \qquad (9.1)$$

At $t = T$, $\quad v_c = (2/3)\,V_{CC}$

Therefore, $\dfrac{2}{3}V_{CC} = V_{CC}\,(1 - e^{-T/RC})$

or, $\quad T = RC \ln (1/3)$

or, $\quad T = 1.1\,RC$ (seconds) $\qquad (9.2)$

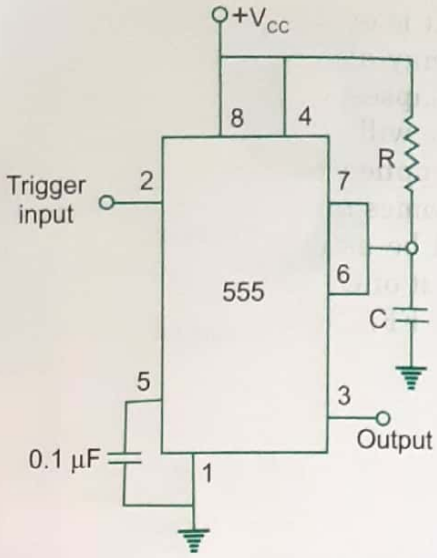

Fig. 9.3 Monostable multivibrator

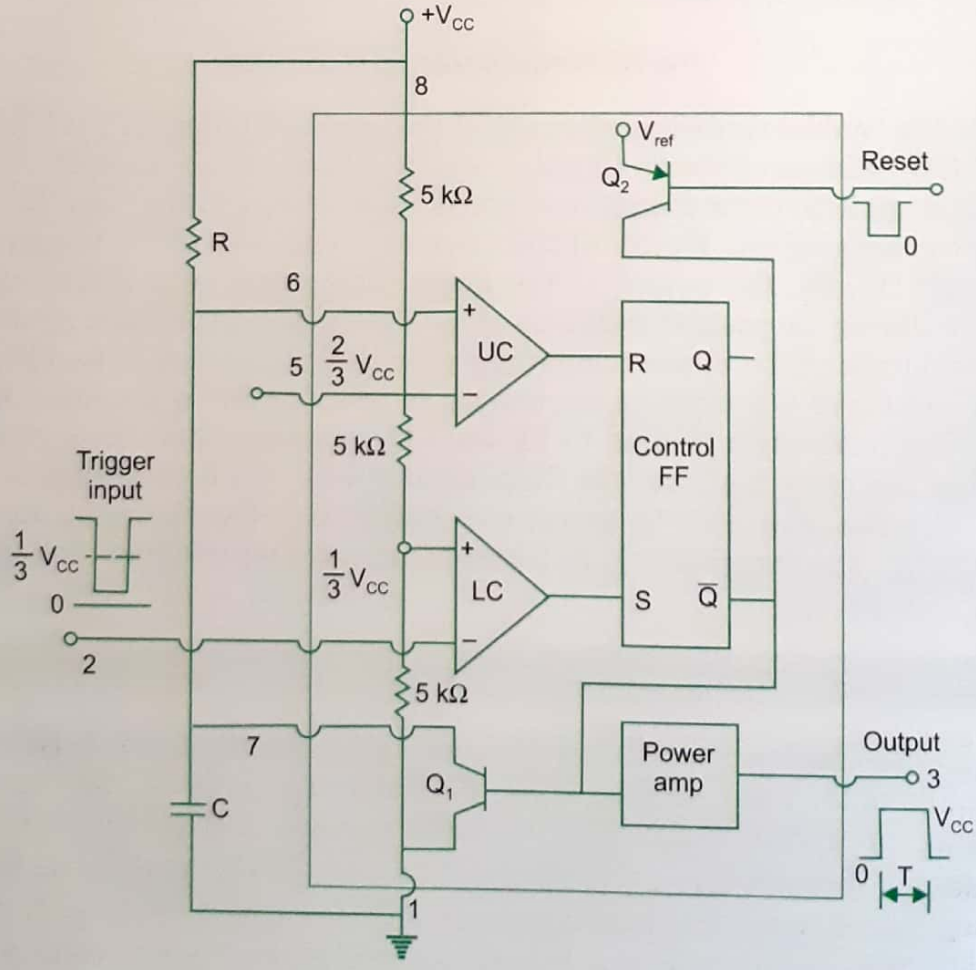

Fig. 9.4 Timer in monostable operation with functional diagram

It is evident from Eq. (9.2) that the timing interval is independent of the supply voltage. It may also be noted that once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state. However, if a negative going reset pulse as in Fig. 9.5(d) is applied to the reset terminal (pin-4) during the timing cycle, transistor Q_2 goes ***off***, Q_1 becomes ***on*** and the external timing capacitor C is immediately discharged. The output now will be as in Fig. 9.5 (e). It may be seen that the output of Q_2 is connected directly to the input of Q_1 so as to turn ***on*** Q_1 immediately and thereby avoid the propagation delay through the FF. Now, even if the reset is released, the output will still remain LOW until a negative going trigger pulse is again applied at pin 2. Figure 9.6 shows a graph of the various combinations of R and C necessary to produce a given time delay.

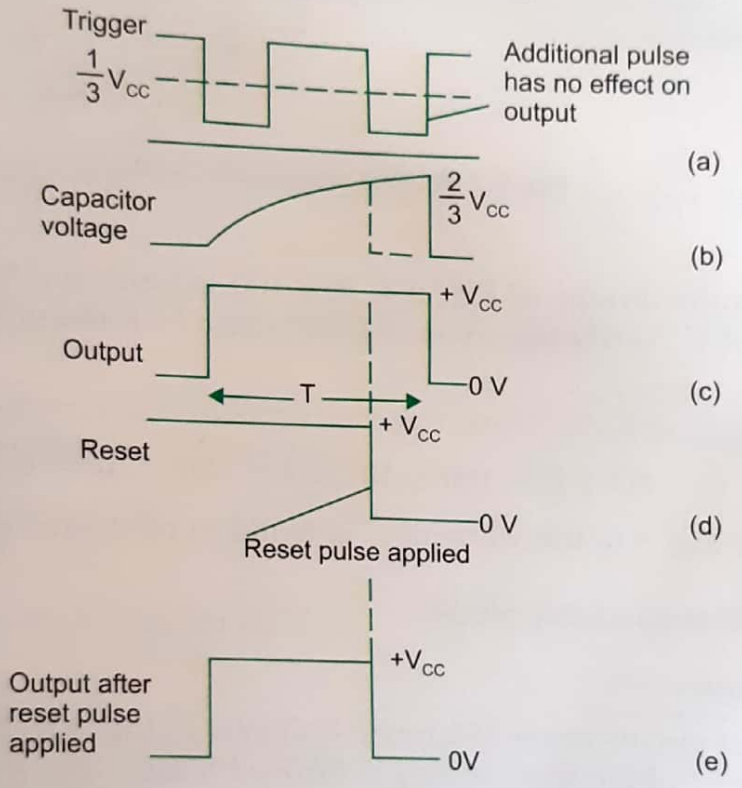

Fig. 9.5 Timing pulses

Sometimes the monostable circuit of Fig. 9.3 mistriggers on positive pulse edges, even with the control pin by pass capacitor. To prevent this, a modified circuit as shown in Fig. 9.7 is used. Here the resistor and capacitor combination of 10 kΩ and 0.001 μF at the input forms a differentiator. During the positive going edge of the trigger, diode D becomes forward biased, thereby limiting the amplitude of the positive spike to 0.7 V.

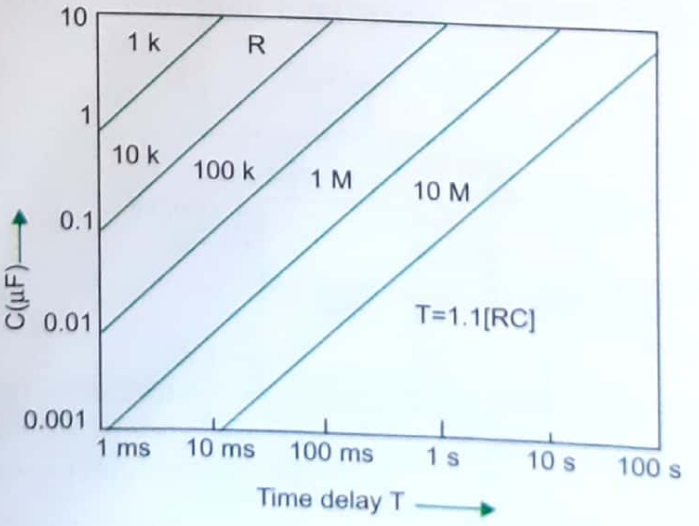

Fig. 9.6 Graph of *RC* combinations for different time delays

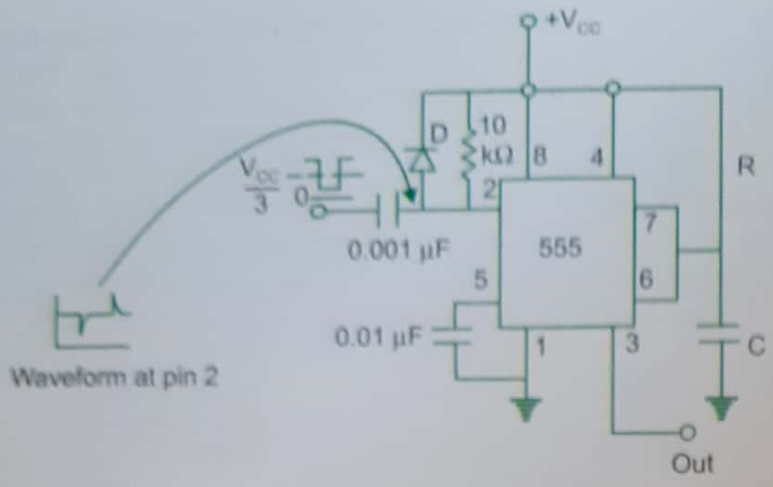

Fig. 9.7 Modified monostable circuit

Example 9.1

In the monostable multivibrator of Fig. 9.3, $R = 100$ kΩ and the time delay $T = 100$ mS. Calculate the value of C. Verify the value of C obtained from the graphs of Fig. 9.6.

Solution

From Eq. (9.2), we get

$$C = T/1.1\ R = 100 \times 10^{-3}/1.1 \times 100 \times 10^{3} = 0.9\ \mu F$$

From the graph of Fig. 9.6, the value of C is found to be 0.9 μF also.

9.3.1 Applications in Monostable Mode

Missing Pulse Detector

Missing pulse detector circuit using 555 timer is shown in Fig. 9.8. Whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~ 0.7 V). The output of the timer goes HIGH. The circuit is designed so that the time period of the monostable circuit is slightly greater (1/3 longer) than that of the triggering pulses. So long the trigger pulse train keeps coming at pin 2, the output remains HIGH. However, if a pulse misses, the trigger input is high and transistor Q is cut

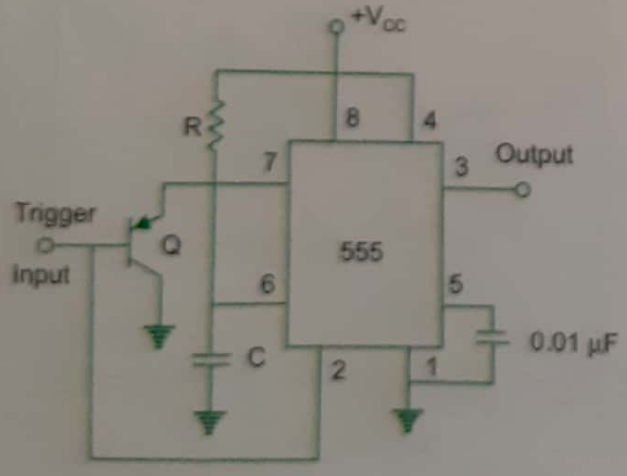

Fig. 9.8 A missing pulse detector monostable circuit

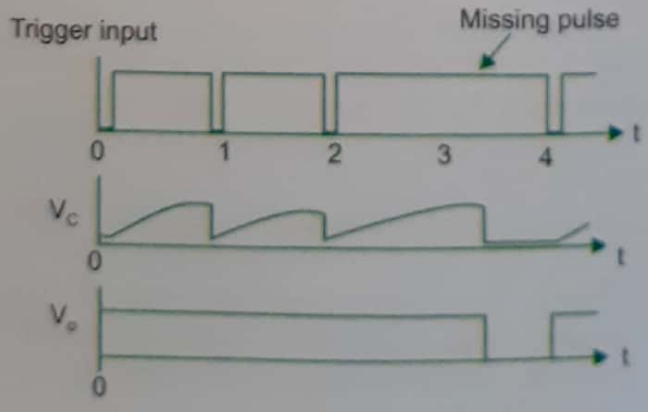

Fig. 9.9 Output of missing pulse detector

off. The 555 timer enters into normal state of monostable operation. The output goes LOW after time T of the mono-shot. Thus this type of circuit can be used to detect missing heartbeat. It can also be used for speed control and measurement. If input trigger pulses are generated from a rotating wheel, the circuit tells when the wheel speed drops below a predetermined value.

Linear Ramp Generator

Linear ramp can be generated by the circuit shown in Fig. 9.10. The resistor R of the monostable circuit is replaced by a constant current source. The capacitor is charged linearly by the constant current source formed by the transistor Q_3. The capacitor voltage v_c can be written as

$$v_c = \frac{1}{C}\int_0^t i\,dt \tag{9.3}$$

where i is the current supplied by the constant current source. Further, the KVL equation can be written as

$$\frac{R_1}{R_1 + R_2}\,V_{CC} - V_{BE} = (\beta + 1)I_B R_E \approx \beta I_B R_E = I_C R_E = iR_E \tag{9.4}$$

where I_B, I_C are the base current and collector current respectively, β is the current amplification factor in CE-mode and is very high. Therefore,

$$i = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2)} \tag{9.5}$$

Now putting the value of the current i in Eq. 9.3, we get

$$v_c = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{C\,R_E(R_1 + R_2)} \times t \tag{9.6}$$

At time $t = T$, the capacitor voltage v_c becomes (2/3) V_{CC}. Then we get

$$\frac{2}{3}V_{CC} = \frac{R_1 V_{CC} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2)C} \times T \tag{9.7}$$

which gives the time period of the linear ramp generator as

$$T = \frac{(2/3)\,V_{CC}\,R_E\,(R_1 + R_2)C}{R_1 V_{CC} - V_{BE}\,(R_1 + R_2)} \tag{9.8}$$

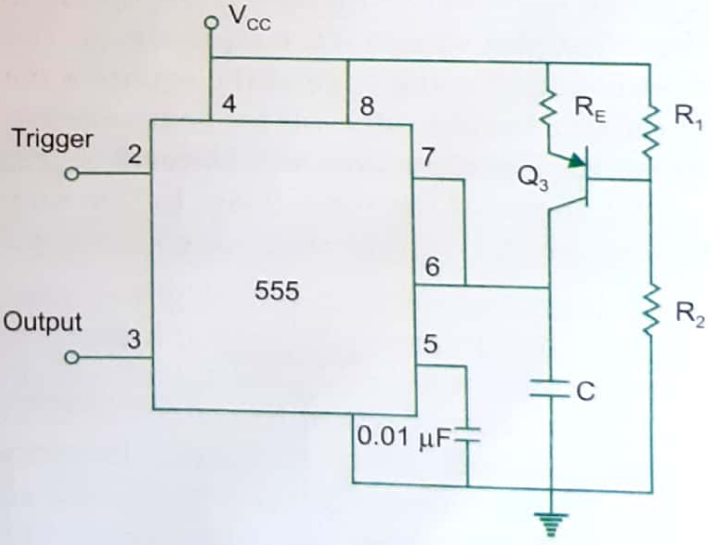

Fig. 9.10 Linear ramp generator

The capacitor discharges as soon as its voltage reaches (2/3) V_{CC} which is the threshold of the upper comparator in the monostable circuit functional diagram. The capacitor voltage remains zero till another trigger is applied. The various waveforms are shown in Fig. 9.11.

The practical values can be noted as

$R_1 = 47\ \text{k}\Omega$; $R_2 = 100\ \text{k}\Omega$; $R_E = 2.7\ \text{k}\Omega$; $C = 0.1\ \mu\text{F}$.
$V_{CC} = 5\ \text{V}$ (any value between 5 to 18 V can be chosen)

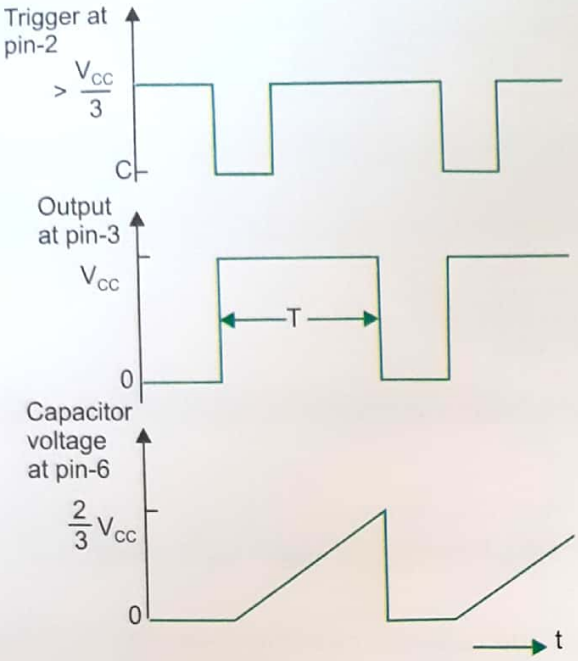

Fig. 9.11 Linear ramp generator output

Frequency Divider

A continuously triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal. The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH (because of greater timing interval) for next negative going edge of the input square wave as shown in Fig. 9.12. The mono-shot will however be triggered on the third negative going input, depending on the choice of the time delay. In this way, the output can be made integral fractions of the frequency of the input triggering square wave.

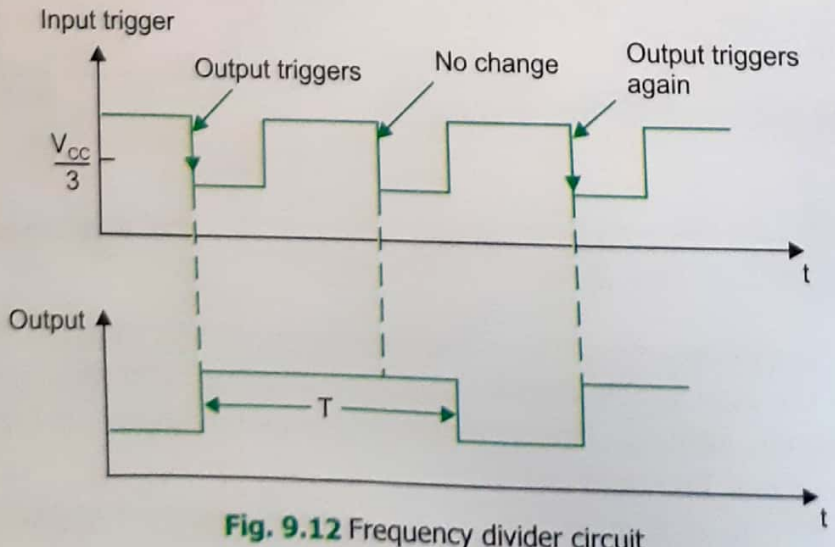

Fig. 9.12 Frequency divider circuit

Pulse Width Modulation

The circuit is shown in Fig. 9.13. This is basically a monostable multivibrator with a modulating input signal applied at pin-5. By the application of continuous trigger at pin-2, a series of output pulses are obtained, the duration of which depends on the modulating input at pin-5. The modulating signal applied at pin-5 gets superimposed upon the already existing voltage (2/3) V_{CC} at the inverting input terminal of UC. This in turn changes the threshold level of UC and the output pulse width modulation takes place. The modulating signal and the output waveform are shown in Fig. 9.14. It may be noted from the output waveform that the pulse duration, that is, the duty cycle only varies, keeping the frequency same as that of the continuous input pulse train trigger.

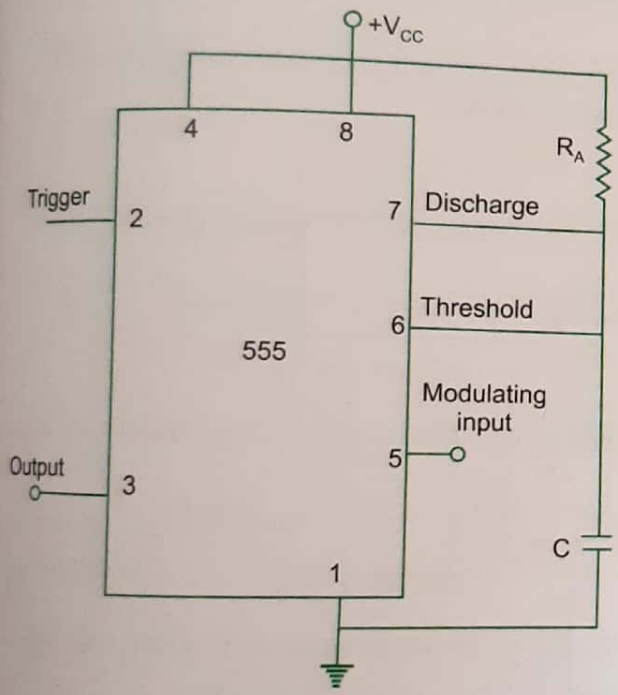

Fig. 9.13 Pulse width modulator

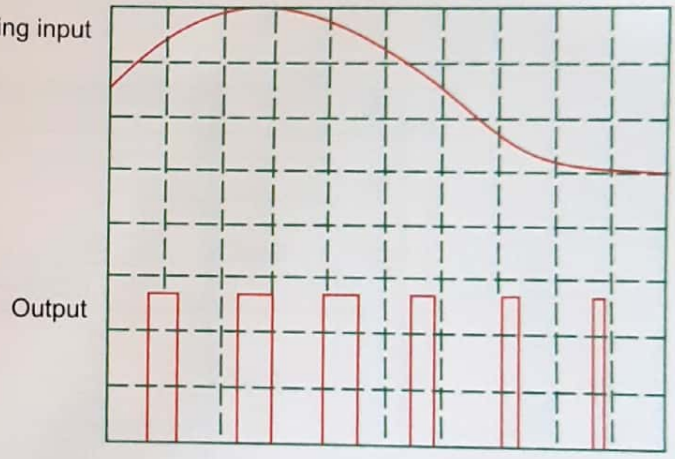

Fig. 9.14 Pulse width modulator waveforms

9.4 ASTABLE OPERATION

The device is connected for astable operation as shown in Fig. 9.15. For better understanding, the complete diagram of astable multivibrator with detailed internal diagram of 555 is shown in Fig. 9.16. Comparing with monostable operation, the timing resistor is now split into two sections R_A and R_B. Pin 7 of discharging transistor Q_1 is connected to the junction of R_A and R_B. When the power supply V_{CC} is connected, the external timing capacitor C charges towards V_{CC} with a time constant $(R_A + R_B)C$. During this time, output (pin 3) is high (equals V_{CC}) as Reset $R = 0$, Set $S = 1$ and this combination makes $\overline{Q} = 0$ which has unclamped the timing capacitor C.

When the capacitor voltage equals (to be precise is just greater than), (2/3) V_{CC} the upper comparator triggers the control flip-flop so that $\overline{Q} = 1$. This, in turn, makes transistor Q_1 ***on*** and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant R_BC (neglecting the forward resistance of Q_1). Current also flows into transistor Q_1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1. The minimum value of R_A is approximately equal to $V_{CC}/0.2$ where 0.2 A is the maximum current through the ***on*** transistor Q_1.

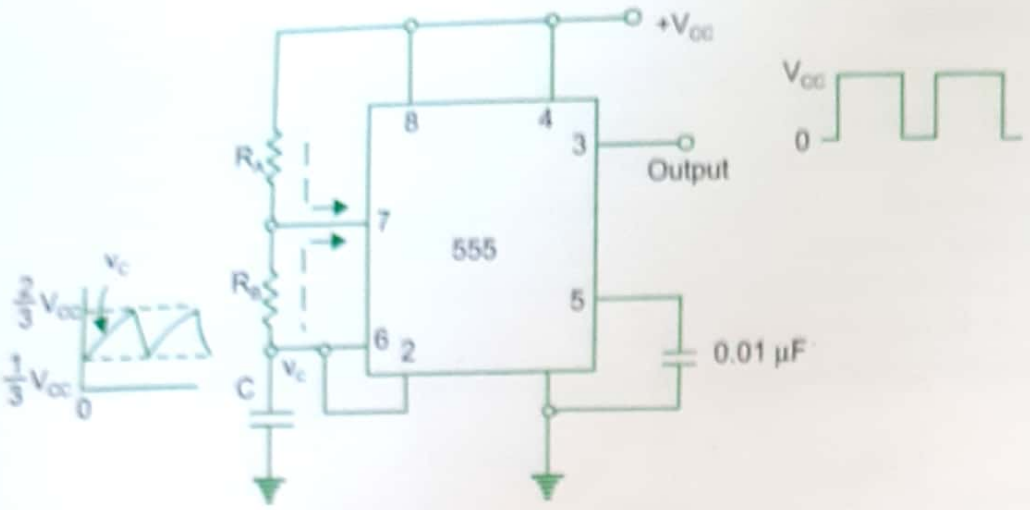

Fig. 9.15 Astable multivibrator using 555 timer

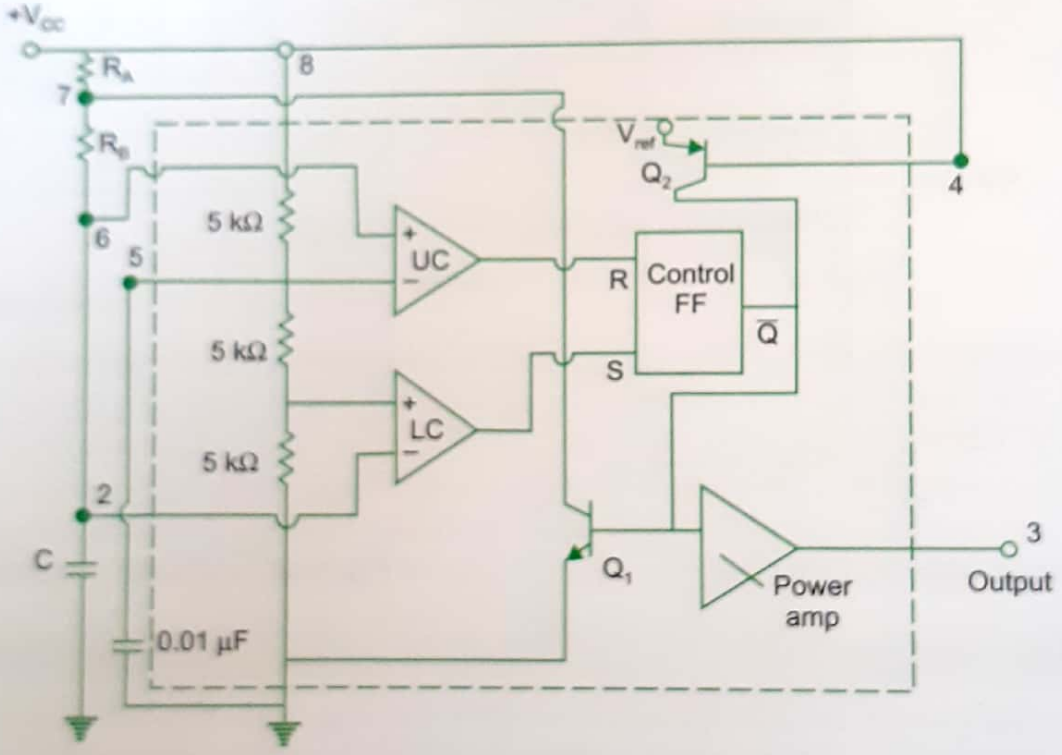

Fig. 9.16 Functional diagram of astable multivibrator using 555 timer

During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) $V_{CC}/3$, the lower comparator is triggered and at this stage $S = 1$, $R = 0$, which turns $\overline{Q} = 0$. Now $\overline{Q} = 0$ unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between (2/3) V_{CC} and (1/3) V_{CC} respectively. Figure 9.17 shows the timing sequence and capacitor voltage wave form. The length of time that the output remains HIGH is the time for the capacitor to charge from (1/3) V_{CC} to (2/3) V_{CC}. It may be calculated as follows:

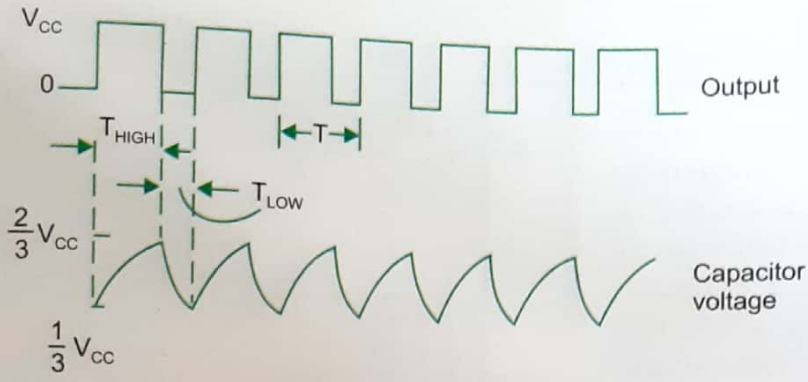

Fig. 9.17 Timing sequence of astable multivibrator

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{CC} volts is given by

$$v_c = V_{CC}(1 - e^{-t/RC})$$

The time t_1 taken by the circuit to charge from 0 to (2/3) V_{CC} is,

$$(2/3)\,V_{CC} = V_{CC}(1 - e^{-t_1/RC}) \tag{9.9}$$

or, $$t_1 = 1.09\,RC$$

and the time t_2 to charge from 0 to (1/3) V_{CC} is,

$$(1/3)\,V_{CC} = V_{CC}(1 - e^{-t_2/RC}) \tag{9.10}$$

or, $$t_2 = 0.405\,RC$$

So the time to charge from (1/3) V_{CC} to (2/3) V_{CC} is

$$t_{HIGH} = t_1 - t_2$$
$$t_{HIGH} = 1.09\,RC - 0.405\,RC = 0.69\,RC$$

So, for the given circuit,

$$t_{HIGH} = 0.69\,(R_A + R_B)C \tag{9.11}$$

The output is low while the capacitor discharges from (2/3) V_{CC} to (1/3) V_{CC} and the voltage across the capacitor is given by

$$(1/3)\,V_{CC} = (2/3)V_{CC}\,e^{-t/RC}$$

Solving, we get $$t = 0.69\,RC$$

So, for the given circuit, $t_{LOW} = 0.69\,R_BC$ (9.12)

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or,
$$T = 0.69\,(R_A + 2R_B)\,C$$

So,
$$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \tag{9.13}$$

Figure 9.18 shows a graph of the various combinations of $(R_A + 2R_B)$ and C necessary to produce a given stable output frequency. The duty cycle D of a circuit is defined as the ratio of ON time to the total time period $T = (t_{ON} + t_{OFF})$. In this circuit, when the transistor Q_1 is ***on***, the output goes low. Hence,

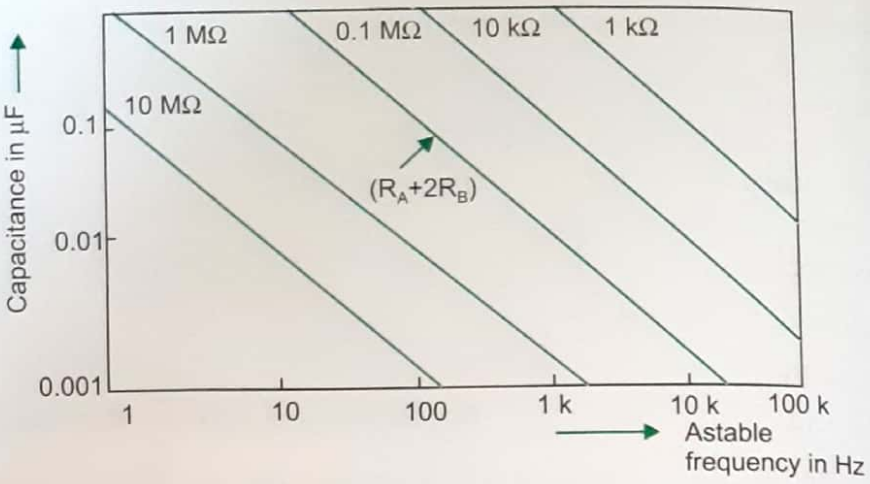

Fig. 9.18 Frequency dependence of R_A, R_B and C

$$D\% = \frac{t_{LOW}}{T} \times 100$$

$$= \frac{R_B}{R_A + 2R_B} \times 100 \qquad (9.14)$$

With the circuit configuration of Fig. 9.15 it is not possible to have a duty cycle more than 50% since $t_{HIGH} = 0.69\ (R_A + R_B)\ C$ will always be greater than $t_{LOW} = 0.69\ R_B\ C$. In order to obtain a symmetrical square wave i.e. $D = 50\%$, the resistance R_A must be reduced to zero. However, now pin 7 is connected directly to V_{CC} and extra current will flow through Q_1 when it is ***on***. This may damage Q_1 and hence the timer.

An alternative circuit which will allow duty cycle to be set at practically any level is shown in Fig. 9.19. During the charging portion of the cycle, diode D_1 is forward biased effectively short circuiting R_B so that

$$t_{HIGH} = 0.69\ R_A C$$

However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

So $$t_{LOW} = 0.69\ R_B\ C \qquad (9.15)$$

$$T = t_{HIGH} + t_{LOW} = 0.69\ (R_A + R_B)\ C \qquad (9.16)$$

or, $$f = \frac{1.45}{(R_A + R_B)C} \qquad (9.17)$$

and duty cycle $D = \dfrac{R_B}{R_A + R_B}$

Resistors R_A and R_B could be made variable to allow adjustment of frequency and pulse width. However, a series resistor of atleast 100 Ω (fixed) should be added to each R_A and R_B. This will limit peak current to the discharge transistor Q_1 when the variable resistors are at minimum value. And, if R_A is made equal to R_B, then 50% duty cycle is achieved.

Symmetrical square wave generator by adding a clocked JK flip-flop to the output of the nonsymmetrical square wave generator is

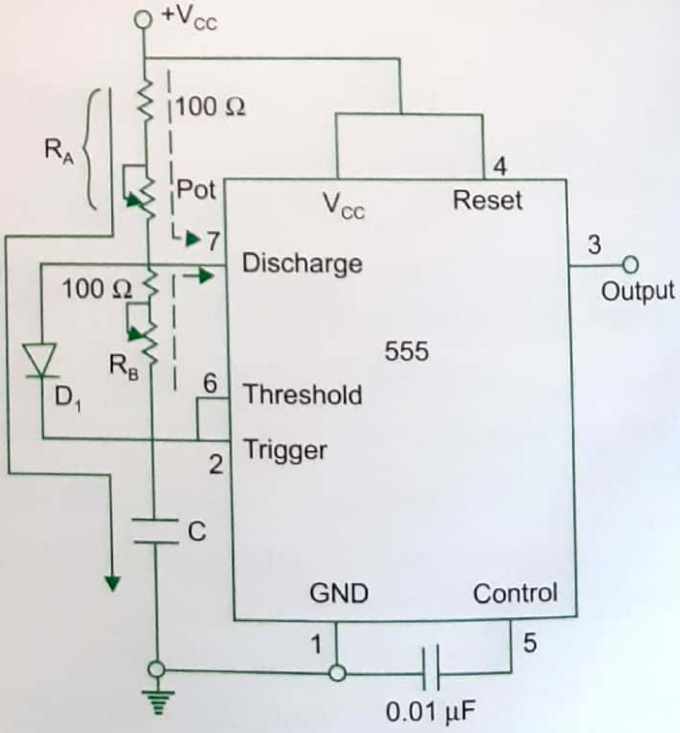

Fig. 9.19 Adjustable duty cycle rectangular wave generator

shown in Fig. 9.20. The clocked flip-flop acts as binary divider to the timer output. The output frequency in this case will be one half that of the timer. The advantage of this circuit is of having output of 50% duty cycle without any restriction on the choice of R_A and R_B.

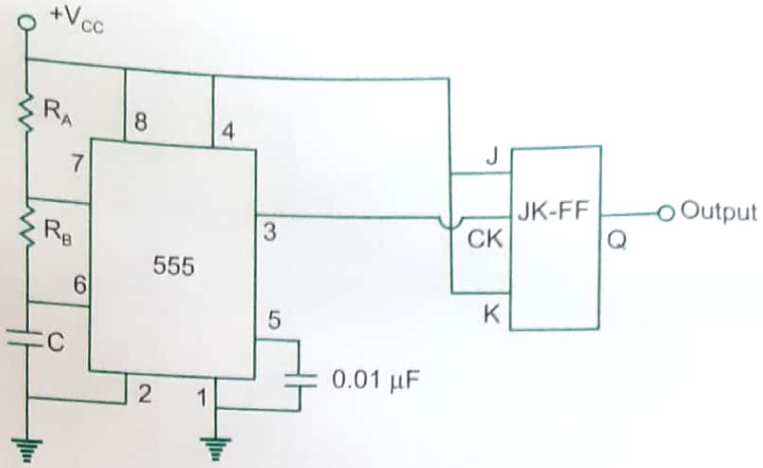

Fig. 9.20 Symmetrical waveform generator

Example 9.2

Refer Fig. 9.15. For $R_A = 6.8\ k\Omega$, $R_B = 3.3\ k\Omega$ and $C = 0.1\ \mu F$, calculate (a) t_{HIGH} (b) t_{LOW} (c) free running frequency (d) duty cycle, D.

Solution

(a) By Eq. (9.11)

$$t_{HIGH} = 0.69\,(6.8\ k\Omega + 3.3\ k\Omega)\,(0.1\ \mu F) = 0.7\ ms$$

(b) By Eq. (9.12)

$$t_{LOW} = 0.69\,(3.3\ k\Omega)\,(0.1\ \mu F) = 0.23\ ms$$

(c) $$f = \frac{1.45}{[(6.8\ k\Omega) + (2)(3.3\ k\Omega)](0.1\ \mu F)} = 1.07\ kHz$$

(d) $$D = \frac{t_{LOW}}{T} = \frac{R_B}{R_A + 2R_B}$$

$$= \frac{3.3\ k\Omega}{6.8\ k\Omega + 2(3.3\ k\Omega)} = 0.25 \text{ or, } 25\%$$

9.4.1 Applications in Astable Mode

FSK Generator

In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique. A 555 timer in astable mode can be used to generate FSK signal. The circuit is as shown in Fig. 9.21. The standard digital data input frequency is 150 Hz. When input is HIGH, transistor Q is ***off*** and 555 timer works in the normal astable mode of operation. The frequency of the output waveform given by Eq. (9.1) can be rewritten as

$$f_o = \frac{1.45}{(R_A + 2R_B)C} \qquad (9.18)$$

In a tele-typewriter using a modulator-demodulator (MODEM), a frequency between 1070 Hz to 1270 Hz is used as one of the standard FSK signals. The components R_A and R_B and the capacitor C can be selected so that f_o is 1070 Hz.

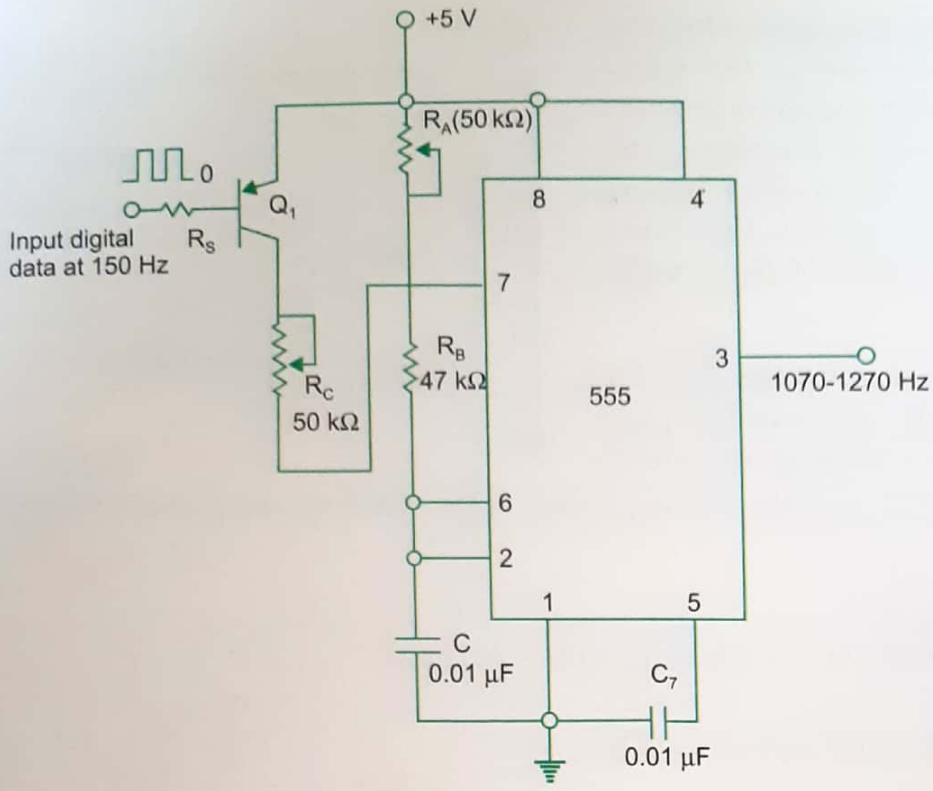

Fig. 9.21 FSK generator

When the input is LOW, Q goes ***on*** and connects the resistance R_C across R_A. The output frequency is now given by

$$\frac{1.45}{(R_A \parallel R_C) + 2R_B} \tag{9.19}$$

The resistance R_C can be adjusted to get an output frequency 1270 Hz.

Pulse-Position Modulator

The pulse-position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation as shown in Fig. 9.22. The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.

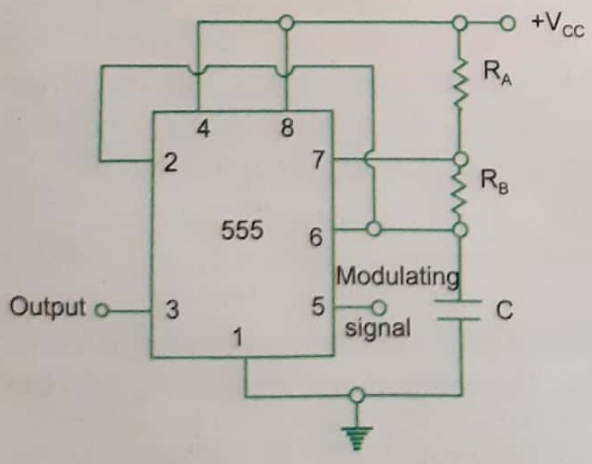

Fig. 9.22 Pulse position modulator

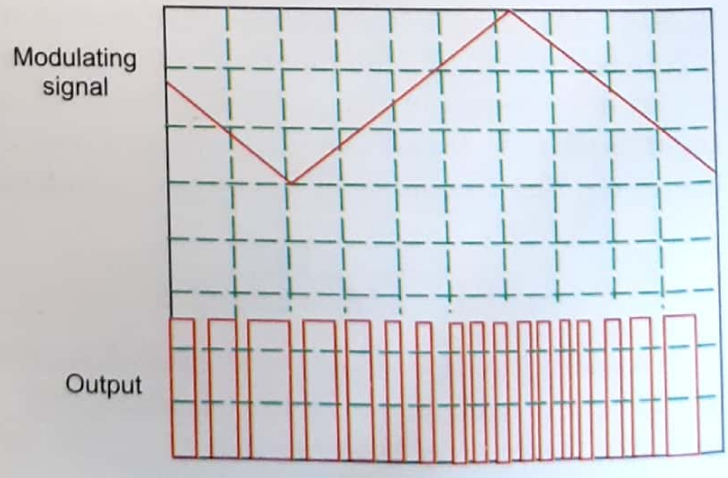

Fig. 9.23 Pulse position modulator output

Figure 9.23 shows the output waveform generated for a triangle wave modulation signal. It may be noted from the output waveform that the frequency is varying leading to pulse position modulation. The typical practical component values may be noted as

$R_A = 3.9\ k\Omega$, $R_B = 3\ k\Omega$, $C = 0.01\ \mu F$

$V_{CC} = 5$ V (any value between 5 V to 18 V may be chosen)

9.5 SCHMITT TRIGGER

The use of 555 timer as a Schmitt Trigger is shown in Fig. 9.24. Here the two internal comparators are tied together and externally biased at $V_{CC}/2$ through R_1 and R_2. Since the upper comparator will trip at (2/3) V_{CC} and lower comparator at (1/3) V_{CC}, the bias provided by R_1 and R_2 is centered within these two thresholds.

Thus, a sine wave of sufficient amplitude ($> V_{CC}/6 = 2/3\ V_{CC} - V_{CC}/2$) to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave output as shown in Fig. 9.25.

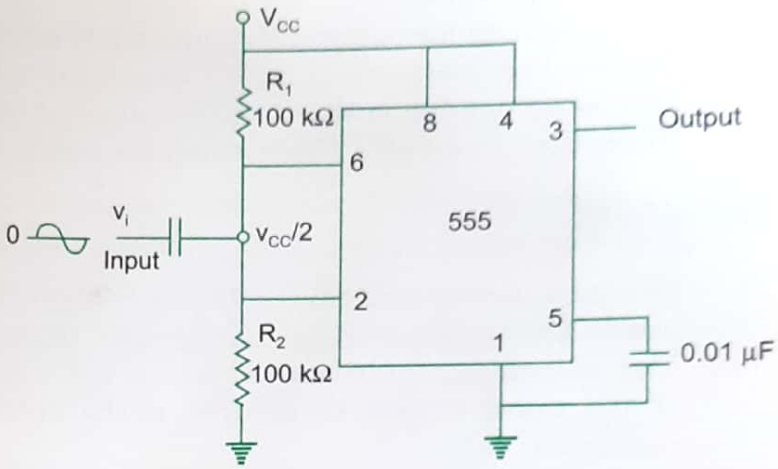

Fig. 9.24 Timer in Schmitt Trigger Operation

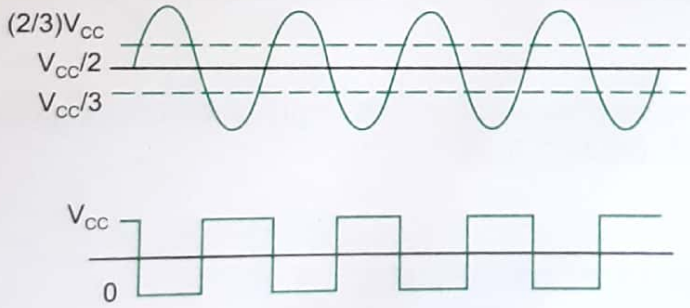

Fig. 9.25 Input output waveforms of Schmitt Trigger

It may be noted that unlike conventional multivibrator, no frequency division is taking place and frequency of square wave remains the same as that of input signal.

SUMMARY

1. 555 IC Timer can produce very accurate and stable time delays, from microseconds to hours.
2. Timer is available in two packages, circular can and DIP.
3. It can be used with supply voltage varying from 5 to 18 V and thus is compatible with TTL and CMOS circuits.
4. Timer can be used in monostable or astable mode of operation. Its various applications include waveform generator, missing pulse detector, frequency divider, pulse width modulator, burglar alarm, FSK generator, ramp generator, pulse position modulator etc.