

EC19441 – ANALOG CIRCUITS – II

UNIT-I

OPERATIONAL AMPLIFIER AND ITS CHARACTERISTICS:

Introduction, ideal op-amp, Op-amp-internal circuit, DC and AC characteristics, slew rate, frequency compensation techniques.

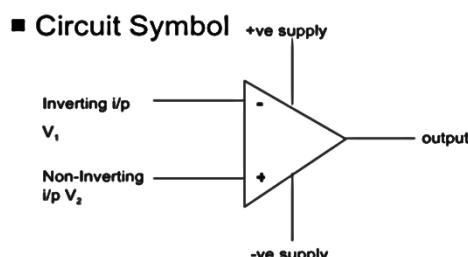
OPERATIONAL AMPLIFIER:

An operational amplifier is a direct-coupled, high gain amplifier consisting of one or more differential amplifier. By properly selecting the external components, it can be used to perform a variety of mathematical operations.

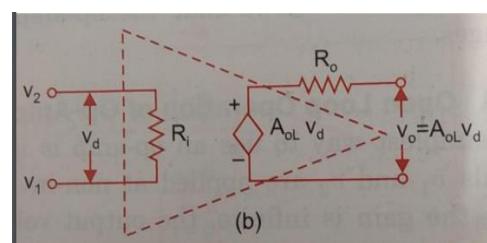
Ideal characteristics of op-amp:

1. Open loop voltage gain $A_{OL} = \infty$ (infinity)
2. Input impedance $R_i = \infty$ (infinity)
3. Output impedance $R_o = 0$ (zero)
4. Zero offset i.e., ($V_o = 0$ when $V_1 = V_2 = 0$)
5. Band width BW = ∞ (infinity)

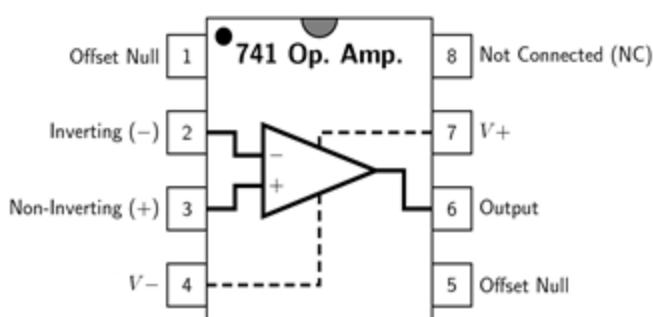
Operational Amplifier Symbol



EQUIVALENT CIRCUIT OF OPAMP:



PIN DIAGRAM OF IC741:



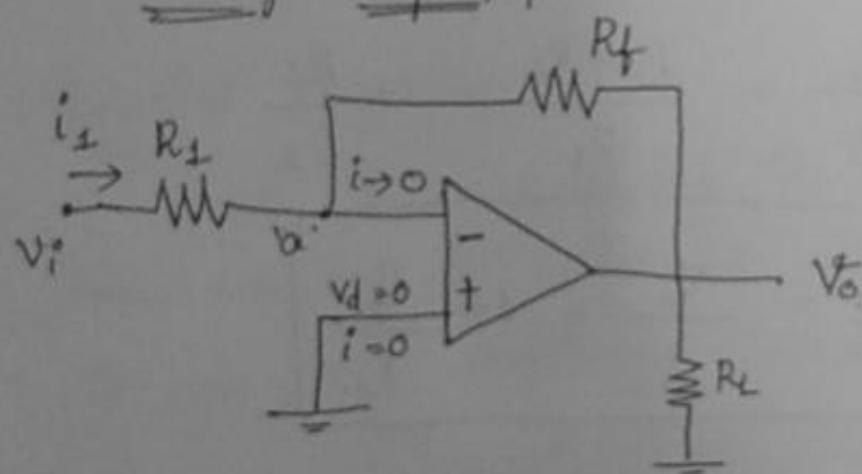
Ideal Op-amp:

- (i) Input impedance $\rightarrow \infty$ then no current at both the terminals.
- (ii) Gain $\rightarrow \infty$, so $V_d = (V_1 - V_2) = 0$.
 - (iii) $V_1 = V_2$.

Feedback in ideal op-amp:

Negative feedback \rightarrow Gain \uparrow .

Inverting Amplifier:



$R_f \rightarrow$ feedback Resistor

$R_1 \rightarrow$ S/P Resistor

Analysis:

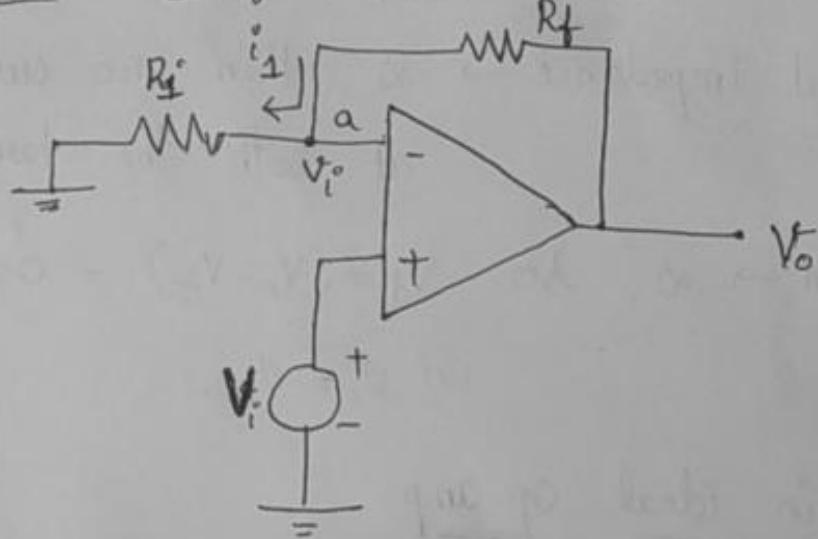
For ideal op-amp, $V_d = 0$; then

$$i_1 = \frac{V_i}{R_1}$$

$$V_o = -i_1 R_f = -\frac{V_i}{R_1} R_f$$

$$\therefore \text{Gain}(A_{cl}) = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

(2) Non-Inverting Amplifier:



Here,

$$V_{i^*} = \frac{V_o}{R_i + R_f} R_i$$

Then $\frac{V_o}{V_i} = \frac{R_i + R_f}{R_i} = 1 + \frac{R_f}{R_i}$

Gain $A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}$

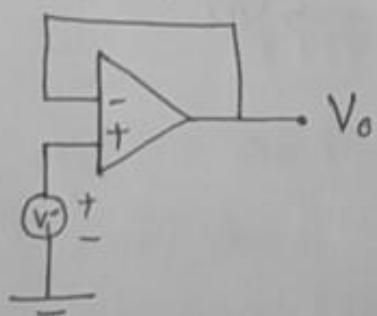
(3) Voltage follower:

* In an non-inverting amplifier, if $R_f = 0 \Omega$ & $R_i = \infty$, we get the Voltage follower circuit.

Here

$$V_o = V_i$$

* The output voltage is equal to the input voltage both in magnitude and phase.



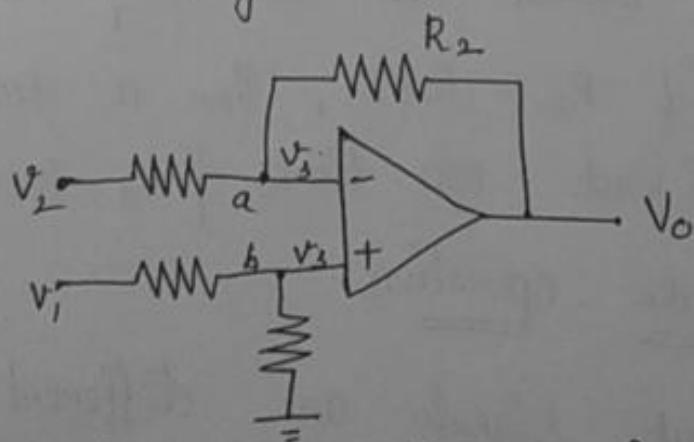
* Unity gain circuit $\rightarrow R_i \uparrow$; $R_o = 0$

* used as a buffer for impedance matching.

(4) Differential Amplifier:

* A circuit that amplifies the difference between two signals is called a differential amplifier.

* It is very useful in instrumentation circuits.



The nodal equation at 'a', is

$$\frac{V_3 - V_2}{R_1} + \frac{V_3 - V_o}{R_2} = 0 \rightarrow ①$$

The nodal equation at b,

$$\frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0 \rightarrow \textcircled{2}$$

Eqn. ① & ② is re-written as,

$$\left(\frac{1}{R_1} + \frac{1}{R_2} \right) V_3 - \frac{V_2}{R_1} = \frac{V_o}{R_2} \rightarrow \textcircled{3}$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2} \right) V_3 - \frac{V_1}{R_1} = 0 \rightarrow \textcircled{4}$$

Subtracting ④ from ③, we get

$$\frac{1}{R_1} (V_1 - V_2) = \frac{V_o}{R_2}$$

$$\therefore V_o = \frac{R_2}{R_1} (V_1 - V_2)$$

* This circuit is useful in detecting very small differences in signals, the gain (R_2/R_1) can be chosen to be very large.

* For eg:- if $R_2 = 100R_1$, then a small difference is amplified 100 times [$V_o = 100(V_1 - V_2)$].

Differential Mode operation:

* Two input signals are different.

$$V_d = V_1 - V_2.$$

$$A_{DH} = \frac{1}{2} (A_1 - A_2)$$

Common-mode operation:

- * Two input signals are same, then ideally $V_o = 0$, but in practical,

$$V_{cm} = \frac{V_1 + V_2}{2}$$

$$A_{CH} = A_1 + A_2$$

Common-Mode Rejection Ratio (CMRR):

- * The relative sensitivity of an op-amp to a difference signal as compared to a common-mode signal is called CMRR.

$$CMRR = \left| \frac{A_{DM}}{A_{CH}} \right|$$

where $A_{DM} \rightarrow$ Differential mode gain
 $A_{CH} \rightarrow$ Common mode gain.

INTERNAL CIRCUIT OF Op-AMP:

- * Commercial IC op-amps usually consists of four cascaded blocks \Rightarrow refer fig. given below.
- * The First two stages are cascaded differential amplifier and are designed to provide high gain and high input resistance.
- * The Third stage acts as a buffer as well as a level shifter. The buffer is usually an emitter follower whose input impedance is very high so that it prevents loading of the high gain stage.
- * The Level shifter adjusts the dc.voltages so that output voltage is zero for zero inputs, thus zero offset condition.
- * The output stage is designed to provide a low output impedance as demanded by the ideal op-amp characteristics.

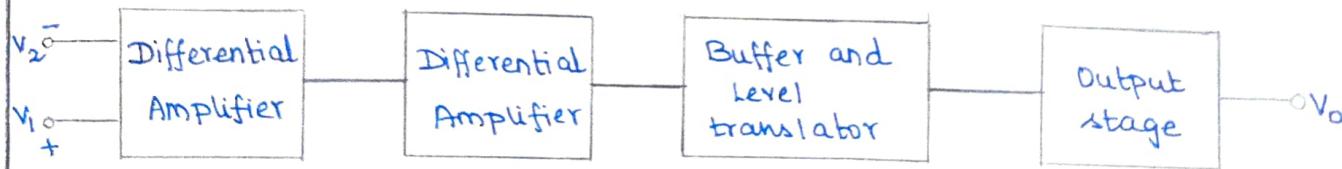


Fig. Shows the Block schematic of an op-amp

DIFFERENTIAL AMPLIFIER:

- * The main purpose of the differential amplifier stage is to provide high gain to the difference-mode signal and cancel the common-mode signal.
- * It is able to suppress any undesired noise which is common to both of the input terminals.

CMRR definition and its importance:-

- * The relative sensitivity of an op-amp to a difference signal as compared to common-mode signal is called common-mode rejection ratio (CMRR) and gives the figure of merit of the differential amplifier.
- * The higher the value of CMRR, better is the op-amp.
- * Another requisite of a good op-amp is that it should have high input impedance.

$$CMRR = \left| \frac{A_d}{A_c} \right| ; \text{ no unit}$$

where,

$A_d \rightarrow$ differential mode gain

$A_c \rightarrow$ common mode gain

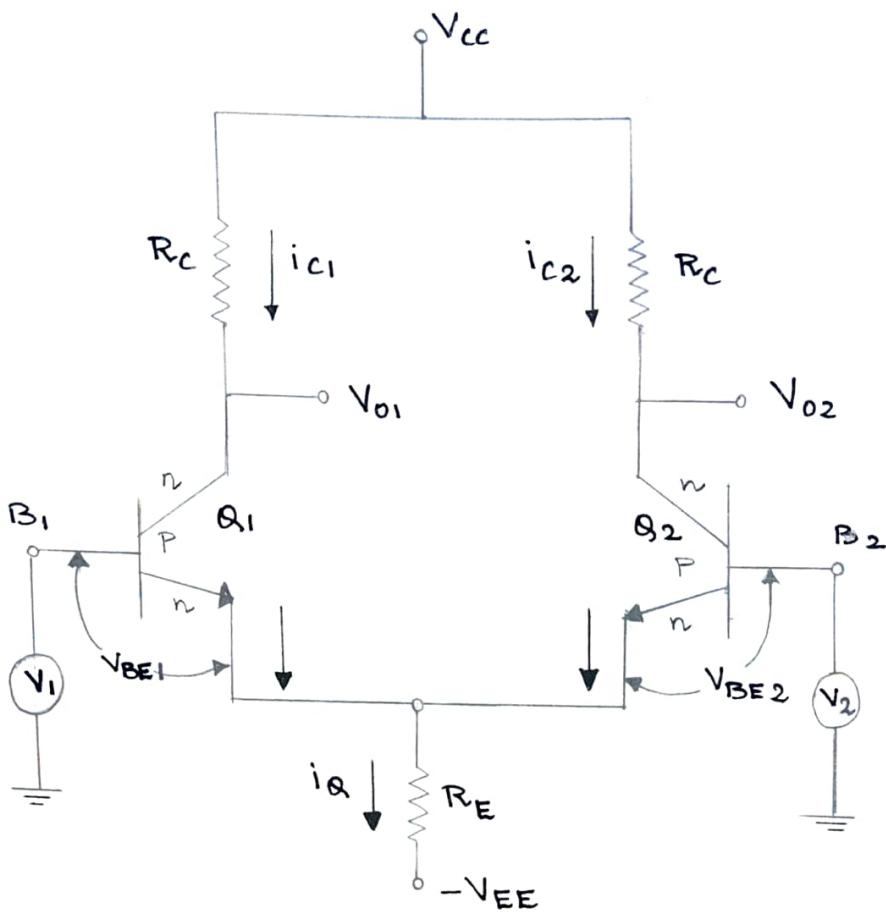


fig. The Basic differential amplifier

There are four different configurations depending upon the number of input signals used and the way output is taken. These four configurations are:

1. Dual-input balanced-output (or) Differential-input, differential-output.
2. Dual-input unbalanced-output (or) Differential-input, single ended-output
3. Single-input balanced-output (or) single ended-input, differential output.
4. Single-input unbalanced-output (or) single ended-input, single ended-output.

* Hint : in general balanced opamp refers that the OIP is taken from both the transistors Q1 & Q2

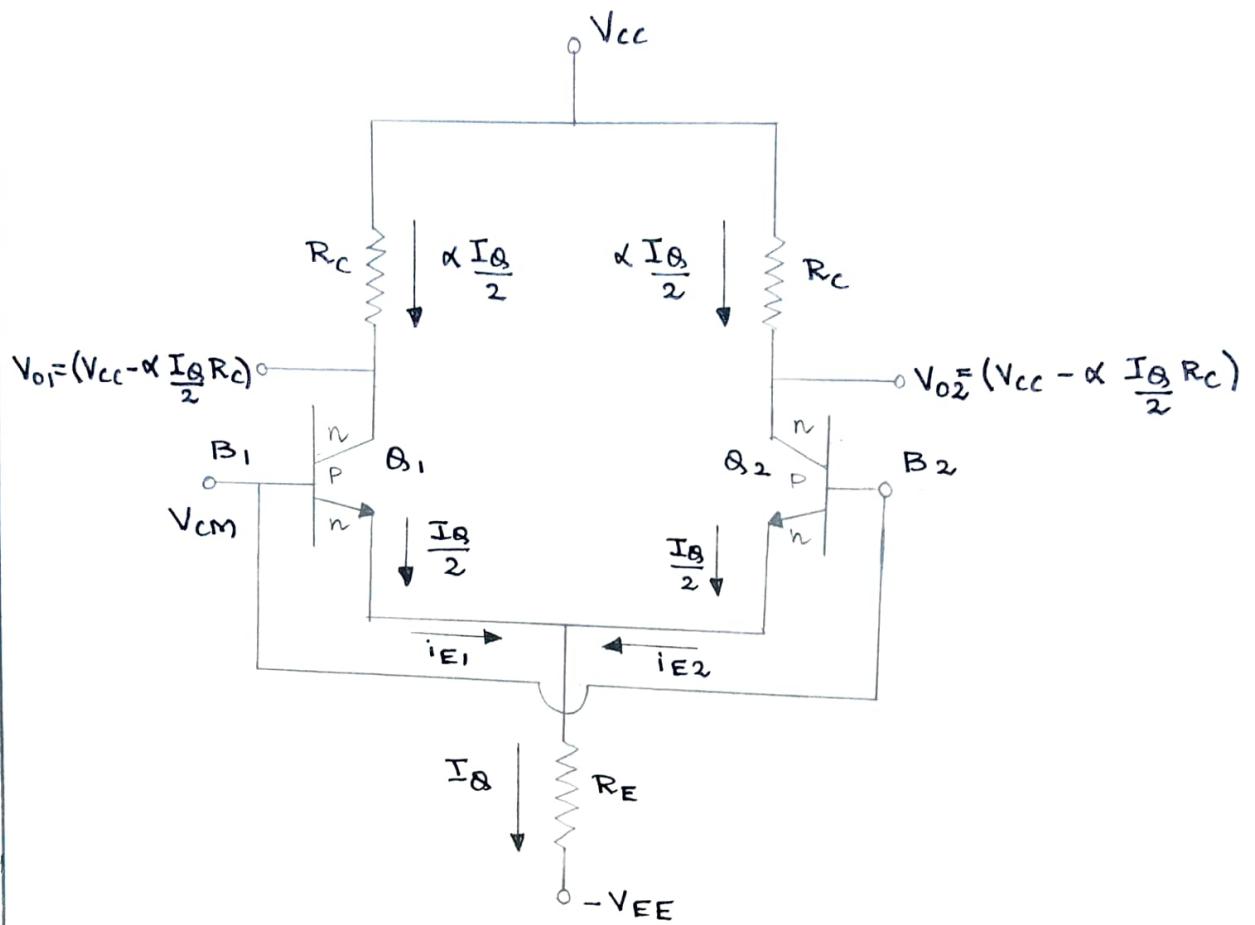


Fig. Shows the Differential pair with a common-mode input signal V_{CM}

Analysis:

$i_{E1} = i_{E2}$ { $\therefore Q_1$ and Q_2 are perfectly matched}

$$I_Q = i_{E1} + i_{E2}$$

$$i_{E1} = \frac{I_Q}{2} \quad \text{and} \quad i_{E2} = \frac{I_Q}{2}$$

$$i_{C1} = \alpha i_{E1} = \alpha \frac{I_Q}{2}$$

$$i_{C2} = \alpha i_{E2} = \alpha \frac{I_Q}{2}$$

$$\therefore V_{O1} = V_{CC} - i_{C1} R_C$$

$V_{O1} = V_{CC} - \alpha \frac{I_Q}{2} R_C$
--

$$\therefore V_{O2} = V_{CC} - i_{C2} R_C$$

$V_{O2} = V_{CC} - \alpha \frac{I_Q}{2} R_C$
--

$V_o = V_{o1} - V_{o2} = 0$ (Rejects the common-mode gain)
 ↳ Result

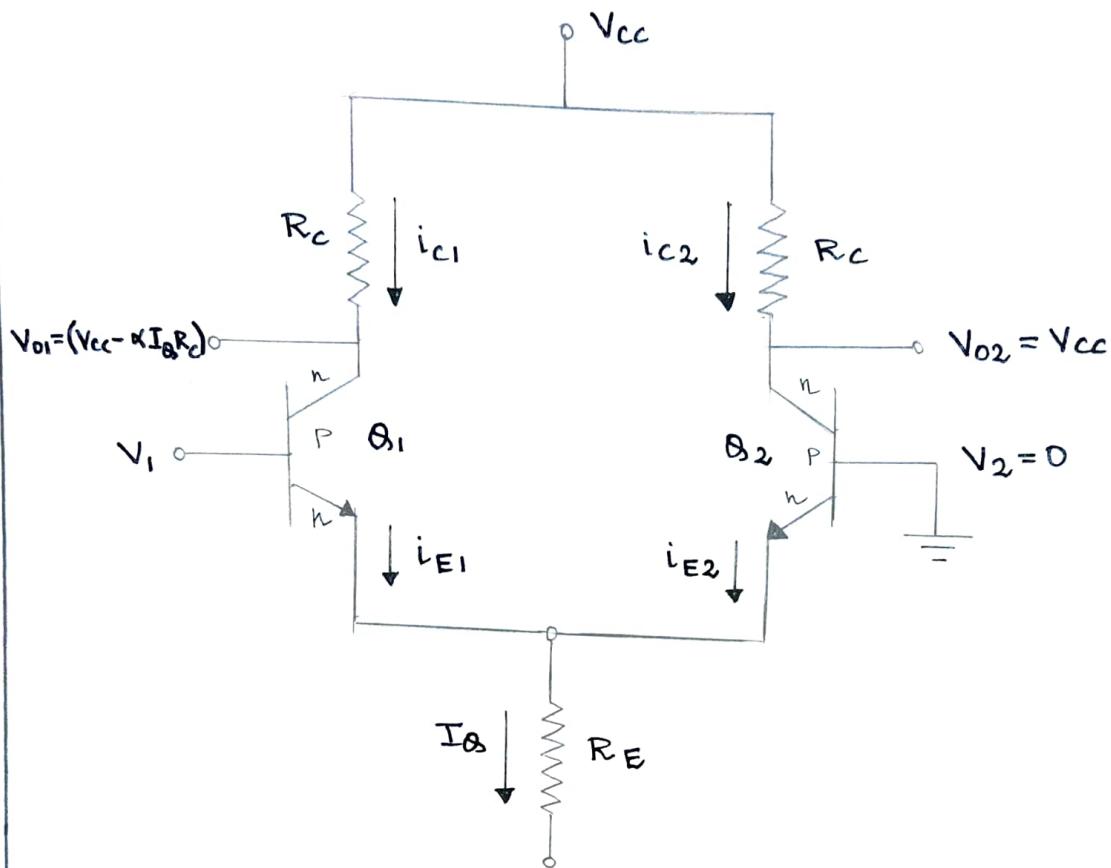


Fig. shows The differential pair with 'large' differential input signal.

Analysis:

$$I_Q = i_{E1} + i_{E2} \quad i_c = \alpha i_E$$

$$i_{E1} = I_Q \quad i_{c1} = \alpha i_{E1} = \alpha I_Q$$

Different inputs are given $\Rightarrow V_1 = 1V ; V_2 = 0V$

$$V_{o1} = V_{cc} - i_{c1} R_c$$

$$V_{o1} = V_{cc} - \alpha I_Q R_c$$

$$V_{o2} = V_{cc}$$

$$V_{o2} - V_{o1} = \alpha I_Q R_c$$

Thus, the differential pair responds only to the difference mode signals and rejects common-mode signals.

LEVEL TRANSLATOR

* There are two good reasons for using a level shifter in an IC op-amp. As we want an op-amp to operate down to dc, no coupling capacitor is used. Because of direct coupling, the dc level rises from stage to stage. The increase in dc level tends to shift the operating point (Q) of the next stage. This, in turn, limits the output voltage swing and may even distort the output signal. Therefore, it becomes essential that the quiescent voltage of one stage is shifted before it is applied to the next stage.

* Another requirement to be satisfied is that the output should have quiescent voltage level of $0V$ for zero input signal. Thus, zero offset condition.

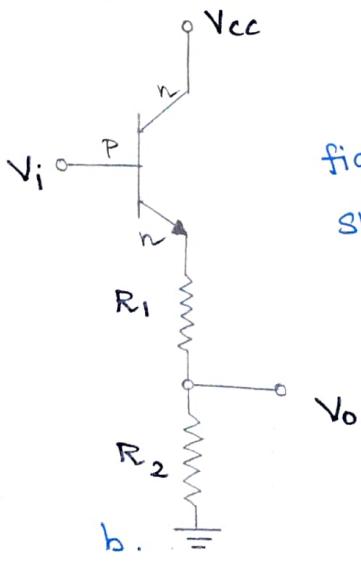
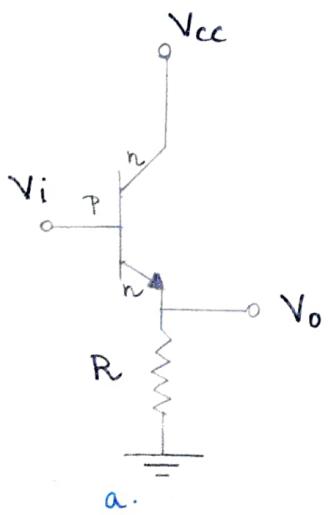


fig. a & fig. b
Shows level translator
using emitter
follower
buffer

* From the figure a & b we can infer that level translator is basically an emitter follower. Hence, the level shifter also acts as a buffer to isolate the high gain stages from the output stage.

OUTPUT STAGE

- * The function of the last stage, that is, the output stage in an op-amp is to supply the load current and provide a low impedance output.
- * A simple output stage consists of two complementary transistors Q_1 (n-p-n) and Q_2 (p-n-p) connected as emitter followers as shown in the figure given below.

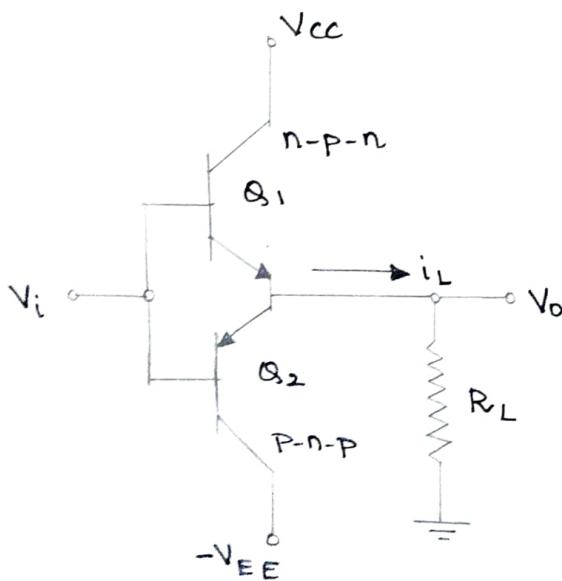


Fig. shows A complementary emitter follower output stage

- * It can be seen that for V_i positive, transistor Q_1 is ON and supplies current to load R_L . And, if V_i is negative, Q_1 is cut off and Q_2 acts as a sink to remove current from the load R_L .

AC CHARACTERISTICS

FREQUENCY RESPONSE

* Ideally, an op-amp should have an infinite bandwidth. This means that, if its open-loop gain is 90dB with dc signal its gain should remain the same 90dB through audio and on to high radio frequencies. The practical op-amp gain, however, decreases (rolls off) at higher frequencies.

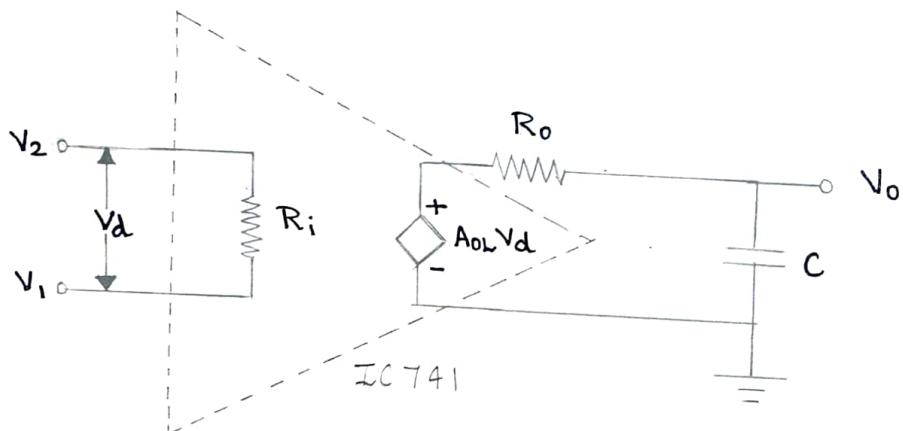


Fig. Shows High frequency model of an op-amp with single corner frequency.

* An op-amp with only one break (corner) frequency, all the capacitor effects can be represented by a single capacitor C. There is one pole due to $R_o C$ and obviously one -20 dB/decade roll-off comes into effect.

$$V_o = \frac{-jX_c}{R_o - jX_c} AOL V_d$$

$$A = \frac{V_o}{V_d} = \frac{AOL}{1 + j2\pi f R_o C}$$

$$A = \frac{A_{OL}}{1 + j(f/f_i)}$$

where, $f_i = \frac{1}{2\pi R_o C}$

f_i is the corner frequency or the upper 3-dB frequency of the op-amp.

The magnitude and the phase angle of the open loop voltage gain are function of frequency and can be written as

$$|A| = \frac{A_{OL}}{\sqrt{1 + (f/f_i)^2}}$$

$$\phi = -\tan^{-1}(f/f_i)$$

* -ve sign indicates the phase shift

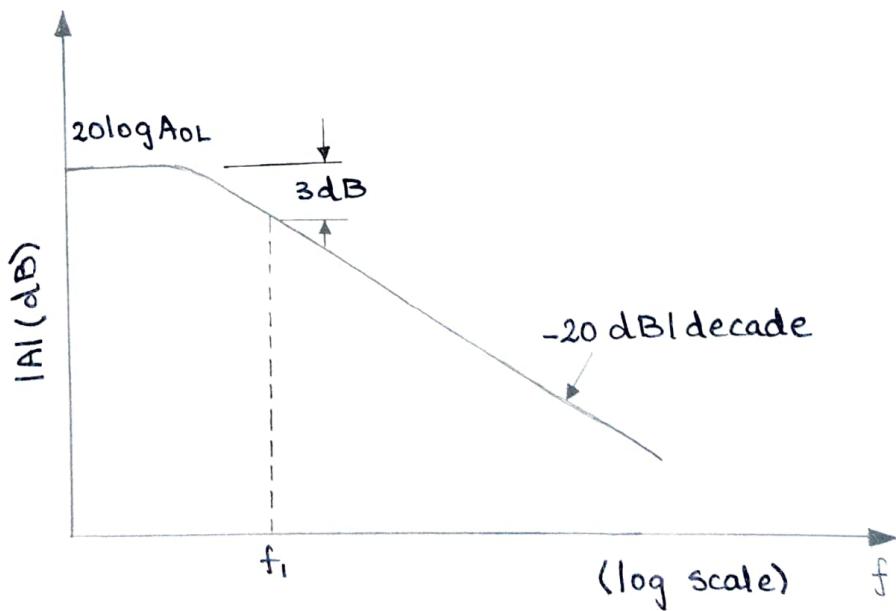


Fig. Open loop magnitude characteristics

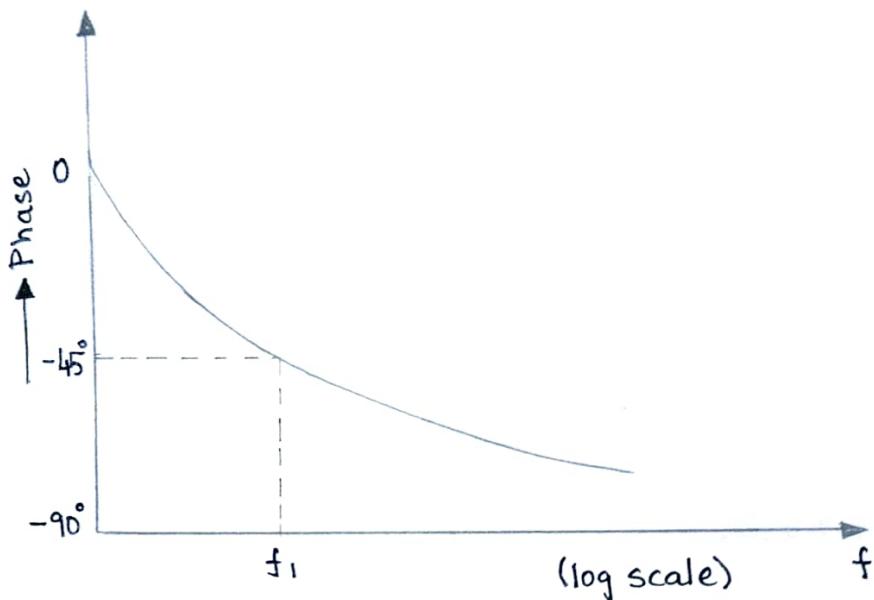


Fig. shows Phase Characteristics for an op-amp with single break frequency.

Single Pole System

ϕ at $f_1 = -45^\circ$; maximum phase change $= 90^\circ$

Two Pole System

ϕ at $f = f_2 = -90^\circ$; maximum phase change $= 135^\circ$

Three Pole System

ϕ at $f = f_3 = -135^\circ$; maximum phase change $= 180^\circ$

Gain equation for single pole system

$$A = \frac{A_{OL}}{1 + j(f/f_1)}$$

Gain equation for Two pole system

$$A = \frac{A_{OL}}{(1 + jf/f_1)(1 + jf/f_2)}$$

$f_1 < f_2$
↳ condition

Gain equation for Three pole system

$$A = \frac{A_{OL}}{(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)}$$

$f_1 < f_2 < f_3$
↳ condition

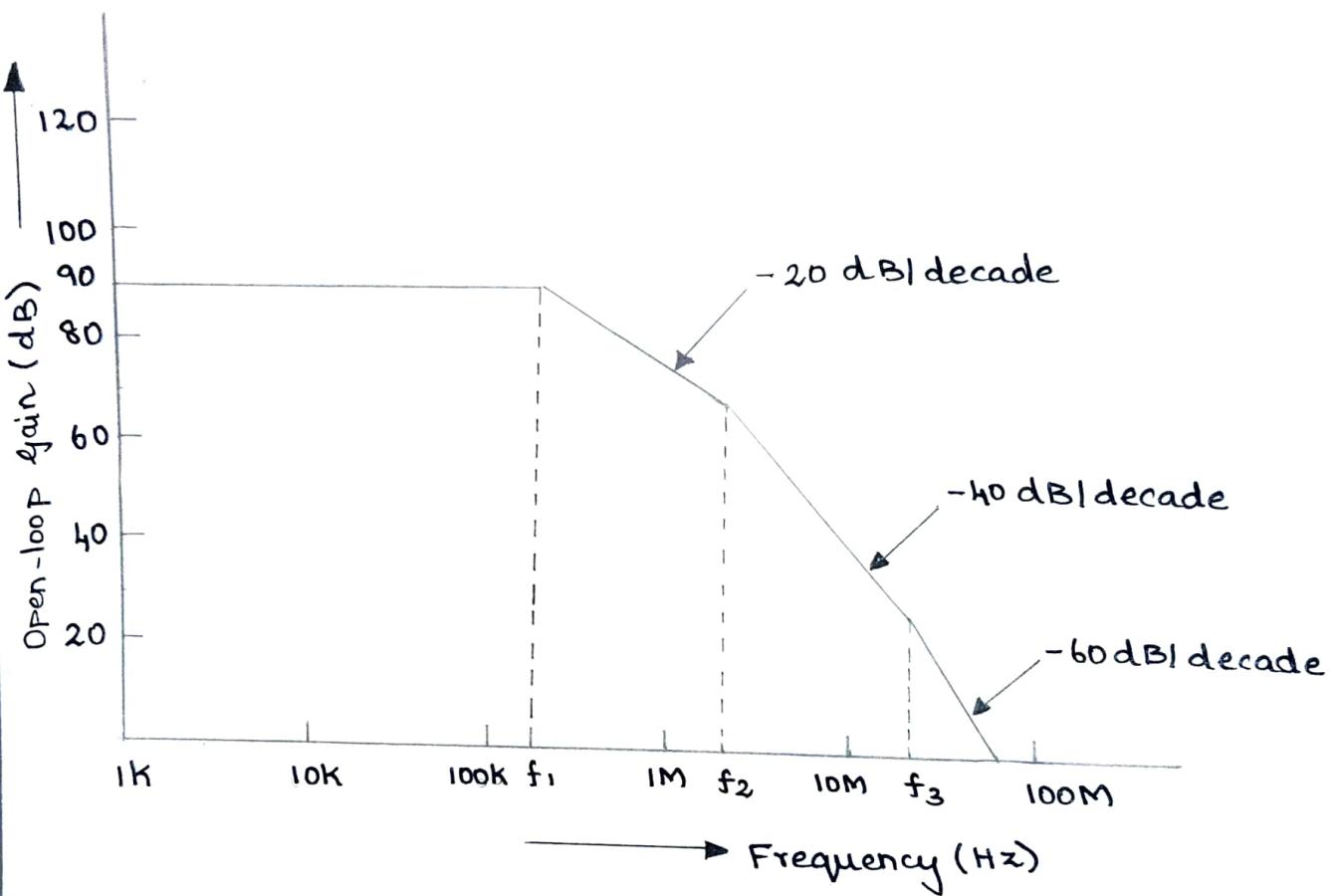


Fig. shows Approximation of open loop gain Vs frequency curve

From the graph, the open loop frequency response is flat (90dB) from low frequencies (including dc) to 200kHz, the first break frequency. From 200kHz to 2MHz the gain drops from 90 dB to 70 dB which is at a -20 dB/decade or -6 dB/octave rate. At frequencies from 2MHz to 20MHz, the roll-off rate is -40 dB/decade or -12 dB/octave.

Accordingly, as frequency is increasing, cascading effect of RC pairs (poles) come into effect and roll-off rate increases successively by -20 dB/decade at each corner frequency.

STABILITY OF AN OP-AMP

- * From the negative feedback concept,

$$A_{CL} = \frac{A}{1 + AB}$$

where AB is the loop gain

$1 + AB = 0$ is the characteristic equation

Op-Amp is said to be stable if it satisfies the condition :

(*) * $|AB| < 1$ where $|AB| \Rightarrow$ magnitude of loop gain

* $\phi = 180^\circ$ $\phi \Rightarrow$ phase shift

* if any of the condition is not satisfied, then it behaves like a oscillator thus the starting point of instability.

FREQUENCY COMPENSATION

* In systems containing more than three poles the phase shift is more than 180° thus $\phi > 180^\circ$, disatisfies the condition for stability. Therefore, the op-amp becomes unstable. Thus, we are going for frequency compensation technique. eg:-

1 pole system \Rightarrow phase shift $\phi = 90^\circ$ 3 pole system $= \phi = 180^\circ$

2 pole system $= \phi = 135^\circ$ 4 pole system $= \phi = \frac{225^\circ}{\hookrightarrow \phi > 180^\circ}$

FREQUENCY COMPENSATION TECHNIQUE:

* The method of modifying loop gain frequency response of an Op-Amp so that it behaves like single break frequency response that provides sufficient positive phase margin that is called frequency compensation.

TYPES OF COMPENSATION TECHNIQUES:

1. External Frequency Compensation
2. Internal Frequency Compensation

EXTERNAL FREQUENCY COMPENSATION:

* Op-Amps are made to be used with externally connected compensating components to compensate the phase shift.

TWO METHODS:

1. Dominant-pole compensation
2. Pole-zero (lag) compensation

Dominant Pole Compensation

* Introduce a dominant pole by adding RC-network in series with op-amp as shown in the figure given below:

(2)

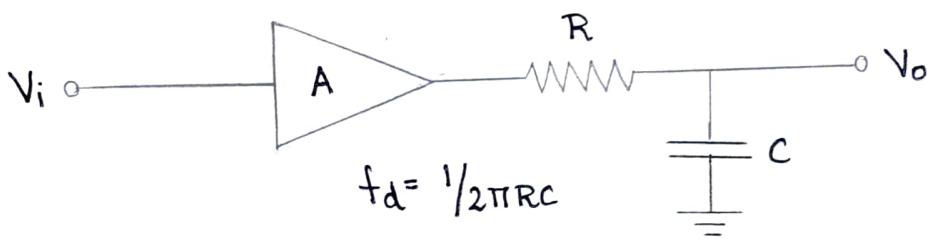


Fig. shows Dominant Pole compensation

$$A' = \frac{V_o}{V_i}$$

$$= A \cdot \frac{-j/\omega_c}{R - j/\omega_c} = \frac{A}{1 + j \frac{f}{f_d}}$$

where, $f_d = \frac{1}{2\pi RC}$ f_d : dominant frequency

3 pole system gain equation (in general)

$$A = \frac{A_{OL}}{(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)} \quad f_1 < f_2 < f_3$$

\Leftrightarrow condition

Then,

$$A' = \frac{A_{OL}}{(1+jf/f_d)(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)}$$

$f_d < f_1 < f_2 < f_3$
 \Leftrightarrow condition

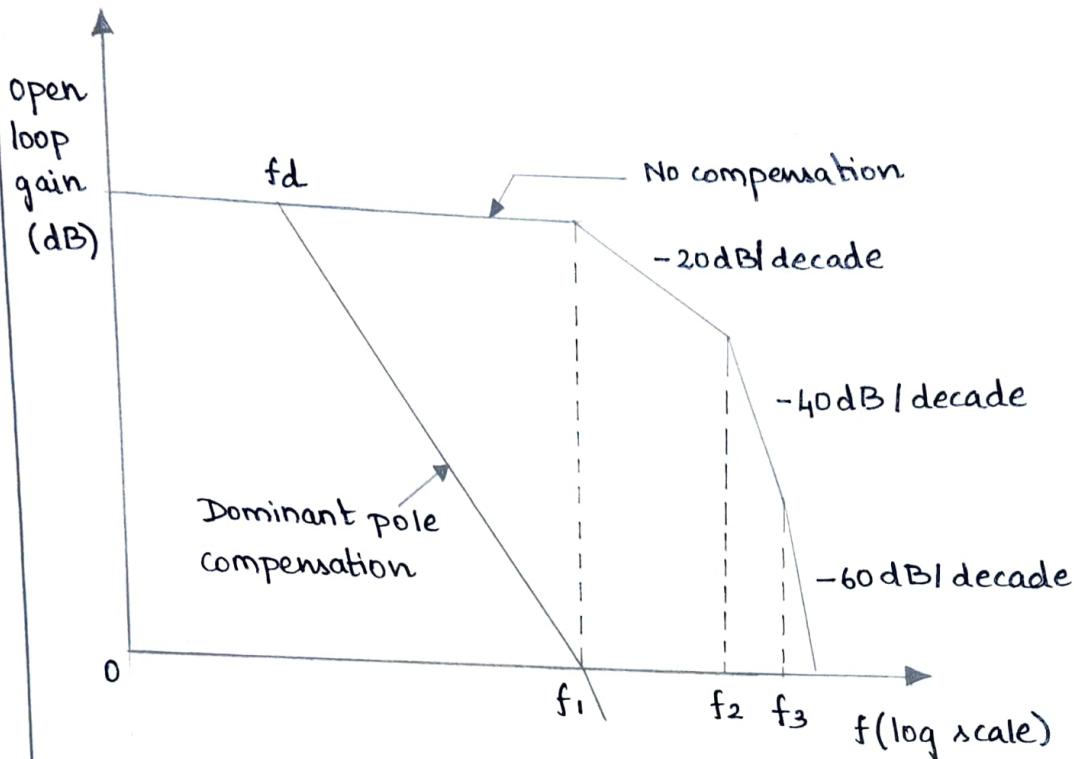


Fig. shows Gain Vs frequency curve for dominant pole compensation

MERITS

- * Maintaining the gain thus gain is high at low frequency
- * Excellent noise immunity
- * By adjusting f_d adequate phase margin and stability is assured.

DEMERITS

- * The bandwidth is reduced for a compensated system.

POLE-ZERO COMPENSATION

- * Here the uncompensated transfer function A is altered by adding both pole and a zero as shown in the figure given below. The zero should be at higher frequency than pole.

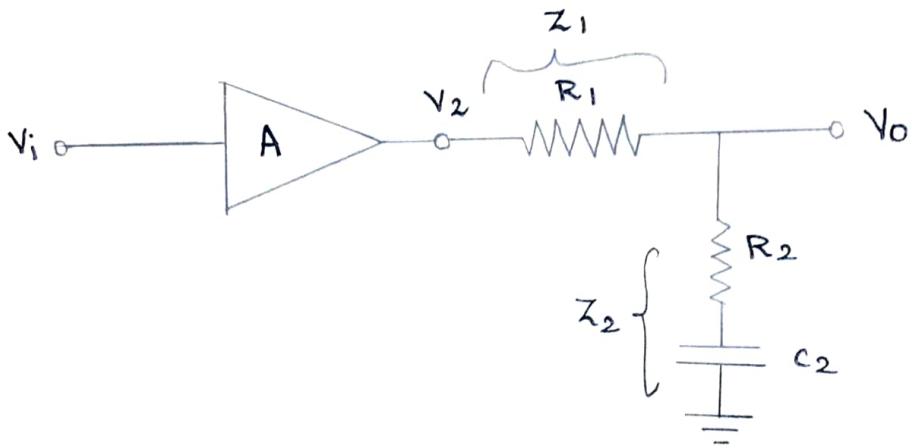


Fig. shows Pole-Zero compensation

$$Z_1 = R_1 ; \quad Z_2 = R_2 - jX_{C2}$$

$$A = \frac{Z_2}{Z_1 + Z_2}$$

$$A_1 = \frac{R_2 - jX_{C2}}{R_1 + R_2 - jX_{C2}}$$

$$A_1 = \frac{1 + j2\pi f R_2 C_2}{1 + j2\pi f (R_1 + R_2) C_2}$$

where,

$$A_1 = \frac{1 + j(f/f_1)}{1 + j(f/f_0)}$$

$$f_1 = \frac{1}{2\pi R_2 C_2} \quad f_0 = \frac{1}{2\pi (R_1 + R_2) C_2}$$

$$A = \frac{A_{OL} (1 + jf/f_1)}{(1 + jf/f_0)(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)}$$

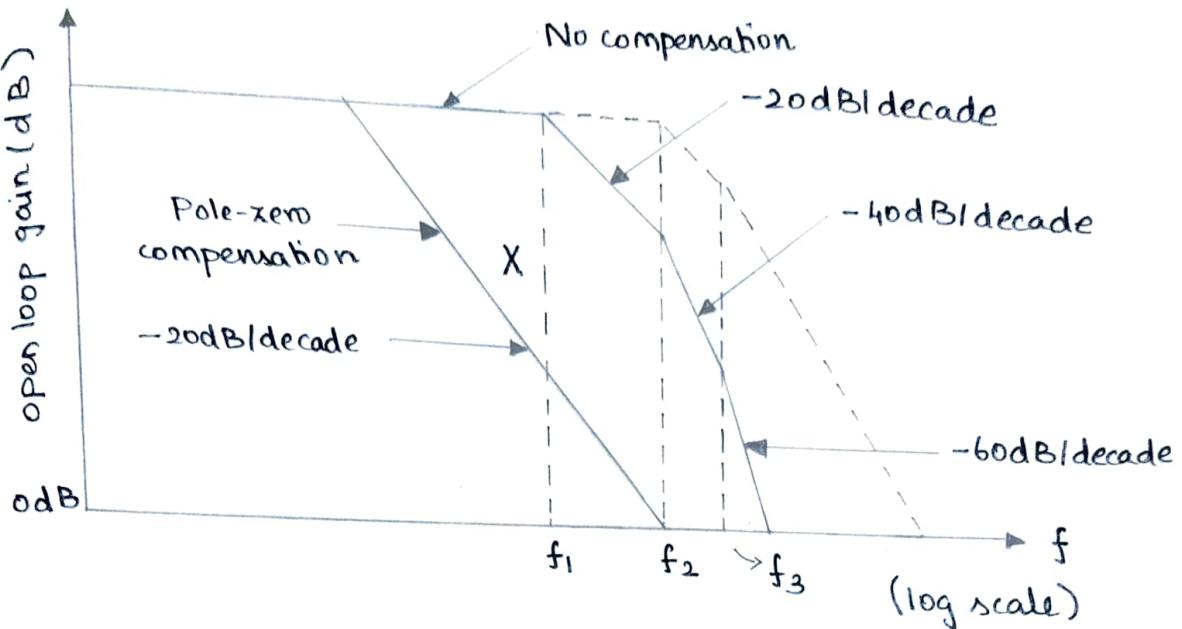
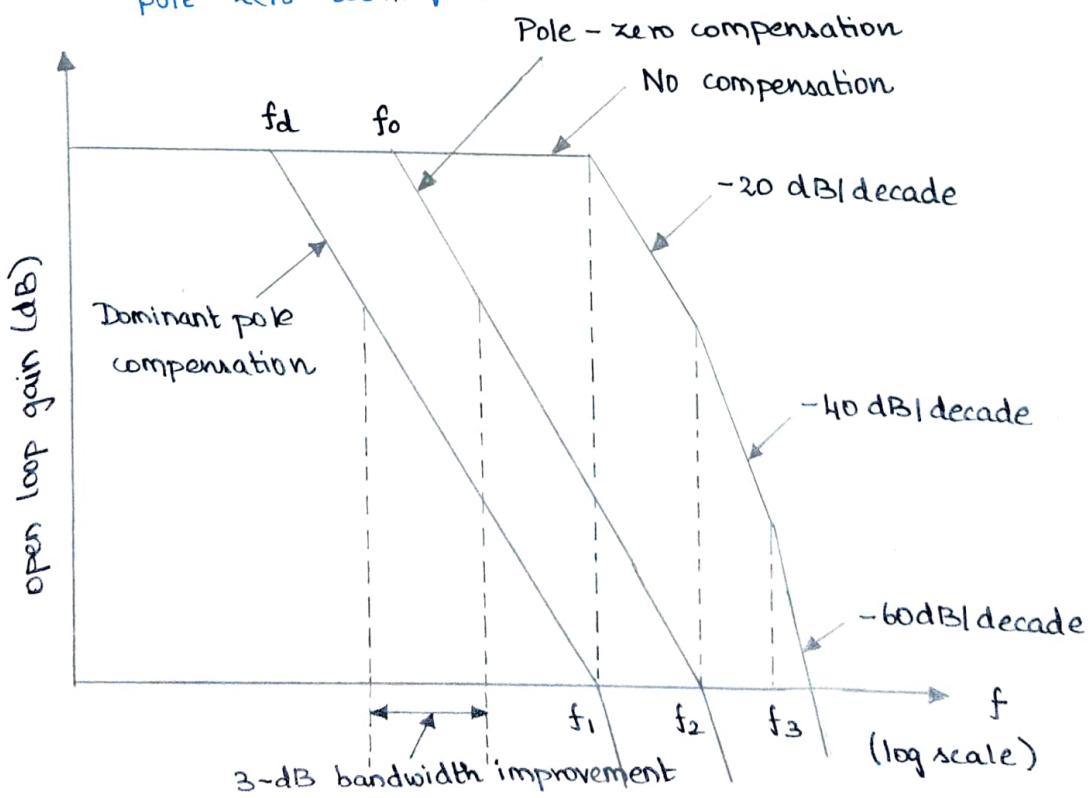


Fig. shows Open loop gain Vs frequency for pole-zero compensation.

MERITS:

- * Bandwidth is more compared to Dominant Pole compensation. Fig. shows comparison of dominant pole and pole-zero techniques



INTERNAL COMPENSATION TECHNIQUE

(12)

* In recently developed op-Amps like IC741 the compensation is built internally. A capacitor ranging from 10-30PF is fabricated between input and output stage to achieve the required compensation. So, this type of compensation is called Miller effect compensation.

e.g.: LM107, LM741, LM112 and MC1558

SLEW RATE

* The rise time of an amplifier is defined as the time the output takes to change from 10 to 90 per cent of the final value for a step input and is given as $0.35/BW$, where BW is the bandwidth of the amplifier.

* Rise time is usually specified for small signals usually when the peak output voltage is less than one volt (1V).

* For large signal output (i.e., $V_m > 1$ volt), the op-amp's speed is limited by slew rate.

DEFINITION:

* The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in $V/\mu s$.

What causes slew rate?

* There is usually a capacitor within or outside an op-amp to prevent oscillation. It is this capacitor which prevents the output voltage from responding immediately to a fast changing input.

$$I = \frac{C dV_C}{dt}$$

$$\text{Slew rate SR} = \left. \frac{dV_C}{dt} \right|_{\max} = \frac{I_{\max}}{C}$$

DC CHARACTERISTICS

* An ideal op-amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. These non-ideal dc characteristics that add error components to the dc output voltage are:

1. Input bias current
2. Input offset current
3. Input offset Voltage
4. Thermal drift

1. INPUT BIAS CURRENT

* In an ideal op-amp, we assumed that no current is drawn from the input terminals. However, practically, input terminals do conduct a small value of dc current to bias the input transistors.

* Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalances between the two inputs.

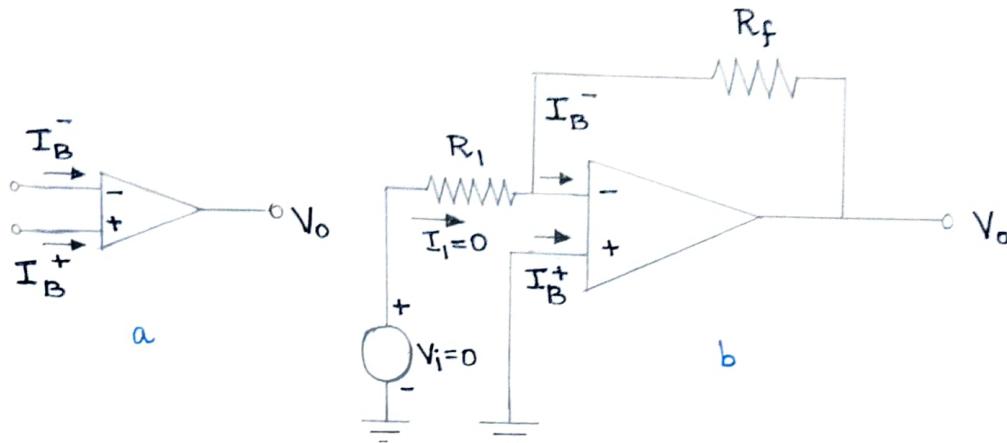


Fig. shows (a) Input bias currents (b) Inverting amplifier with bias currents

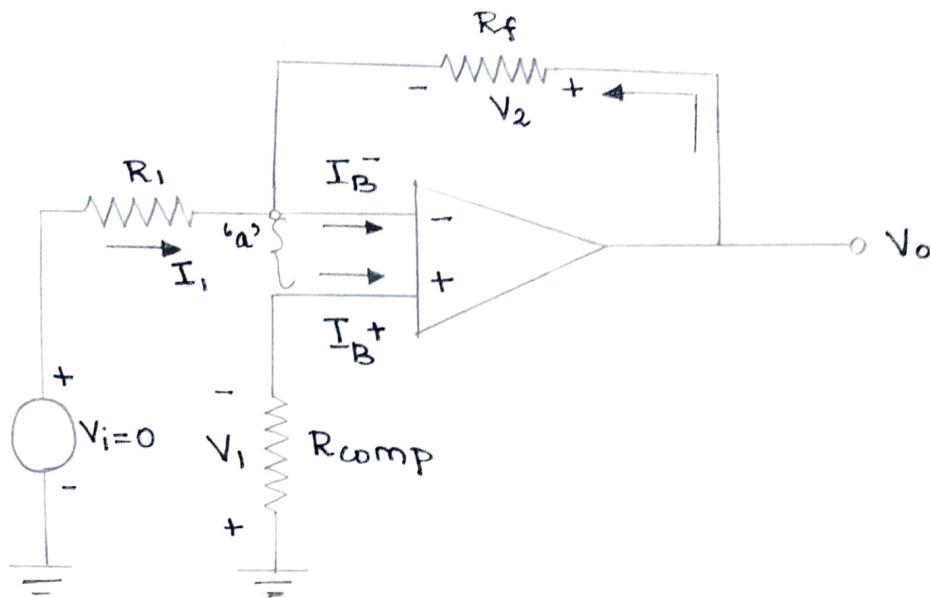
$$\text{Practically, } I_B = \frac{I_B^+ + I_B^-}{2}$$

For IC141, the input bias current is 500nA or less.

* If input voltage V_i is set to zero volt, the output voltage V_o should also be zero volt. Instead, we find that the output voltage is offset by,

$$\begin{aligned} V_o &= (I_B^-) R_f \quad R_f = 1M\Omega \\ &= (500nA) 10^6 \\ &= 500 \times 10^{-9} \times 10^6 = 500 \text{ mV} \end{aligned}$$

* The output is driven to 500mV with zero input because of the bias currents. In order to compensate this output a resistor is included in the non-inverting terminal.



Derivation:

$$I_B^+ = \frac{V_1}{R_{\text{comp}}} \rightarrow ①$$

$$\begin{aligned} I_B^- &= I_1 + I_2 \\ &= \frac{V_1}{R_1} + \frac{V_2}{R_f} \quad \text{consider } V_1 = V_2 \end{aligned}$$

then,

$$I_B^- = \frac{V_1}{R_1} + \frac{V_1}{R_f}$$

$$I_B^- = V_1 \left(\frac{R_1 + R_f}{R_1 R_f} \right)$$

compare I_B^+ and I_B^-

$$\frac{V_1}{R_{\text{comp}}} = V_1 \left(\frac{R_1 + R_f}{R_1 R_f} \right)$$

$$\therefore R_{\text{comp}} = \frac{R_1 R_f}{R_1 + R_f}$$

$$\therefore R_{\text{comp}} = R_1 \parallel R_f$$

2. INPUT OFFSET CURRENT

(12)

* Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. Since the input transistors cannot be made identical, there will always be some small difference between I_B^+ and I_B^- . This difference is called the offset current I_{OS} and can be written as

$$|I_{OS}| = I_B^+ - I_B^-$$

* For IC741, the offset current I_{OS} for an op-Amp is $200nA$.

$$V_1 = I_B^+ R_{comp} \rightarrow ①$$

$$I_1 = \frac{V_1}{R_1}$$

$$I_2 = (I_B^- - I_1) = I_B^- - \left(\frac{I_B^+ \cdot R_{comp}}{R_1} \right) \rightarrow ②$$

$$V_o = I_2 R_f - V_1 = I_2 R_f - I_B^+ R_{comp} \rightarrow ③$$

substitute I_2 in eqn. ③

$$V_o = \left[I_B^- - \left(\frac{I_B^+ \cdot R_{comp}}{R_1} \right) R_f \right] - I_B^+ R_{comp}$$

substitute $R_{comp} = R_1 \parallel R_f$ then

$$V_o = R_f [I_B^- - I_B^+] = R_f I_{OS}$$

$$\therefore V_o = R_f I_{OS}$$

If $I_{OS} = 200nA$; $R_f = 1M\Omega$

$$V_o = (200nA) 10^6$$

$$\underline{\underline{V_o = 200mV}}$$

* To compensate this output voltage we use
T-feedback Network

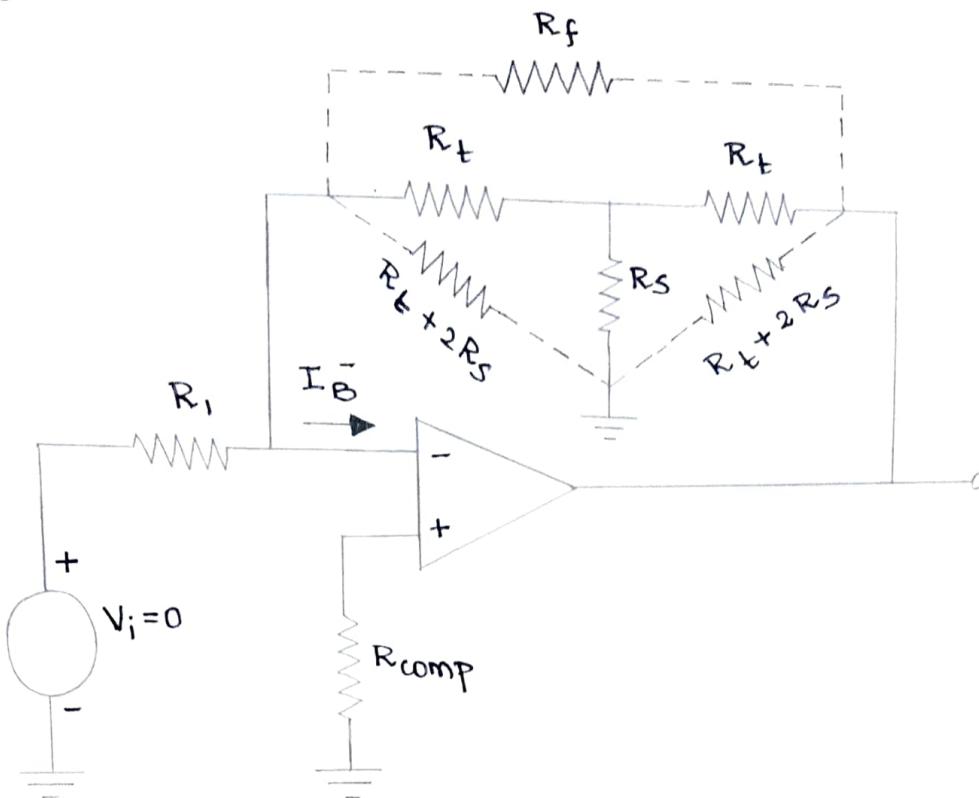


Fig. shows Inverting amplifier with T-feedback network

To design a T-network, first pick

$$R_t \ll \frac{R_f}{2}$$

Then calculate

$$R_s = \frac{R_t^2}{R_f - 2R_t}$$

3. INPUT OFFSET VOLTAGE

- * Inspite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminals to make output voltage zero. This voltage is called

input offset voltage V_{ios} .

(12)

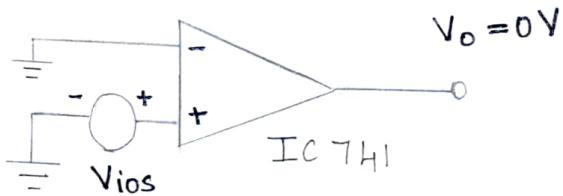


Fig. shows Op-amp input offset voltage

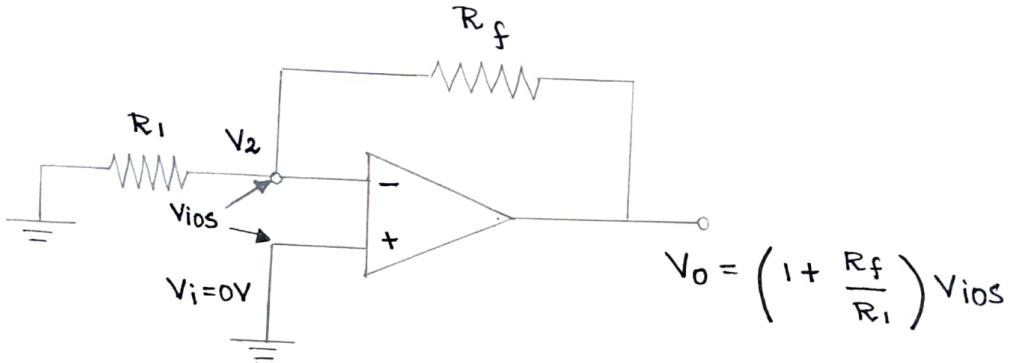


Fig. shows Equivalent circuit for $V_i=0$

$$V_o = \left(1 + \frac{R_f}{R_1} \right) V_{ios}$$

Total Output Offset Voltage

* The total output offset voltage V_{OT} could be either more or less than the offset voltage produced at the output due to input bias current or input offset voltage alone. This is because input offset voltage V_{ios} and input bias current I_B could be either positive or negative with respect to ground.

$$V_{OT} = \left(1 + \frac{R_f}{R_1} \right) V_{ios} + R_f I_{os}$$

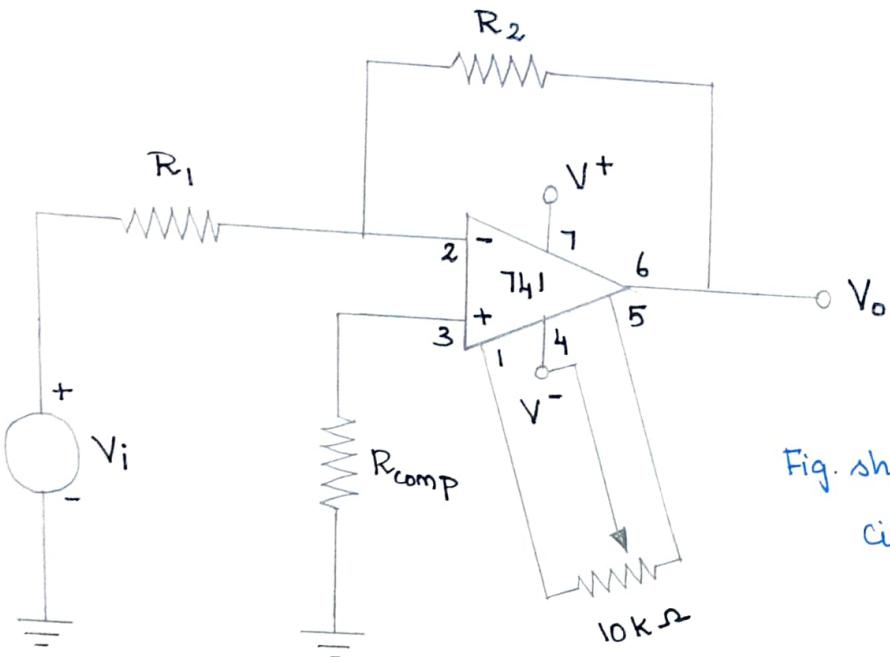


Fig. shows Equivalent circuit for $V_i=0$

* Many op-amps provide offset compensation pins to nullify the offset voltage. The position of the wiper which is connected to the negative supply pin 4 is adjusted to nullify the output offset voltage.

4. THERMAL DRIFT

* Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°C may not remain so when the temperature rises to 35°C. This is called drift. These indicate the change in offset for each degree celsius change in temperature.

Methods to minimize the thermal drift

- * Careful printed circuit board layout must be used to keep op-amps away from source of heat.
- * Forced air cooling may be used to stabilize the ambient temperature.