

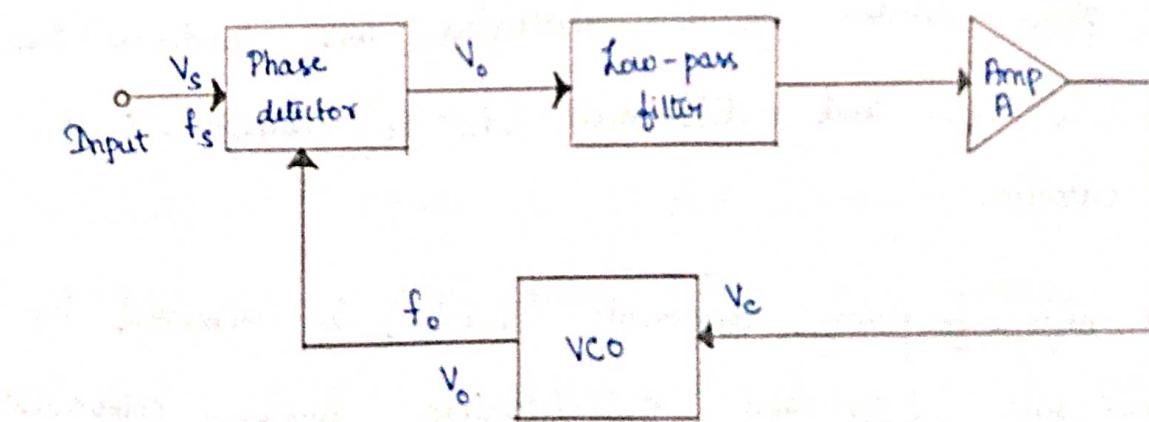
Phase - locked loops (PLL)

The phase-locked loop (PLL) is an important building block of linear systems. This technique for electronic frequency control is used today in satellite communication system, air borne navigational system, FM communication system, computers etc.

Basic Principles:

This feedback system consists of :

1. Phase detector / Comparator.
2. A low pass filter.
3. An error amplifier.
4. A Voltage Controlled Oscillator (vco).



- * The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency.
- * The frequency can also be shifted to either side by applying a dc control voltage V_c to an appropriate terminal of the IC.
- * The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator".
- * If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output V_o of the VCO.
- * If two signals differ in frequency / phase, an error voltage V_e is generated.
- * The phase detector is a multiplier and produces the sum ($f_s + f_o$) and difference ($f_s - f_o$) components at its output.
- * The high frequency component ($f_s + f_o$) is removed by the low pass filter and the difference frequency component is amplified and then ~~suppl~~ applied as control voltage V_c to VCO.

* The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference between f_c and f_o . Once this action starts, we say that the signal is in the capture range.

* The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. This circuit is then said to be locked.

* Once locked, PLL tracks the frequency changes of the input signal. Thus a PLL through three stages:
i) free running ii) Capture iii) Locked or tracking.

Lock-in Range:

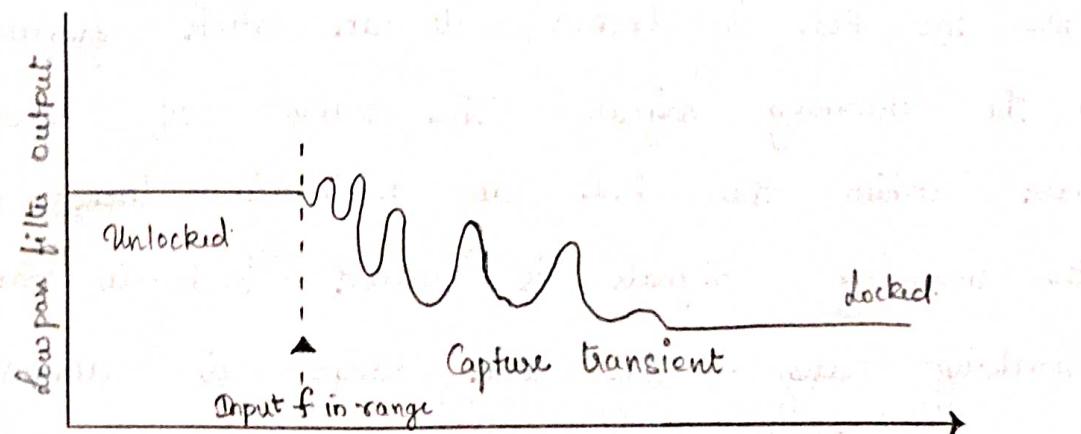
Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signals is called lock-in range or tracking range. The lock range is usually expressed as a percentage of f_o , the VCO frequency.

Capture Range:

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_0 .

Pull-in time:

The total time taken by PLL to establish lock is called pull-in time. This depends on the initial phase and phase difference between the two signals as well as on the overall loop gain and loop filter characteristics.



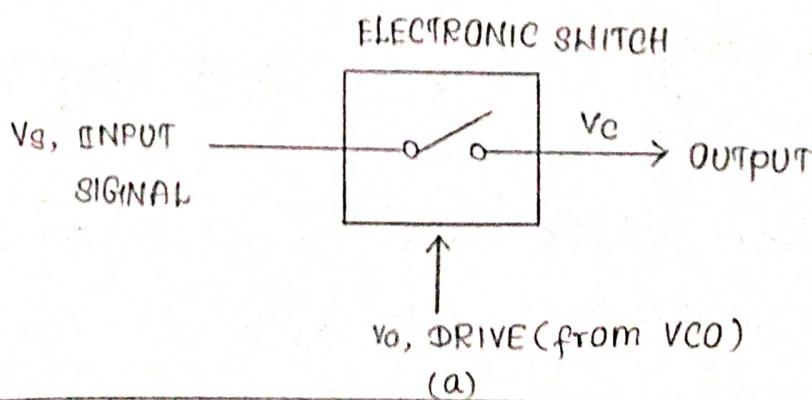
The Capture transient.

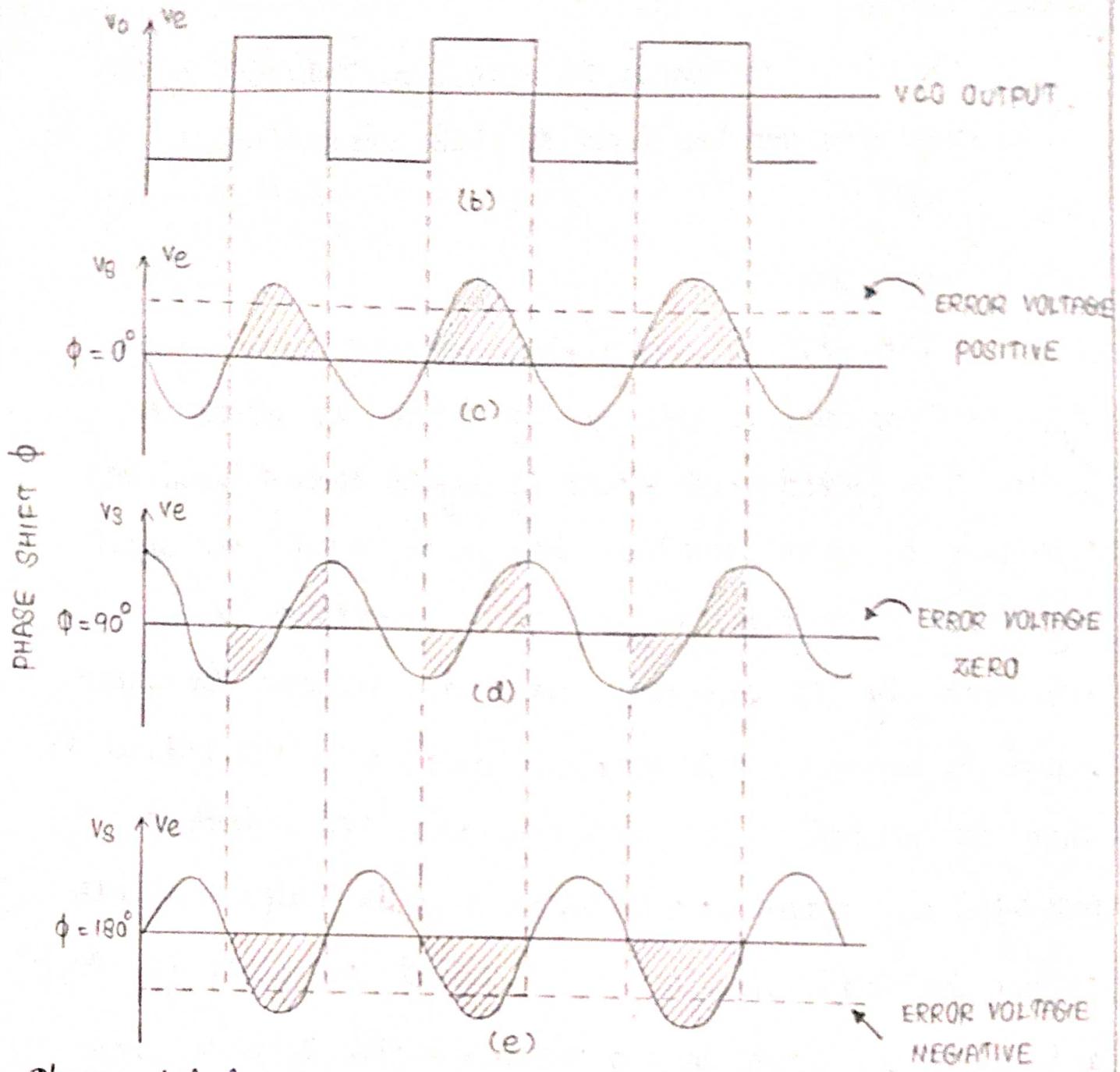
PHASE DETECTOR :-

The phase detection is the most important part of the PLL system. There are two types of phase detectors used, analog and digital.

ANALOG PHASE DETECTOR :-

The principle of analog phase detection using switch type phase detector is shown in Fig. 9.3(a). An electronic switch S is opened and closed by signal coming from VCO (normally a square wave) as shown in Fig. 9.3(b). The input signal is, therefore, chopped at a repetition rate determined by VCO frequency. Figure 9.3(c) shows the input signal v_s assumed to be in phase ($\phi = 0^\circ$) with VCO output v_o since the switch S is closed only when VCO output is positive, the output waveform v_e will be half sinusoids (shown hatched). Similarly, the output waveform for $\phi = 90^\circ$ and $\phi = 180^\circ$ is shown in Fig. 9.3(d, e). This type of phase detector is called a half wave detector, since the phase information for only one-half of the input waveform is detected and averaged. The output of the phase comparator





Phase detector for PLL (a) Basic schema b) vco output Waveform · Input and output waveform (hatched) of phase detector for (c) $\phi = 0^\circ$ (d) $\phi = 90^\circ$ (e) $\phi = 180^\circ$

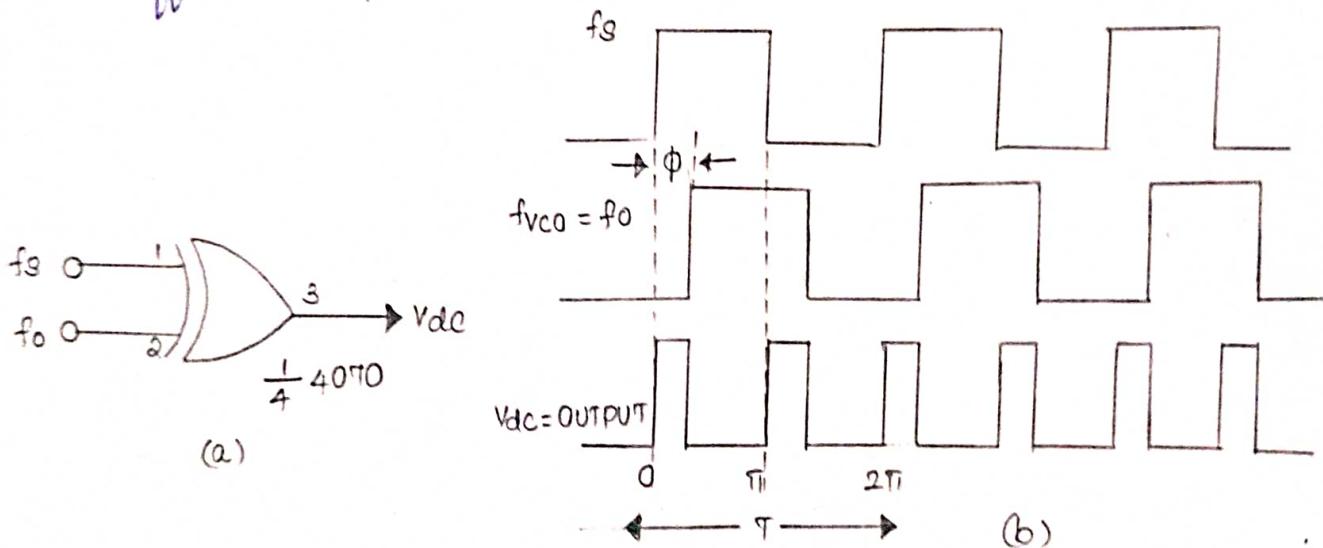
when filtered through a low pass filter gives an error signal which is the average value of the output waveform shown by dotted line in Fig. 9.3 (c,d,e)

It may be seen that the error voltage is zero when the phase shift between the two inputs is 90° . so, for

perfect lock, the vco output should be 90° out of phase with respect to the input signal.

DIGITAL PHASE DETECTOR:

Figure 9.5(a) shows the digital type XOR (exclusive OR) phase detector. It uses CMOS type 4010 quad 2-input XOR gate. The output of the XOR gate is high when only one of the input signals f_s or f_0 is high. This type of detector is used when both the input signals are square waves. The input and output waveforms for $f_s = f_0$ are shown in Fig 9.5(b). In this figure, f_s is leading f_0 by ϕ degrees. The variation of dc output voltage with phase difference ϕ



(a) Exclusive-OR phase detector b) Input and output waveform .

is shown in Fig 9.5(c). It can be seen that the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains

high throughout. The slope of the curve gives the conversion ratio k_ϕ of the phase detector. so, the conversion ratio k_ϕ for a supply voltage $V_{CC} = 5V$ is

$$k_\phi = \frac{5}{\pi} = 1.59 \text{ V/}^{\circ}\text{rad}$$

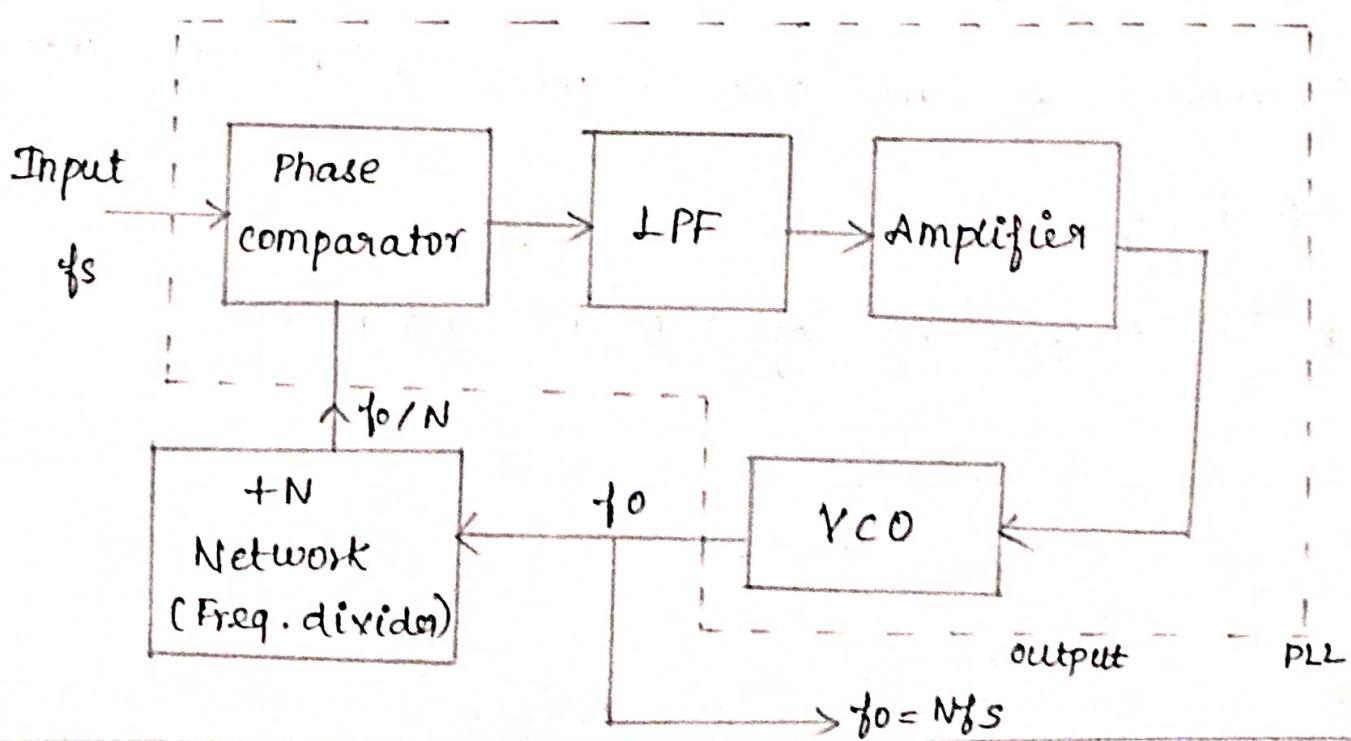
PLL APPLICATIONS.

The output from a PLL system can be obtained either as the voltage signal $V_C(t)$ corresponding to the error voltage in the feedback loop, or as frequency signal at V_{CO} output terminal.

The voltage output is used in frequency discriminator application whereas the frequency output is used in signal conditioning or clock recovery applications.

Some of the typical applications of PLL are:

1. FREQUENCY MULTIPLICATION / DIVISION:



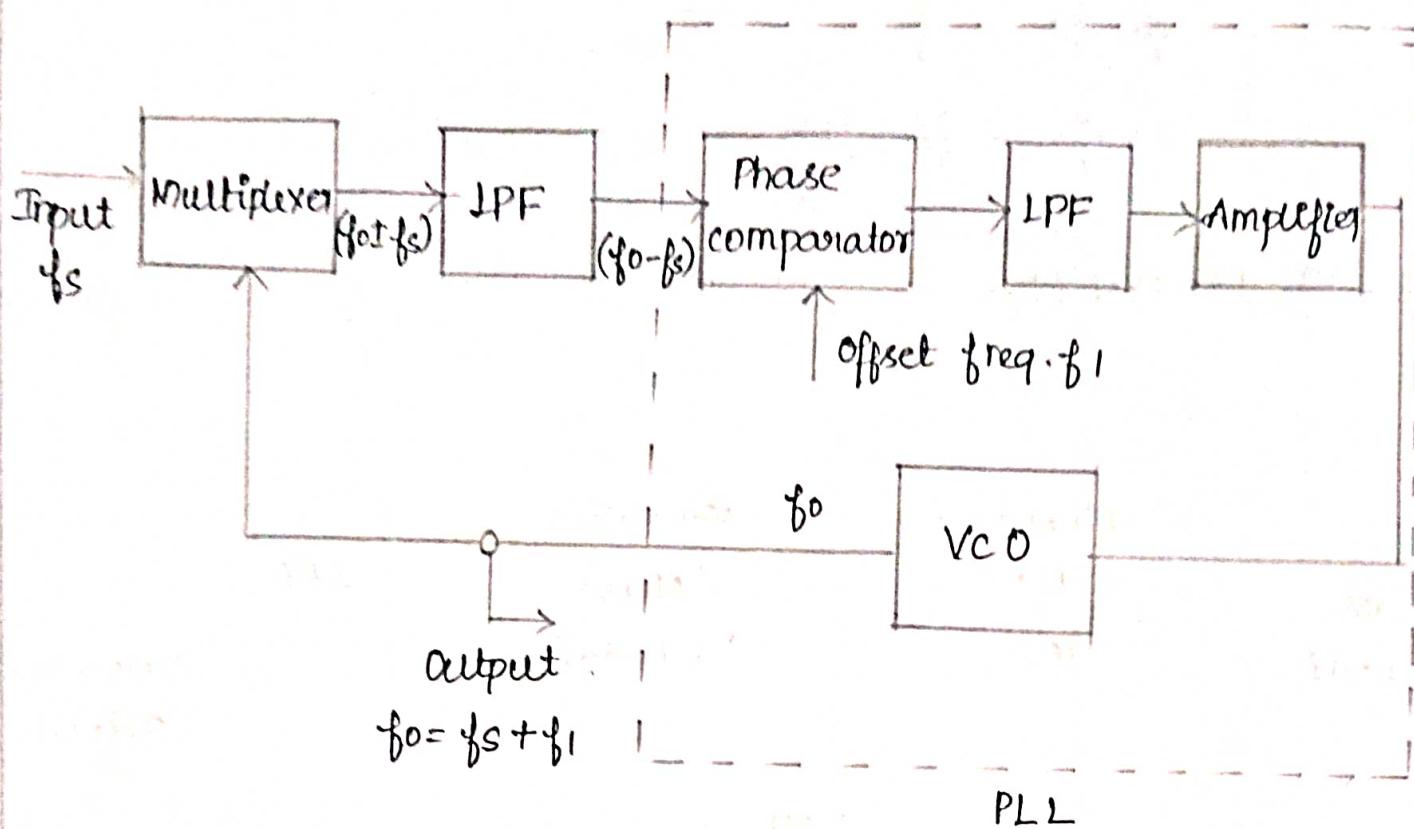
- * A divide by N network is inserted between the VCO output and the phase comparator input.
- * In the locked state, the VCO output frequency f_0 is given by

$$f_0 = N f_s$$

- * The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.
- * Frequency multiplication can also be obtained by using PLL in its harmonic locking mode.
- * This circuit can also be used for frequency division. Since the VCO output is rich in harmonics, it is possible to lock the mth harmonic of the VCO output with the input signal f_s .
- * The output f_0 of VCO is given by

$$f_0 = \frac{f_s}{m}$$

2. FREQUENCY TRANSLATION:



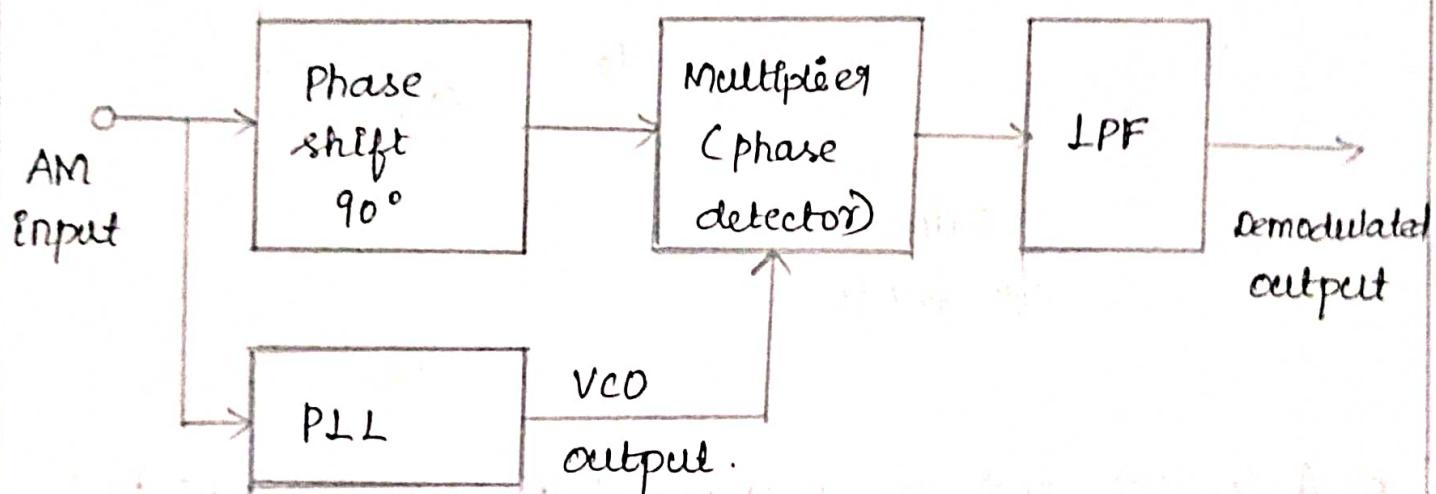
- * A mixer and a lowpass filter are connected externally to the PLL.
- * The signal f_s which has to be shifted and output frequency f_o of VCO are applied as inputs to the mixer.
- * The output of the mixer contains sum and difference of f_s and f_o . The output of LPF contains only the difference signal ($f_o - f_s$).
- * The translator or offset frequency is applied to the phase comparator.

when PLL is in locked state,

$$f_0 - f_s = f_l$$

$$f_0 = f_s + f_l$$

3. AM DETECTION:



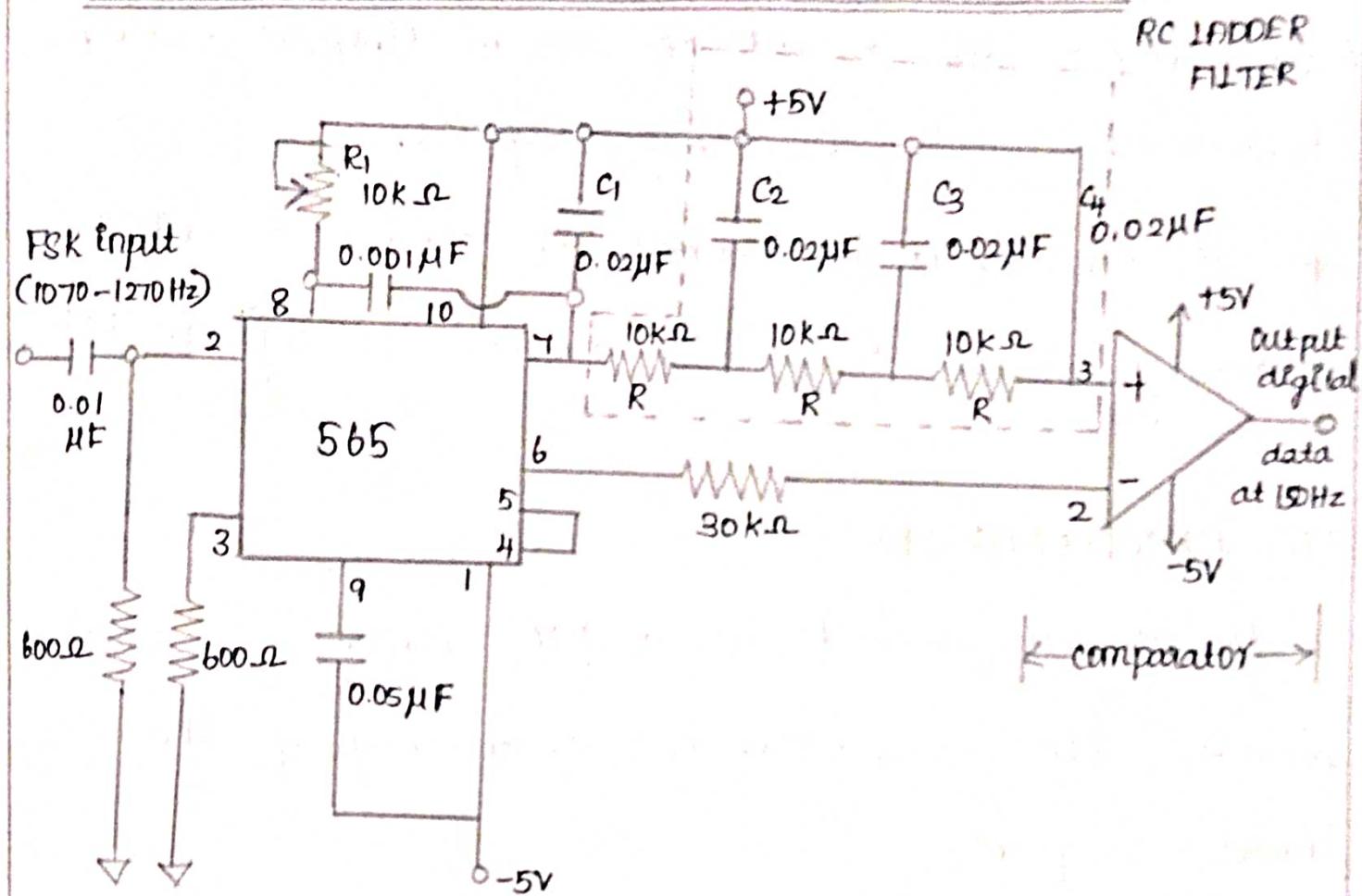
- * The PLL is locked to the carrier frequency of the incoming AM signal.
- * The output of VCO has the same frequency as the carrier but unmodulated is fed to the multiplier.
- * Since the VCO output is always 90° out of phase with incoming AM signal under locked condition, the input AM signal is also shifted in phase by 90° .

- * Both the signals applied to multiplexer are in same phase. The output of the multiplexer contains both sum and difference signals.
- * The demodulated output is obtained after filtering high frequency components by the LPF.

4. FM DEMODULATION:

- * If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal.
- * The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output.
- * Since VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

5. FREQUENCY SHIFT KEYING (FSK) DEMODULATOR:

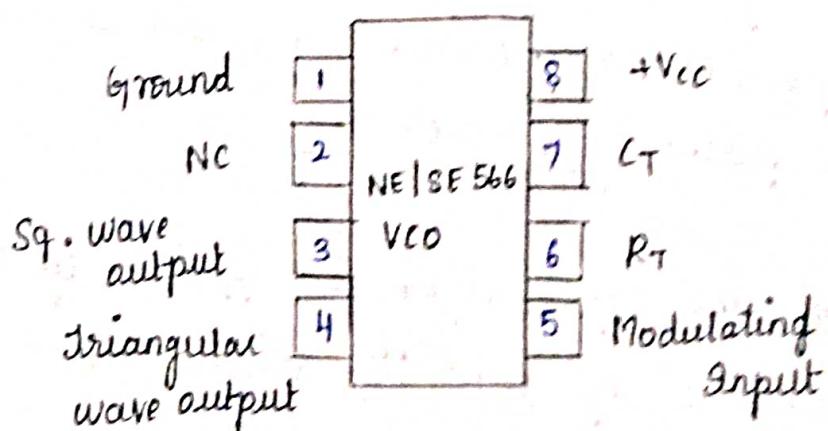


- * In digital data communication and computer peripheral, binary data is transmitted by means of carrier frequency which is shifted between two preset frequencies.
- * This type of data transmission is called frequency shifting keying (FSK) technique.
- * The binary data can be retrieved using a FSK demodulator at the receiving end.
- * The 565 PLL is very useful as a FSK demodulator.

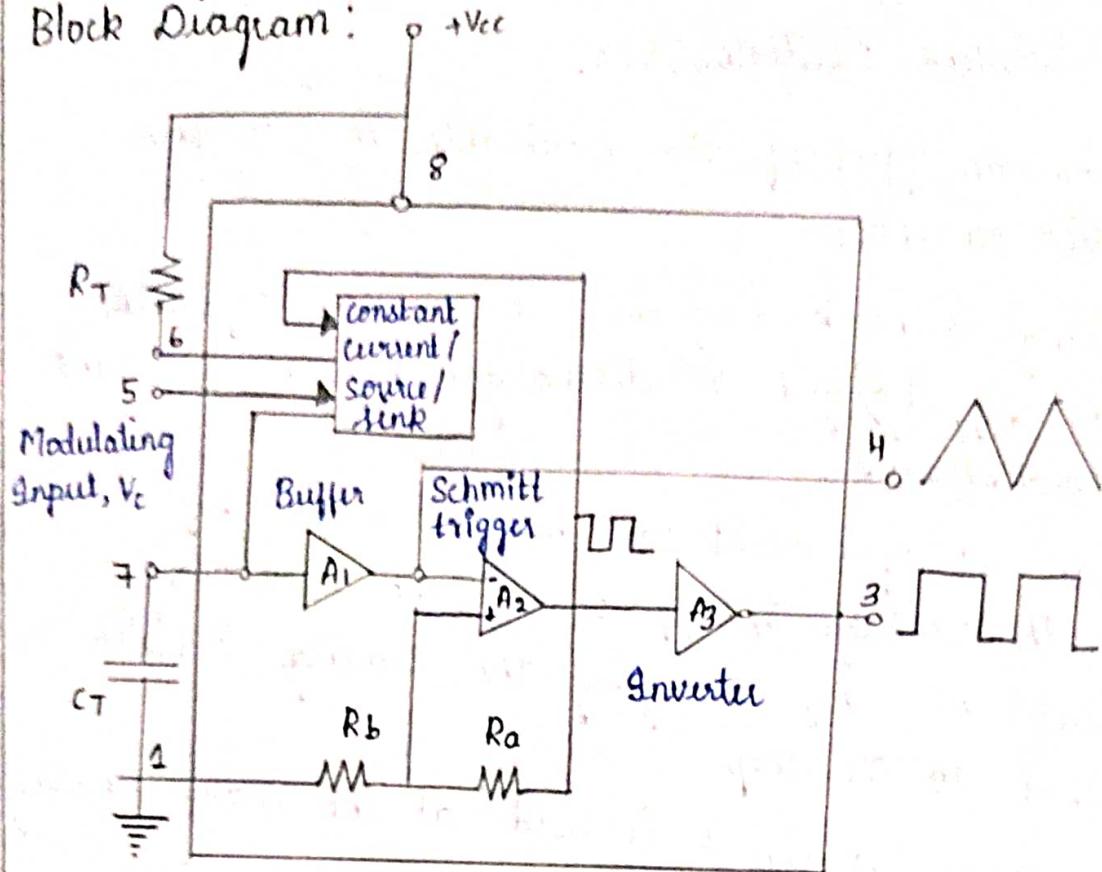
Voltage Controlled Oscillator (VCO)

- * A common type of VCO available in IC form is signetics NE/SE566
- * Referring to block diagram, a timing capacitor C_T is linearly charged or discharged by a constant current source / sink.
- * The amount of current can be controlled by changing the voltage V_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip.
- * The voltage at pin 6 is held at the same voltage as pin 5
- * Thus, if the modulating voltage at pin 5 is increased the voltage at pin 6 also increases resulting in less voltage across R_T and thereby decreasing the charging current.

Pin configuration



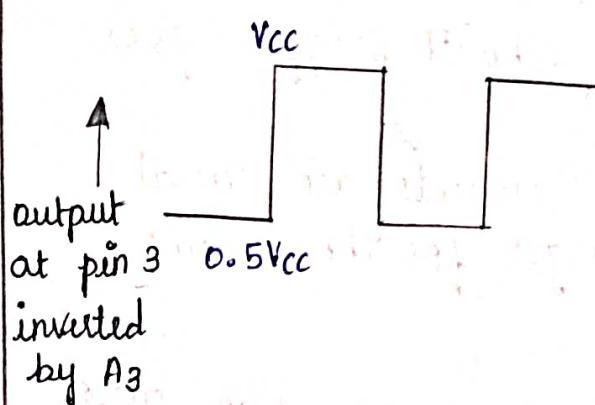
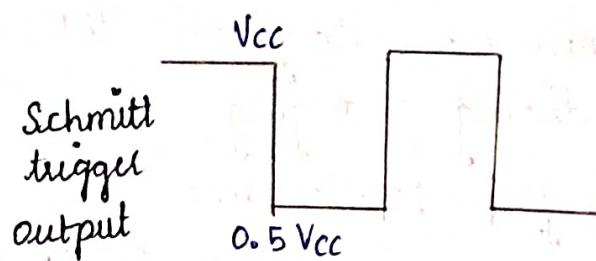
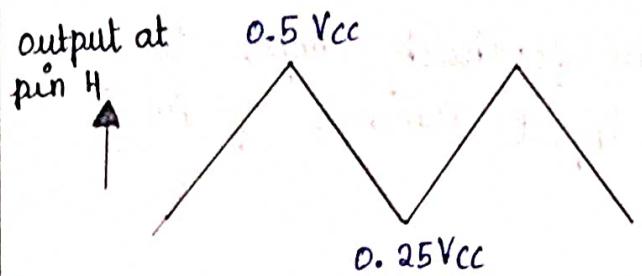
Block Diagram:



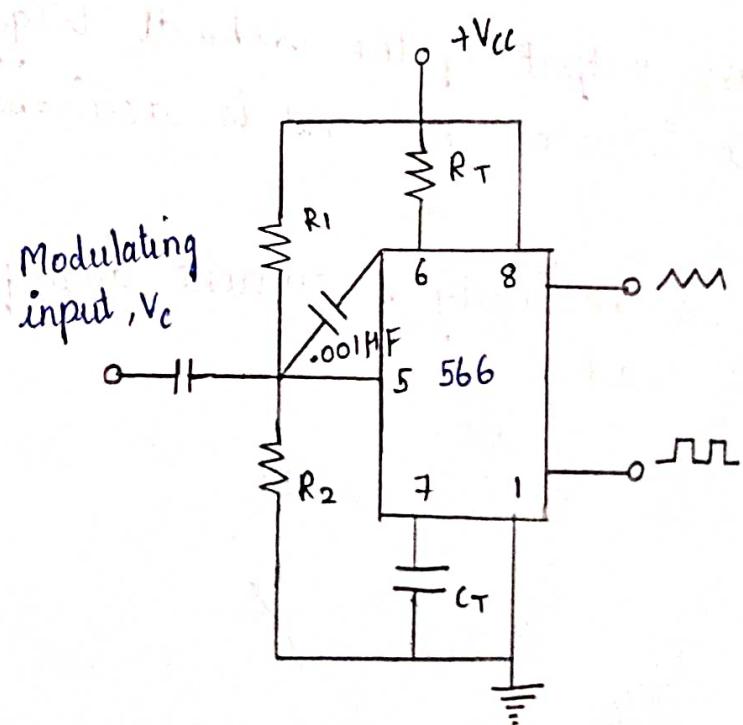
- * A small capacitor of .001 HF should be connected between pin 5 and 6 to eliminate possible oscillations.
- * A VCO is commonly used in converting low frequency signals such as EEG's EKG into an audio frequency range
- * These audio signals can be transmitted over telephone lines or a two way radio communication systems for diagnostic purposes or can be recorded on a magnetic tape for further reference.
- * The voltage across the capacitor C_T is applied to the inverting input terminal of schmitt trigger A_2 via buffer amplifier A_1 .

- * The output voltage swing of the schmitt trigger is designed to V_{cc} and $0.5V_{cc}$
- * If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from $0.5V_{cc}$ to $0.25V_{cc}$
- * In the output waveform, when the voltage on the capacitor C_T exceeds $0.5V_{cc}$ during charging, the output of the schmitt trigger goes LOW($0.5V_{cc}$)
- * The capacitor now discharges and when it is at $0.25V_{cc}$, the output of the schmitt trigger goes HIGH(V_{cc}).
- * Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time.
- * This gives a triangular voltage waveform across C_T which is also available at pin 4.
- * The square wave output of the schmitt trigger is inverted by the inverter A_3 and is available at pin 3
- * The inverter A_3 is basically a current amplifier used to drive the load.

Output waveforms:



Typical connection diagram



The output frequency of the VCO can be calculated as follows:

The total voltage on the capacitor changes from $0.25V_{cc}$ to $0.5V_{cc}$, thus $\Delta V = 0.25V_{cc}$.
The capacitor charges with a constant current source.

So,

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_T}$$

$$\frac{0.25V_{cc}}{\Delta t} = \frac{i}{C_T}$$

$$\Delta t = \frac{0.25V_{cc} C_T}{i} \rightarrow ①$$

The time period T of the triangular waveform $= 2\Delta t$
The frequency of oscillator f_0 is

$$f_0 = \frac{1}{T}$$

$$= \frac{1}{2\Delta t}$$

$$= \frac{i}{0.5V_{cc} C_T}$$

But

$$i = \frac{V_{cc} - V_c}{R_T} \rightarrow ②$$

where V_c is the voltage at pin 5

Therefore,

$$f_0 = \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}} \rightarrow ③$$

The output frequency of the VCO can be changed either by

i) R_T ii) C_T (or) iii) the voltage V_c at the modulating input terminal pin 5.

The voltage V_c can be varied by connecting a $R_1 R_2$ circuit

The components R_T and C_T are first selected so that VCO output frequency lies in the center of the operating frequency range.

Now the modulating input voltage is usually varied from $0.75V_{cc}$ to V_{cc} which can produce a frequency variation of about 10 to 1

With no modulating input signal, if the voltage at pin 5 is biased at $(\frac{7}{8})V_{cc}$ equation 3 gives the VCO output frequency as

$$f_o = \frac{2(V_{cc} - (\frac{7}{8})V_{cc})}{C_T R_T V_{cc}}$$

$$= \frac{1}{4R_T C_T}$$

$$= \frac{0.25}{R_T C_T} \rightarrow ④$$

Voltage to frequency conversion factor

A parameter of importance for VCO is voltage to frequency conversion factor K_V and is defined as

$$K_V = \frac{\Delta f_0}{\Delta V_c}$$

Here ΔV_c is the modulation voltage required to produce the frequency shift Δf_0 for the VCO. If we assume that the original frequency is f_0 and the new frequency is f_1 , then,

$$\Delta f_0 = f_1 - f_0$$

$$= \frac{2(V_{cc} - V_c + \Delta V_c)}{C_T R_T V_{cc}} - \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}}$$

$$= \frac{2 \Delta V_c}{C_T R_T V_{cc}}$$

or,

$$\Delta V_c = \frac{\Delta f_0 C_T R_T V_{cc}}{2}$$

putting the value of $C_T R_T$ from eqn (1)

$$\Delta V_c = \Delta f_0 V_{cc} / 8f_0$$

or,

$$K_V = \frac{\Delta f_0}{\Delta V_c} = \frac{8f_0}{V_{cc}}$$