4.15 DUAL SLOPE ADC

Dual slope conversion is an indirect method for A/D conversion where an analog voltage and reference voltage are converted into time periods by an integrator, and then measured by counter.

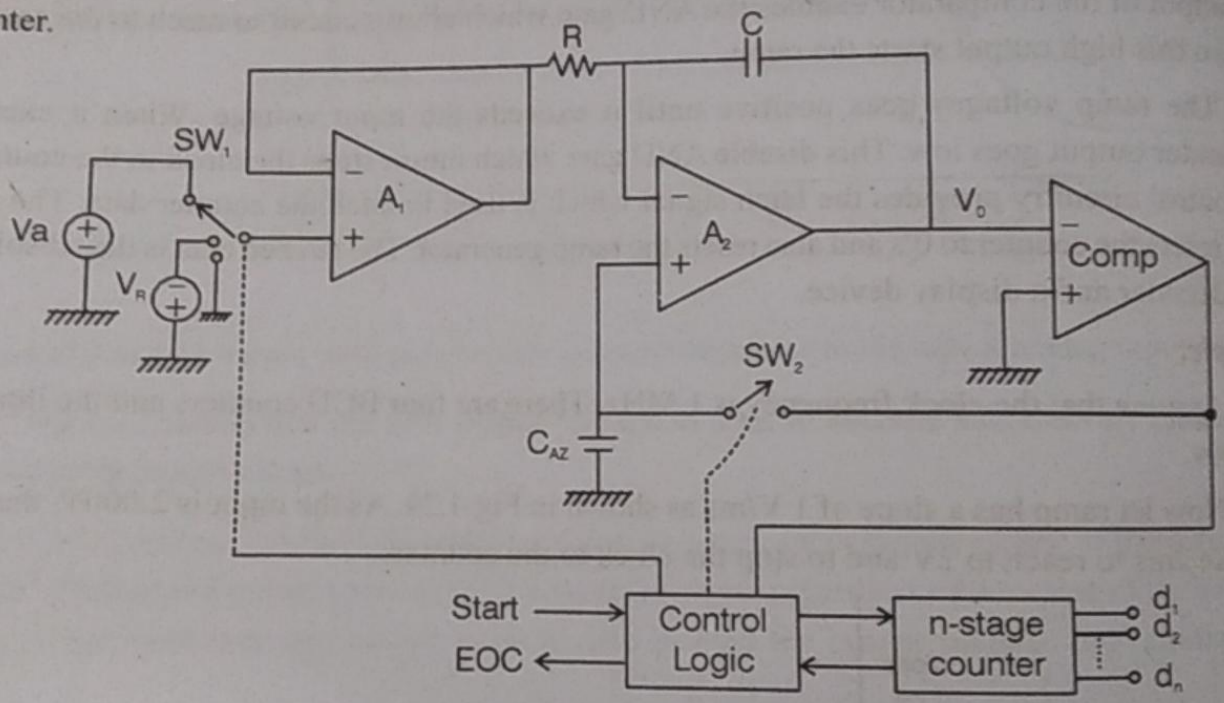

Fig.4.25 Functional diagram of the dual slope ADC

Fig.4.25 shows the functional diagram of the dual slope or dual ramp converter. The analog part of the circuit consists of a high input impedence buffer, A_1 precision integrator A_2 and a voltage comparator. The converter first integrates the analog input signal for a fixed duration of 2^n clock periods as shown in Fig.4.26. Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. The number N of clock cycles required to reduce the integrator to zero is proportional to the value of V_a averaged over the integration period. Hence N represents the desired output code. The circuits operates as follows.

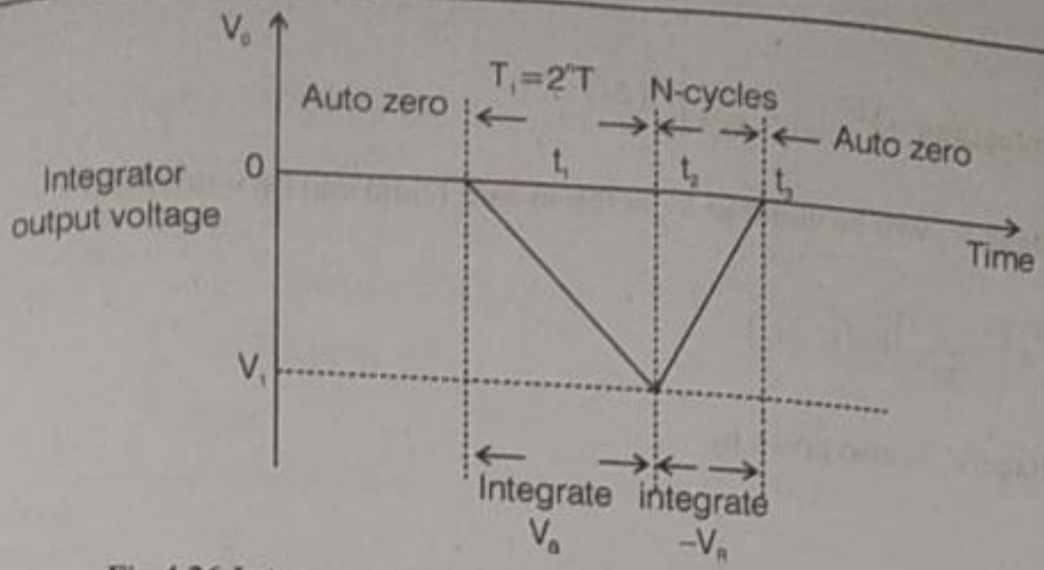

Fig.4.26 Integrated output waveform for the dualslope ADC

Operation :

- Before the START command arrives, the switch SW_1, is connected to ground and SW_2 is closed. Any offset voltage present in the A_1, A_2, comparator loop after integration appears across the capacitor C_{AZ} till the threshold of the comparator is achieved.
- The capacitor C_{AZ} thus provides automatic compenzation for the input offset voltages of all the three amplifier.
- Later, when SW_2 opens, C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled.
- At the arrival of the START command at $t = t_1$, the control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero.
- This circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses.
- The analog voltage V_a is integrated for a fixed number 2^n counts of clock pulses after which the coutner resets to zero. If the clock period is T, the integration takes place for a time $T_1 = 2^n \times T$ and the output is a ramp going downwards as shown in Fig.4.26.
- The counter resets itself to zero at the end of the internal T_1 and the switch SW_1 is connected to the reference voltage ($-V_R$). The output V_0 will now have a positive slope.
- As long as V_0 is negative, the output of the comparator is positive and the control logic allows the clock pulse to be counted. However, when V_0 becomes just zero at time $t = t_3$, the control logic issues an end of conversion (ECC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t_3 is proportional to the analog output voltage V_a.

In Fig. 4.26 $$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{Clock rate}}$$

$$t_3 - t_2 = \frac{\text{digital count N}}{\text{Clock rate}}$$

For an integrator, $\Delta V_0 = \left(-\frac{1}{RC}\right) V(\Delta t)$

The voltage V_0 will be equal to V_1 at the instant t_2 and can be written as

$$V_1 = \left(-\frac{1}{RC}\right) V_a (t_2 - t_1)$$

The voltage V_1 is also given by

at $t = t_2$

$$V_1 = \left(-\frac{1}{R_C}\right) - V_R (t_2 - t_3)$$

$$Va(t_2 - t_1) = V_R(t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$ we get

$$V_a (2^n) = V_R (N)$$

$$V_a = (V_R)\,(N/2^n)$$

1. Since V_R and n are constant, the analog voltage V_a is proportional to the count reading N and is independent of R, C and T.
2. The dual slope ADC integrates the input signal for a fixed time, hence it provides excellent noise rejection of ac signals whose periods are integral multiplies of the integration time T_1.

Disadvantage:

Long conversion time.

Dual slope converters are particularly suitable for accurate measurement of slowly varying signals such as thermocouples and weighing scales. Dual slope ADC's also form the basis of digital panel meter and multimeter.