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<div>DM&P</div> <div>M6117D SYSTEM ON CHIP</div> <div>SCHEMATIC SHEETS EXAMPLES</div> <div>REV 1.0</div> <div>September 24,1998</div>																					
<div>THE INFORMATION CONTAINED IN THESE SCHEMATIC SHEET IS PRELIMINARY AND SUBJECT TO CHANGE WITHOUT NOTICE. (DM&P)JAN YIN CHAN BEARS NO RESPONSIBILITY FOR ANY ERRORS IN THESE SCHEMATIC SHEETS.</div>																					
FILENAME		DESCRIPTION				REVISION HISTORY				HARDWARE CONFIGURATION:											
SOC1_1.SCH		M6117D MODE LIBRARY DESCRIPTION				REV 1.0 : RELEASE. 9/24/1998				DACK0 : PULL LO -- M6117D MODE , PULL HI -- M6117C MODE. DACK1 : (INTERNAL PULL HI) DACK2 : PULL LO -- EXTERNAL RTC ,PULL HI -- INTERNAL RTC. DACK3 : MUST BE PULLED HI (INTERNAL ALREADY PULL HI) DACK5 : MUST BE PULLED LO DACK6 : MUST BE PULLED HI (INTERNAL ALREADY PULL HI) DACK7 : (INTERNAL PULL HI) KESJ : MUST BE PULLED LO TC : MUST BE PULLED LO AEN : MUST BE PULLED HI											
SOC1_2.SCH		M6117C MODE LIBRARY DESCRIPTION								LINK SOC1_1.SCH SOC1_2.SCH SOC1_1.SCH SOC2_2.SCH SOC3_1.SCH SOC3_2.SCH SOC3_2.SCH SOC3_3.SCH SOC3_4.SCH SOC3_5.SCH SOC3_6.SCH SOC3_7.SCH SOC4_1.SCH SOC4_2.SCH SOC5_1.SCH SOC5_2.SCH SOC5_3.SCH SOC5_4.SCH SOC5_5.SCH											
SOC2_1.SCH		MINIMUM COMPONENT FOR M6117D																			
SOC2_2.SCH		MINIMUM COMPONENT FOR M6117D + ISA INTERFACE																			
SOC3_1.SCH		M6117D KERNEL + K.B./PS2 MOUSE + SPEAKER																			
SOC3_2.SCH		DRAM INTERFACE																			
SOC3_3.SCH		ISA BUS , PC/104 , IDE INTERFACE																			
SOC3_4.SCH		PROGRAMABLE CHIP SELECT SCHEMATIC EXAMPLES(GPCSO..1)																			
SOC3_5.SCH		GENERAL PURPOSE I/O SCHEMATIC EXAMPLES (GPO..15)																			
SOC3_6.SCH		SERIAL INTERFACE																			
SOC3_7.SCH		ETHERNET INTERFACE (RTL8019AS)																			
SOC4_1.SCH		SINGLE CHIP PC																			
SOC4_2.SCH		SINGLE CHIP PC CONNECTOR																			
SOC5_1.SCH		DELVLOPMENT DEMO BOARD FOR 'SINGLE CHIP PC'																			
SOC5_2.SCH		DELVLOPMENT DEMO BOARD MULTI I/O (ALI M5113)																			
SOC5_3.SCH		DELVLOPMENT DEMO BOARD DiskonChip/ROM/FLASHDISK																			
SOC5_4.SCH		DELVLOPMENT DEMO BOARD VGA CONTROLLER (HMC HM86508)																			
SOC5_5.SCH		DELVLOPMENT DEMO BOARD VGA DRAM + LCD INTERFACE																			
<div>DM&P JAN YIN CHAN ELECTRONICS CO.LTD.</div> <div>AUTHORS : Gen He CHAN.</div> <div>Doc M6117D EXAMPLE SCHEMATIC INDEX</div> <table><tr><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td>B</td><td>SOC.SCH(SYSTEMONCHIP)</td><td>1.0</td></tr></table> <div>Date: Thursday, May 03, 2002Sheet 1 of 19</div>																Size	Document Number	Rev	B	SOC.SCH(SYSTEMONCHIP)	1.0
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B	SOC.SCH(SYSTEMONCHIP)	1.0																			
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