

# Roofline and Matrix Multiplication PAPI Analysis

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# Sources for Machine Specifications

Sources used for a complete profile:

**Linux System Information** (/proc/cpuinfo, /proc/meminfo) To gather specifications on hardware;

**Web** (ark.intel.com, crucial.com) For micro architecture and memory specifications;

**Linux Tools and Packages** (dmidecode, sysctl, bandwidth) To gather memory, cpu and bandwidth info;

# Machines Specs

<b>Manufacturer:</b>	Apple
<b>Model:</b>	MacBook Pro late 2008
<b>Processor</b>	
Manufacturer:	Intel
Arch:	Core
Model:	Core 2 Duo T9600
Cores:	2
Clock Frequency:	2.80 GHz
FP Performance's Peak:	44.8 GFlops/s

Table : MacBook Pro late 2008 specifications

# Machines Specs

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## Cache

Level:	1
Size:	32KB + 32KB
Line Size:	64 B
Associative:	8-way
Memory Access Bandwidth:	40 GB/s

Level:	2
Size:	6 MB
Line Size:	64 B
Associative:	24-way

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## RAM

Type:	SDRAM DDR3 PC3-8500
Frequency:	1067 MHz
Size:	4 GB
Num. Channels:	2
Latency:	13.13 ns

Table : MacBook Pro late 2008 specifications

# Machines Specs

<b>Manufacturer:</b>	HP
<b>Model:</b>	Pavillion dv6-2190ep
<b>Processor</b>	
Manufacturer:	Intel
Arch:	Nehalem
Model:	i7-720QM
Cores:	4
Clock Frequency:	1.60 GHz
FP Performance's Peak:	51.2 GFlops/s

Table : HP Pavillion dv6-2190ep specifications

# Machines Specs

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## Cache

Level:	1
Size:	32KB + 32KB
Line Size:	64 B
Associative:	4/8-way
Memory Access Bandwidth:	22 GB/s

Level:	2
Size:	256 KB
Line Size:	64 B
Associative:	8-way

Level:	3
Size:	6 MB
Line Size:	64 B
Associative:	12-way

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## RAM

Type:	SDRAM DDR3 PC3-10600
Frequency:	1333 MHz





# Problem

Analyse the performance of a **matrix multiplication** algorithm,

$$\text{MatrixA} * \text{MatrixB} = \text{MatrixC} \quad (1)$$

which contains a triple nested loop with the indexes  $i, j$  and  $k$  (line, column and position).

The implementation used runs two versions of the problem, one multiplying matrixA with matrixB, and another multiplying matrixA with the transpose of matrixB.

# Algorithm

Standard implementation of a matrix multiplication in C.

```
for (i = 0; i < size; i++) {  
    for (j = 0; j < size; j++) {  
        for(k = 0; k < size; k++) {  
            acc += matrixA[i][k] * matrixB[k][j];  
        }  
        matrixC[i][j] = acc;  
        acc = 0;  
    }  
}
```

# Counters Used

Used counters gathered by PAPI:

PAPI\_TOT\_CYC Total cycles;

PAPI\_TOT\_INS Total instructions

PAPI\_LD\_INS Load Instructions

PAPI\_SR\_INS Store Instructions

PAPI\_FML\_INS Multiply instructions

PAPI\_FDV\_INS Division instructions

PAPI\_VEC\_INS Vector Instructions

PAPI\_FP\_OPS Floating point operations

PAPI\_L1\_DCA L1 data cache accesses

PAPI\_L1\_DCM L1 data cache misses

PAPI\_L2\_DCA L2 data cache accesses

PAPI\_L2\_DCM L2 data cache misses

# Test cases

Test cases were selected to fit on the multiple memory levels.  
Each Test case was run 4 times for each version of the problem.

Memory	Size	Matrix Size
L1	30 KB	50
L2	255 KB	146
L3	3 MB	500
RAM	7.68 MB	800

Table : Test cases

# Memory Accesses

The following table shows the number of memory accesses, through PAPI readings.

Test	PAPI	Accesses/Inst
L1_1	380844	0.49033
L1_2	258412	0.33270
L2_1	9411279	0.42860
L2_2	6318058	0.33449
L3_1	7761996	0.00885
L3_2	152192	0.00020

# Conclusion

- Some difficulties measuring memory ceilings;
- Lack of analysis of output from PAPI;

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