1 Roofline

1.1 Machines Profile

The machines used for this study were a MacBook Pro late 2008 and a HP dv6-2190ep from 2010. The information about the machines were gathered from */proc/cpuinfo*, */proc/meminfo*, the *Intel Ark* and *Crucial* websites and with *dmidecode* and *sysctl* linux tools.

1.1.1 Peaks

In order to calculate the rooflines, we needed the Floating-Point(FP) Performance's Peak and the Memory Bandwidth's Peak. To attain the FP Performance's Peak we calculate the following formula:

$$\text{GFlop/s}_{\text{max}} = \#_{\text{cores}} \times f_{\text{clock}} \times \#_{\text{SIMD}}$$

To calculate de Memory Bandwidth's Peak we resolve the following formula:

$$\text{BW}_{\text{max}} = \#_{\text{channels}} \times mem_{\text{clock}} \times bus_{\text{bandwidth}}$$

1.1.2 Specifications

The specifications of the MacBook Pro are displayed on Table 1.

The specifications of the HP dv6-2190ep are displayed on Table 2.

1.2 Roofline Model

1.2.1 Machines' Roofline

IMAGEM MBP
IMAGEM HP

1.2.2 Ceilings

As suggested by the Roofline paper we added several ceilings to understand wich optimizations we may perform. This ceilings were given by recalculating the roofline without some key charateristics.

Peak floating-point performance The roofline, where all components and features are considered.

For memory only one ceiling was calculated, besides the roofline.

Peak stream bandwidth The roofline, where all features are considered.

One-channel

Manufacter:	Apple
Model:	MacBook Pro late 2008

Processor

Manufacturer:	Intel
Arch:	Core
Model:	Core 2 Duo T9600
Clock Frequency:	2.80 GHz
FP Performance's Peak:	44.8 GFlops/s

Cache

Level:	1
Size:	32KB + 32KB
Line Size:	64 B
Associative:	8-way
Memory Access Bandwidth:	VER ISTO !!!!!!!!!!

Level:	2
Size:	6 MB
Line Size:	64 B
Associative:	24-way

RAM

Type:	VER ISTO !!!!!!!!!
Frequency:	VER ISTO !!!!!!!!!
Size:	VER ISTO !!!!!!!!!
Num. Channels:	2
Latency:	VER ISTO !!!!!!!!!!

Tabela 1: MacBook Pro late 2008 specifications

Manufacter:	HP
Model:	Pavillion dv6-2190ep

Processor

Manufacturer:	Intel
Arch:	Nehalem
Model:	i7-720QM
Clock Frequency:	1.60 GHz
FP Performance's Peak:	51.2 GFlops/s

Cache

Level:	1
Size:	32KB + 32KB
Line Size:	64 B
Associative:	4/8-way
Memory Access Bandwidth:	VER ISTO !!!!!!!!!!

Level:	2
Size:	256 KB
Line Size:	64 B
Associative:	8-way

Level:	3
Size:	6 MB
Line Size:	64 B
Associative:	12-way

RAM

Type:	SDRAM DDR3 PC3-10600
Frequency:	1333 MHz
Size:	4GB
Num. Channels:	2
Latency:	VER ISTO !!!!!!!!

Tabela 2: HP Pavillion dv6-2190ep specifications

2 PAPI Case Study

2.1 Problem

The case study of this report, is to analyse the performance of a **matrix multiplication** algorithm,

$$MatrixA * MatrixB = MatrixC \tag{1}$$

wich contains a triple nested loop with the indexes i,j and k(line,column and position). Our implementation will explore the index order **i,j,k** of the triple nested loop.

2.2 Algorithm Analysis

The algorithm produced to calculate the matrix multiplication is:

```
for (i = 0; i < size; i++) {
    for (j = 0; j < size; j++) {
        for(k = 0; k < size; k++) {
            acc += matrixA[i][k] * matrixB[k][j];
            }
            matrixC[i][j] = acc;
            acc = 0;
        }
    }
```

2.3 Counters Used

2.4 Tests

2.5 Results

2.5.1 Analysis Miss Rates

2.5.2 Analysis Memory Access