GMetis - Xeon Phi

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Outline

Introduction

- Blabla
- Bleble

Stampede Host

Manufacturer	Intel
Model	Xeon E5-2680
μArch	Sandy Bridge
Clock freq	2.70 GHz
#CPUs (sockets)	2
#Cores/CPU	8
#Thread/Core	1
L1 cache size/core	32 KB
L2 cache size/core	256 KB
L3 shared cache size/CPU	20 MB
Vector width	256 bits (AVX)

Table 1 : Intel Xeon E5-2680

Stampede Coprocessor

Manufacturer	Intel
Model	Xeon E5-2680
μArch	Sandy Bridge
Clock freq	1.1 GHz
#CPUs (sockets)	1
#Cores/CPU	61
#Thread/Core	4
L1 cache size/core	32KB
L2 cache size/core	512 KB
Vector width	512 bits

Table 2 : Intel Xeon Phi

Important characteristics

- Dual issue pipeline
- Four hardware threads per core
- Pipeline does not issue instructions from the same hardware context for two consecutive clock cycles
- Maximum issue rate only attainable with at least 2 threads per core

Number of Hardware Threads per core	Minimum Theoretical CPI per Core
1	1
2	0.5
3	0.5
4	0.5

Table 3 : Minimum Theoretical CPIs

Conclusion

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Questions & Discussion