HOMEWORK : 02
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Question : 01

1. Transient simulations for NMOS and PMOS, to find the R_{eq} (L = 0.18um process)

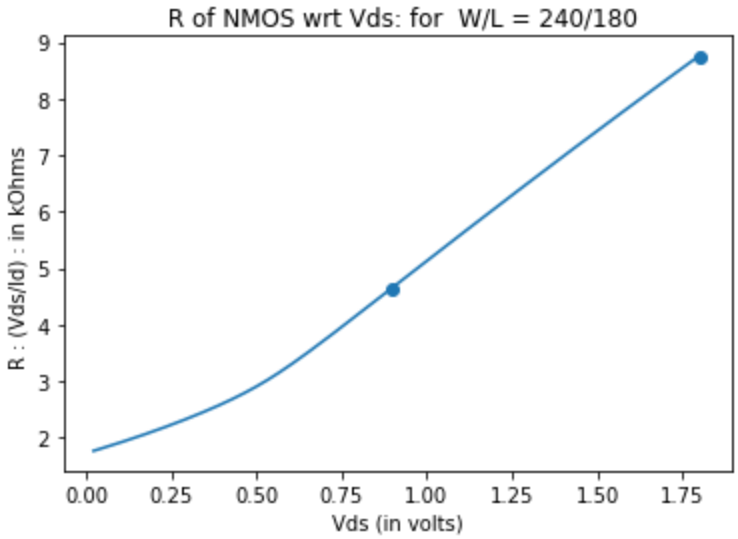
$$\mathbf{R_{eq} \sim (R_{Vdd} + R_{Vdd/2})/2}$$

1.1 NMOS : For Vdd = 1.8V

```
*** For Ques: 1. NMOS
*** Vgs = 1.8V, init Vds = 1.8V.,

** M1 --> 1. W/L = 240/180
** M2 --> 2. W/L = 400/180


.include TSMC180.lib
.model nch_tt nmos (level = 8)

Vgs    g      0      1.8
V_am d      am     0V     ** ammeter
C      am     0      1e-12          IC = 1.8V
*M1    d      g      0      0  nch_tt   W=240n  L = 180n
M2     d      g      0      0  nch_tt   W=400n  L = 180n


.ic V(am) = 1.8V
.control

tran 1p  13n
*plot V(am)
*plot -i(V_am) vs V(am)  title "I vs V"
plot V(am)/-i(V_am) vs V(am) title " Res vs V: M1 "
wrdata 1.a.n.2.dat V(am)  V(am)/-i(V_am)
```

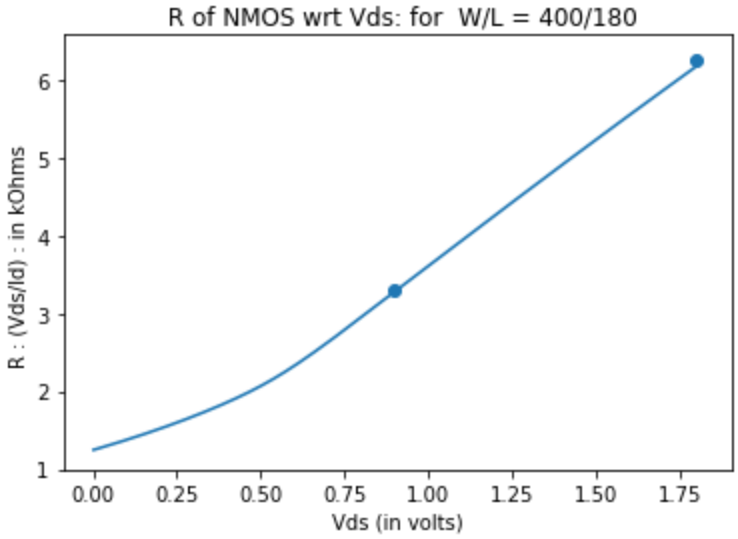
```
.endc
.end
```

1.1.1 W/L = 240/180



Calculating R_{eq} = (8.8 + 4.7)/2 = **6.75 kOhm**

1.1.2 W/L = 400/180

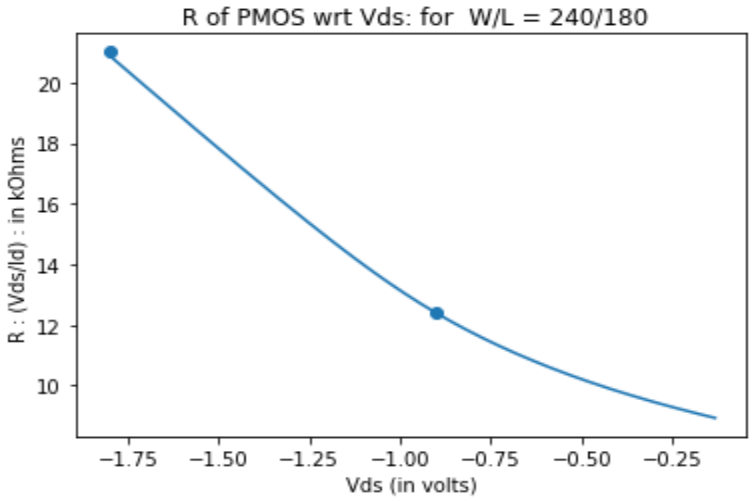


Calculating R_{eq} = (6.2 +3.36)/2 = **4.78 kOhm**

1.2 : PMOS : for V_{dd} = -1.8V

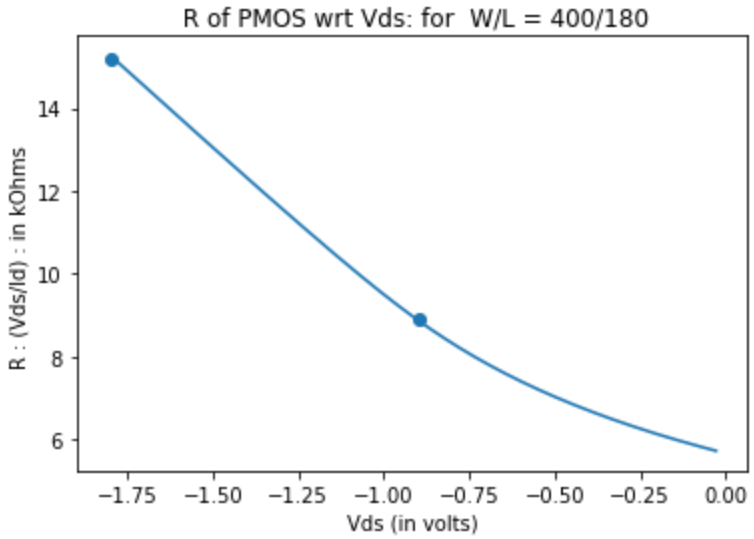
```
*** For Ques: 1. PMOS
*** Vgs = -1.8V, init Vds = -1.8V.,
** M1 --> 1. W/L = 240/180
** M2 --> 2. W/L = 400/180

.include TSMC180.lib
.model pch_tt pmos (level = 8)

Vgs    g       0       -1.8
V_am d       am      0       ** ammeter
C       am      0       1e-12           IC = -1.8V
*M1    d       g       0       0  pch_tt   W=240n  L = 180n
M2     d       g       0       0  pch_tt   W=400n  L = 180n

.ic V(am) = -1.8V

.control

tran .5p  30n
*plot -V(am)
*plot -i(V_am) vs V(am)  title "I vs V"
plot V(am)/-i(V_am) vs V(am) title " Res vs V: M1 "
wrdata 1.a.p.2.dat V(am)  V(am)/-i(V_am)

.endc
.end
```

1.2.1 W/L = 240/180



Calculating R_{eq} = (21 + 12.4)/2 = **16.7 kOhm**

1.2.2 : W/L = 400/180



Calculating R_{eq} = (15.2 +8.9)/2 = **12.05 kOhm**

b) Results for different Vdd **: Trend of R_{eq} w.r.t V_{dd}**

By doing analysis for different V_{dd} :(initial capacitor voltage and V_{gs}). The below are the results for R_{eq} at different Vdd.

For W/L : 240/180

| Vdd | (in V)	Req for NMOS (k Ohm)	Req for PMOS(k Ohm)
1.8	**6.75**	**16.7**
1.5	**7.53**	**21.8**

1.2	9.3	32.6
0.9	14.47	62.5
0.6	63.5	251

For W/L : 400/180 :

| Vdd | (in V)	Req for NMOS (k Ohm)	Req for PMOS(k Ohm)
1.8	4.78	12.05
1.5	5.375	15.25
1.2	6.75	22.1
0.9	10.55	40.65
0.6	51.3	193.7

Observations :

1. We can see that there is a deviation with the values mentioned in the Textbook , where results are produced for (W/L = 1).
2. R_{eq} is inversely proportional to (W/L) ratio.
3. We can observe that when we scale the obtained R_{eq} with (W/L) we get the values closer to that of the TB values.

4. Although there will be differences, since the simulation is done for a 0.25u process (in the TB), while we performed for a 0.18u process
5. Another observation is that R_{eq} of PMOS is relatively high when compared to that of NMOS for the same V_{dd} , reason being that since PMOS works with the mobility of holes which is less when compared to the mobility of electrons in NMOS. This will result in less current , which is seen as a high resistance in PMOS devices.
6. R_{eq} decreases as V_{dd} increases, and reaches a constant low value for high V_{dd} . As V_{dd} increases, the mosfet moves from : Cutoff to saturation region. At cutoff very less current flows , and seen as high resistance. And for high V_{dd} , it reaches saturation, where current is constant and high and does not depend on Vgs. This is seen as a low ON resistance.

Question : 02

MOSFET Capacitance

$V_{app} = V_{CM} + (1/(2.pi.f))\ \sin(wt)$

$I_g = C*\cos(wt)$

The amplitude of the gate current gives the gate capacitance.

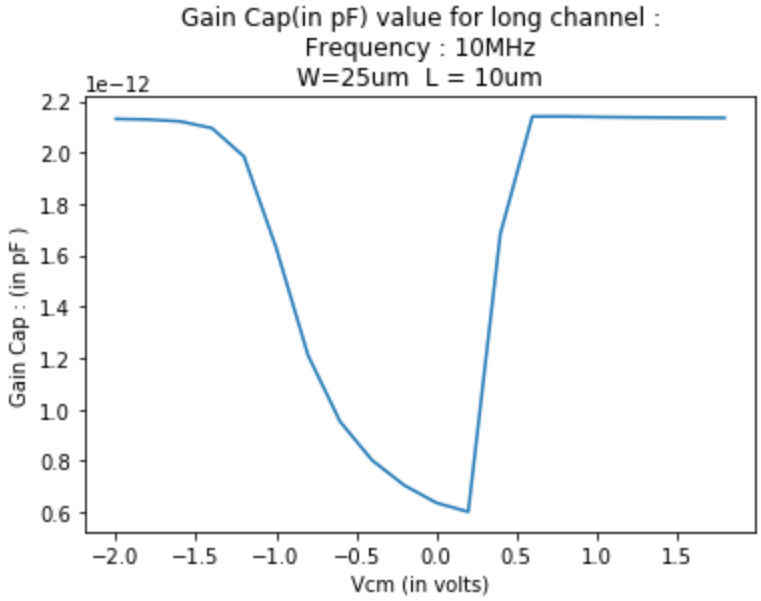
A. CV CHARACTERISTICS :

```
*** For Ques: 2 NMOS
*** Vgs = Vcm + sin(wt),  Vds = 0V.,  sweeping vcm

** M1 --> 1. long channel
** M2 --> 2. short channel


.include TSMC180.lib
.model nch_tt nmos (level = 8)
.param f= 10e6
*.param f = 10e9
Vgs     g       a       dc 0  SIN(0 {1/(2*3.14*f)} f 0 0 0 )
Vcm     a       0       -2V
*Ml     0       g       0       0       nch_tt   W=25u  L = 10u
Ms      0       g       0       0       nch_tt  W = 450n L=180n

.control
let v = -2
let v_vec = vector(20)
let c_vec = vector(20)
let loop = 0
while v <1.8
        alter @Vcm v

        tran 1n 1u
        *tran .1p 10n

        meas tran i_max FIND i(Vcm) AT = 1u
        *meas tran i_max FIND i(Vcm) AT = 10n

      print v
        *plot i(Vcm)   xlabel "Current at Vcm =  $&v"

        let v_vec[loop] = v
        let c_vec[loop] = -i_max
```

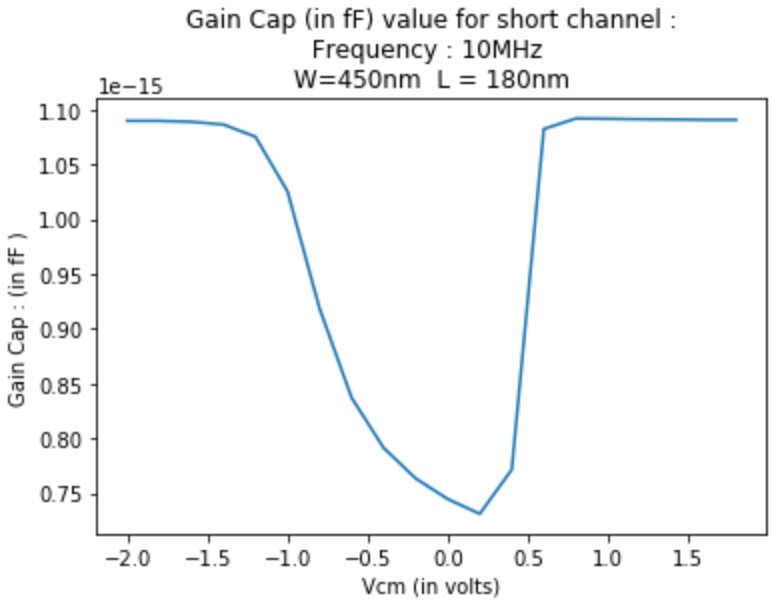
```
        let v = v + 0.2
        let loop  = loop + 1

end

plot c_vec vs v_vec
wrdata 2.b.dat c_vec vs v_vec
.endc
.end
```

Generating C vs V_{cm} graph.
Frequency : 10MHz

A.1. W/L = 2.5,: Long channel L = 10µm ,W = 25µm.



A.2. Short channel : L = 180nm, W = 450nm



OBSERVATIONS

1.Long channel capacitance (pF) is higher than short channel capacitance(fF).

2.The highest value depends on C_{OX} * W * L . Hence it is evident that long channels have a higher cap in order than short channels.

3.The overlap capacitance comes into picture in the short channel case (since it's very small).

Explaining the graph :

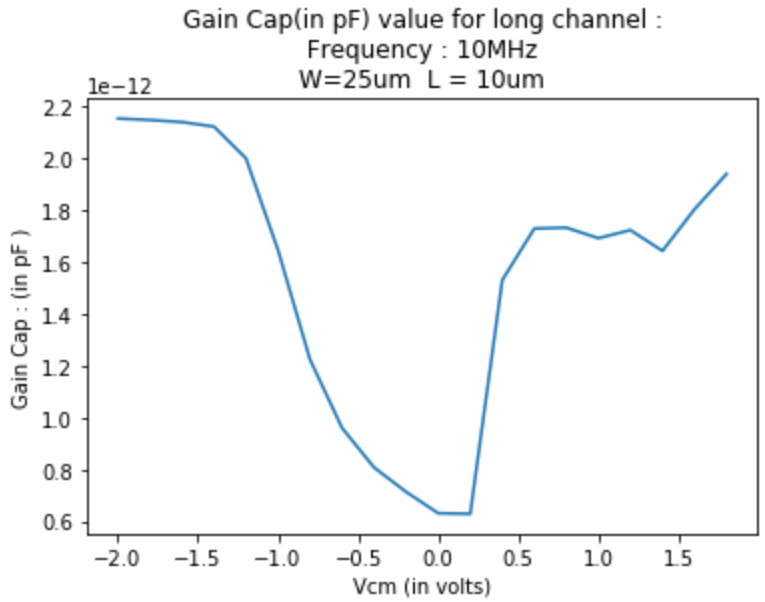
3.1 Cutoff : The Gate-Bulk cap (C_{GBS}) accounts for the left side of the graph (< 0V) , which gradually reduces as Vcm (i.e;Vgs) increases , due to the formation of channel .

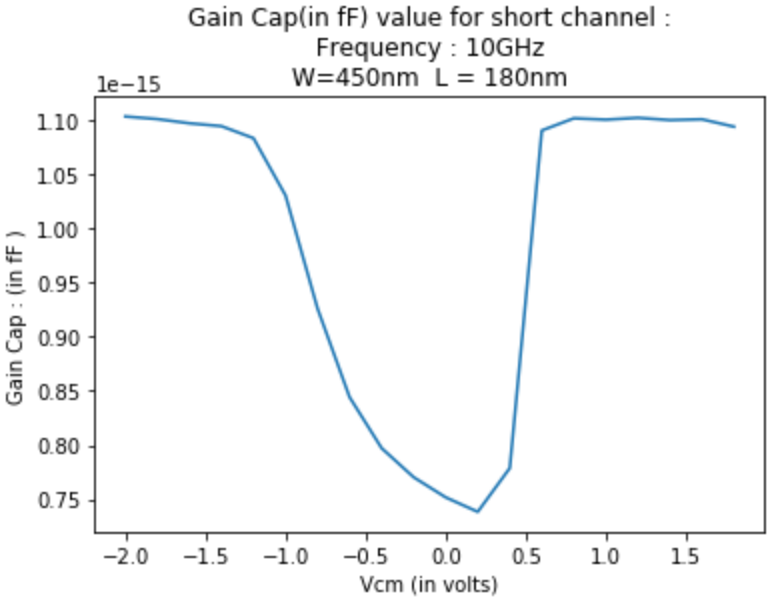
3.2 Linear : A complete channel is formed , later on the capacitance is provided by the source and the drain equally and C_{GBS} ceases to exist.

B) Low vs High Frequency :

Plots for 10MHz are shown above.

Plots for 10 GHz





Observations :

1. We can see that both plots are almost identical with a similar range.
2. Long channel continuous to be in pF range, and short channel in fF range. (due to its dependence on W*L).
3. Due to abundant charges provided by source and the drain , we are able to find similar plots at different frequencies , unlike a MOSCAP, which shows different characteristics due to absence of drain and source.

Question : 03

3@)

$V_{TN} = |V_{TP}| = 0.3V$

$V_{DD} = 1.2V$

a) which one consumes static power? at high input?

→ (i), (ii), (iii).

CMOS (iv), has no current flow due to presence of a PMOS (at OFF state)

Another cases, since NMOS is ON current flows ⇒ static power consumed

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b) Static power at low input?

⇒ None

→ No current is drawn, since ~~PMOS~~ NMOS are off state in every case

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(c) $V_{OH} = 1.2V$?

(i) (ii) (iv)

⇒ (i) MOS is off ⇒ no current

⇒ $V_{out} = 1.2V$ ✓

⇒ (ii) NMOS at bottom requires

no current ⇒ $V_{GS} - V_T = 0$ (of top NMOS)

⇒ $V_{out} = 0.9V$ ✗

⇒ (iii) No current a bottom

$V_{GS} = V_T = 0V$

⇒ $V_S = V_{out} = 1.2V$ ✓

⇒ (iv) NMOS is open ⇒

no current is allowed

⇒ $V_{out} = 1.2V$ ✓

(d) $V_{OL} = 0V$?

(iv)

Reason: Since both

For i, ii, iii ⇒ current is drawn

⇒ Vout is found by voltage divider network. ⇒ Hence $V_{out} \neq 0$

For CMOS:

PMOS is open ⇒ $V_{out} = 0$

(e) (i) (ii) (iii)

All except CMOS are dependent on size of devices

Question 04

Q4) NMOS inverter.

a) V_{OH} ⇒ Since $V_{IN} = 0V$

⇒ No major current ⇒ ~~Major drop across~~ R_L

⇒ $\boxed{V_{out} = 2.5V}$ ⇒ V_{OH}

* V_{OL} :- $V_{IN} = 2.5V\ (V_{DD})$

* Here NMOS in linear region.

$$\frac{k'W}{L}\left((V_{GS}-V_T)V_{OL} - \frac{V_{OL}^2}{2}\right) = \frac{V_{DD}-V_{OL}}{R_L}$$

$$\Rightarrow \quad k' = 345\times10^{-6}$$

$$\Rightarrow (345\times10^{-6})(75\times10^{3})\left(2.07V_{OL} - \frac{V_{OL}^2}{2}\right) = \frac{2.5-V_{OL}}{R_L}$$

$$\Rightarrow (25.87)\left(2.07V_{OL} - \frac{V_{OL}^2}{2}\right) = 2.5 - V_{OL}$$

$$\rightarrow \boxed{V_{OL} = 46.33\ mV}$$

* V_M :- $V_{IN} = V_{out}$

⇒ k'_n (NMOS in saturation)

⇒ $\frac{k'_n W}{2L}(V_M - V_T)^2 = \frac{V_{DD} - V_M}{R_L}$

⇒ $172.5 \times 10^{-6}(V_M - 0.43)^2 = \frac{2.5 - V_M}{75 \times 10^3}$

⇒ $12.9(V_M - 0.43)^2 = 2.5 - V_M$

⇒ Solving the Quad eqn.

⇒

$$\boxed{V_m = 0.79\ V}$$

(b) * V_{IL}, V_{IH} = ?

For V_{IL}, V_{IH} $\Rightarrow$ $\frac{dV_{out}}{dV_{IN}} = -1$

(•) V_{IL} (NMOS is saturation rgn).

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k'W}{2L}(V_{IN} - V_T)^2$$

$\Rightarrow$ Deriving wrt. V_{in}

$$\Rightarrow \frac{-1}{R_L}\left(\underbrace{\frac{dV_{out}}{dV_{IN}}}_{-1}\right) = \frac{k'W}{2L}(2)(V_{IN} - V_T)$$

$$\Rightarrow \frac{1}{R_L} = \frac{k'W}{L}(V_{IN} - V_T)$$

$$\Rightarrow V_{IL} = V_{IN} = \frac{1}{k'WR_L} + V_T$$

$$= \frac{10^6}{(1035)*(15\times10^3)} + 0.43$$

$\Rightarrow$

$$\boxed{V_{IL} = 0.468\ V}$$

$V_{IL} = 0.468V$

* V_{IH} (NMOS in linear rgn)

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{K'W}{L}\left[(V_{IN} - V_T)V_{out} - \frac{V_{out}^2}{2}\right] \rightarrow (1)$$

$$\rightarrow \frac{-1}{R_L}\frac{dV_{out}}{dV_{in}} = \frac{K'W}{L}\left[(V_{IN} - V_T)\frac{dV_{out}}{dV_{IN}} + V_{out} - 2\frac{V_{out}}{2}\frac{dV_{out}}{dV_{in}}\right]$$

$$\Rightarrow \frac{1}{R_L} = \frac{K'W}{L}\left[V_T - V_{in} + 2V_{out}\right]$$

$$\Rightarrow \frac{L}{R_L K'W} = V_T - V_{IN} + 2V_{out}$$

$$\Rightarrow V_{in} = V_T + 2\cdot V_{out} - \frac{L}{R_L K'W} \rightarrow (2)$$

$\Rightarrow$ Solving (2), (1) =

$$\Rightarrow 2.5 - V_{out} = \frac{R_L K'W}{L}\left[\left(2V_{out} - \frac{L}{R_L K'W}\right)V_{out} - \frac{V_{out}^2}{2}\right]$$

On Solving this;

$V_{out} = 0.253\ V$

$\Rightarrow V_{IH} - V_{in} = 2V_{out} + V_T - 0.012$

$\Rightarrow V_{IH} = V_{in} = 0.899\ V$

B) contd. **Noise margin**

$N_{MH} = V_{OH} - V_{IH} = 2.5 - 0.9$

$= 1.6\ V$

$N_{ML} = V_{IL} - V_{OL}$

$= 0.468 - 0.046$

$= 0.42\ V$

(e) Peak gain ⇒ happens at V_M

($V_{IN} = V_{out}$) ⇒ Saturation rgn

$$\frac{k'W}{2L}(V_M - V_T)^2 = \frac{V_{DD} - V_{out}}{R_L}$$

$$\Rightarrow \left.\frac{\partial V_{out}}{\partial V_{in}}\right|_{V_{in}=V_M} \Rightarrow \text{gain}$$

$$\Rightarrow \frac{k'W}{2L}\left(2(V_M - V_T)\right) = \frac{-1}{R_L}\left(\frac{\partial V_{out}}{\partial V_{in}}\right)$$

$$\Rightarrow \frac{-R_L k'W}{L}(V_M - V_T) = \text{gain (peak)}$$

Solving

Peakgain : $\Rightarrow 25.875\,(0.793 - 0.43)$

$\rightarrow 9.38\,V$

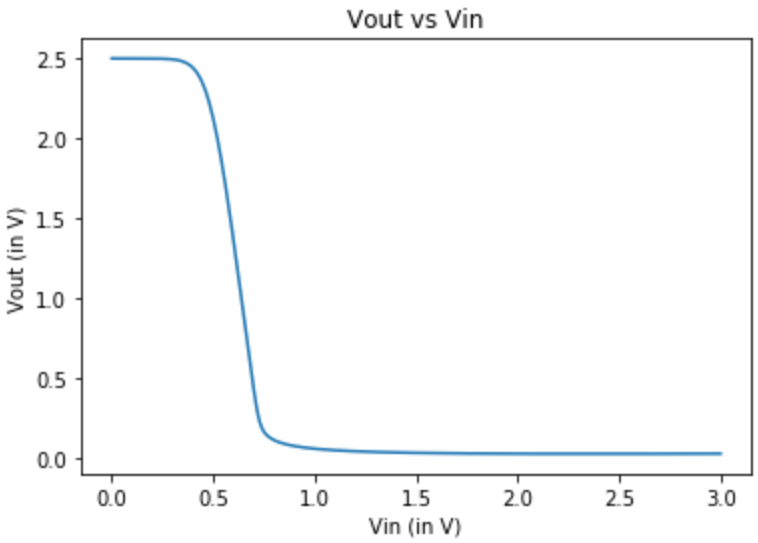
Peakgain = −9.38V

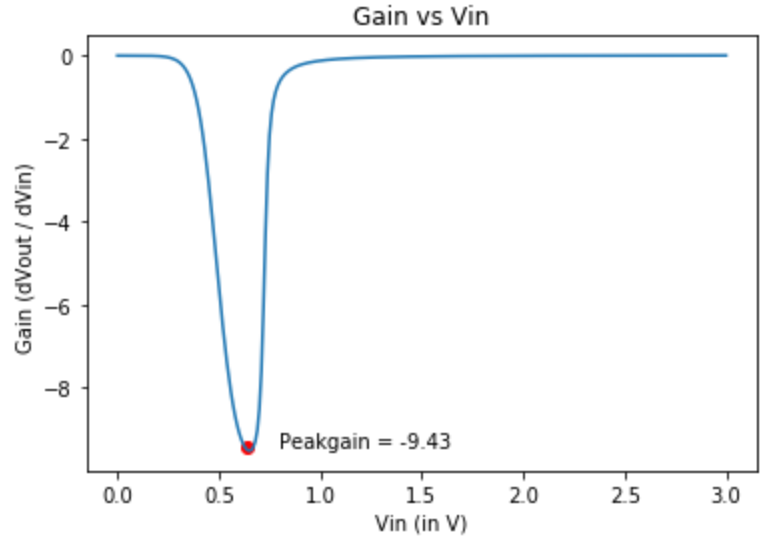
Ques 5 : NMOS

5a) VTC plots :

```
** Q5. VTC of NMOS  with res

.include TSMC180.lib
.model nch_tt nmos


M vout input 0 0 nch_tt W = 0.54u L = 0.18u
R vout vdd 75k
Vin input 0 dc
V Vdd 0 2.5V

.control
dc Vin 0 3 .01

plot V(vout) vs v(input)
plot deriv(V(vout))

let diff=deriv(V(vout))
let peakgain=deriv(diff)
meas dc vIL find V(input) when diff=-1 cross=1
meas dc vIH find V(input) when diff=-1 cross=2
meas dc vOH find V(vout) when V(input)=0 cross=1
meas dc vOL find V(vout) when V(input)=2.5 cross=1
meas dc vM find V(vout) when V(input)=V(vout) cross=1
meas dc gain_peak find diff when peakgain=0

wrdata 5.a.1.dat V(vout)  vs v(input)
wrdata 5.a.2.dat deriv(V(vout)) vs v(input)

.endc
.end
```

Plotting the gain (dVout/ dVin) and Vout vs Vin For R_L = 75k Ohms





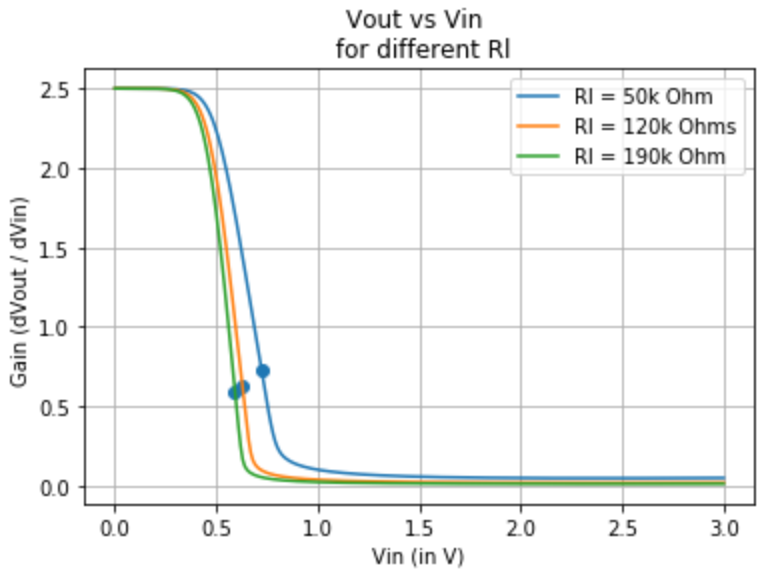
Parameters	Observed Value
V_{IL}	0.387 V
V_{IH}	0.774 V
V_{OH}	2.49 V

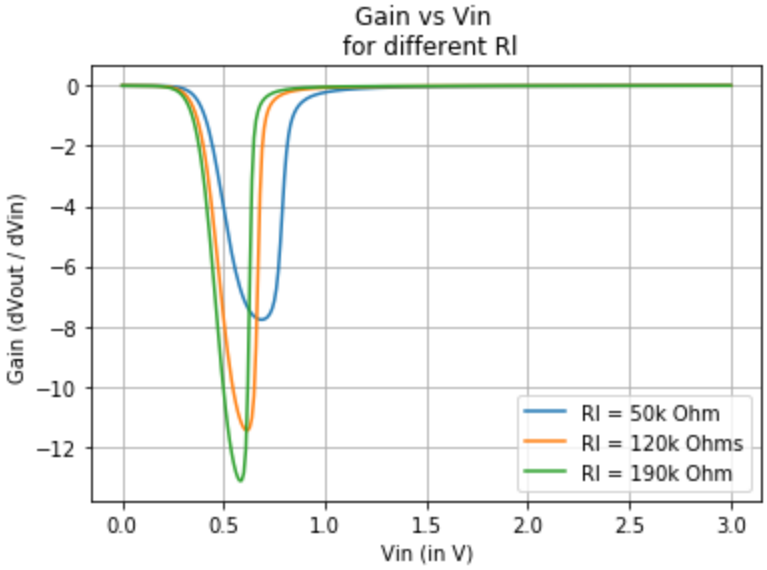
V_{OL}	0.031 V
V_M	0.67 V
Peak gain	-9.43

5b) Change of threshold and peak gain w.r.t load resistance.

Varying resistance : checking for : 50k, 120k , 190k.

```
.include TSMC180.lib
.model nch_tt nmos

M vout input 0 0 nch_tt W=0.54u L=0.18u
R vout vdd 75k
Vin input 0 dc
V vdd 0 2.5V
.control
dc Vin 0V 3V 0.01V R 50k 200k 70k

plot V(vout)
plot deriv(V(vout))
let diff=deriv(V(vout))
let peakgain=deriv(diff)
meas dc vil find V(input) when diff=-1 cross=1
meas dc vih find V(input) when diff=-1 cross=2
meas dc voh find V(vout) when V(input)=0 cross=1
meas dc vol find V(vout) when V(input)=2.5 cross=1
meas dc vm find V(vout) when V(input)=V(vout) cross=1
meas dc gain_peak find diff when peakgain=0

wrdata 5.b.1.dat V(vout)  vs v(input)
wrdata 5.b.2.dat deriv(V(vout)) vs v(input)
.endc
.end
```





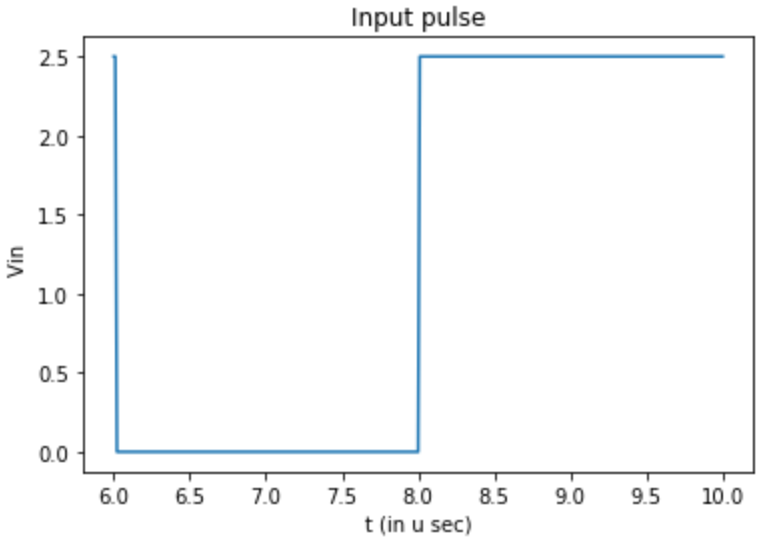
Observations :

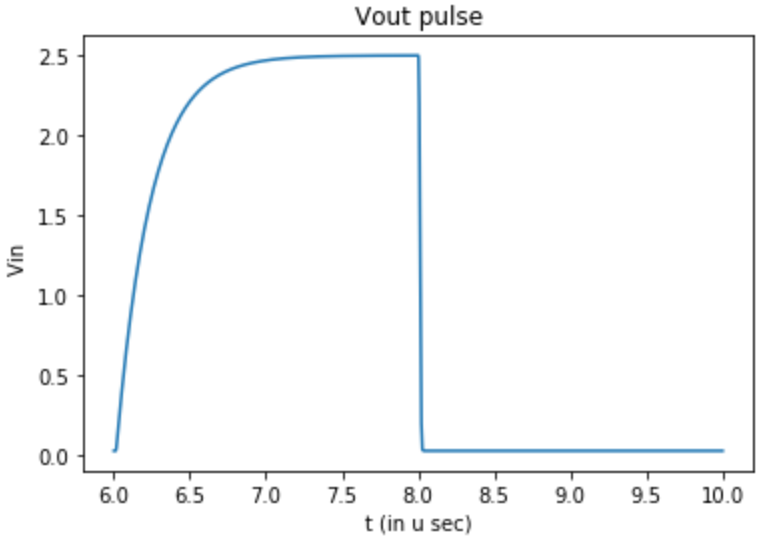
1. As R_L increases, V_M decreases, this is a consequence of the Pull down network becoming stronger.
2. Also the peak gain increases by magnitude. This happens due to the movement of V_M towards V_{IL} , hence the slope needs to drop at a high rate, this inturn increases the peak gain.

5c.) Implementing an inverter : Testing with a square pulse of f = 250k Hz, C_L = 3pF.

```
.include TSMC180.lib
.model nch_tt nmos

M vout input 0 0 nch_tt W = 0.54u L = 0.18u
R vout vdd 75k

** input Vmax 1V, 50 per duty cycle , freq : 25kHz
Vin input 0  PULSE(0 2.5 0 0 0 2u 4u)
V Vdd 0 2.5V
C vout 0 3p


.tran 0.01u 10u 6u
.control
run
plot V(input)
plot V(vout)

meas tran vout(max) MAX V(vout)
meas tran input(max) MAX V(input)

let v_half = vout(max)/2
let v_10 = 0.1*vout(max)
let v_90 = 0.9*vout(max)
let vin_half = 1.25
meas tran tr_10 when V(vout) = v_10 cross = 1
meas tran tr_90 when V(vout) = v_90 cross = 1

meas tran tf_90 when V(vout) = v_90 cross = 2
meas tran tf_10 when V(vout) = v_10 cross = 2
meas tran tr_half_1 when V(vout) = v_half cross = 1
meas tran tr_half_2 when V(vout) = v_half cross = 2


meas tran tin_half1 when V(input) = vin_half cross = 1
meas tran tin_half2 when V(input) = vin_half cross = 2

let tpl = tr_half_1  - tin_half1
let tph = tr_half_2 - tin_half2
let tp  =(tpl+tph)/2


let tr = tr_90 - tr_10
let tf = tf_10 - tf_90
```

```
print tr tf
print tpl tph
print tp

wrdata 5.c.1.dat V(input)
wrdata 5.c.2.dat V(vout)
.endc
.end
```





Parameters obtained from the simulation

Parameter	Value
t_r	494.04 ns
t_f	14.37 ns
t_{plh}	154.25 ns
t_{phl}	7.79 ns
t_p	81.07 ns

- **Comment on t_r and t_f ..**
  $T_r >> T_f$, reason being the RC circuit changes when during the transition. For rise time we consider R_L , while for the fall time we consider R_{ON} . Since $R_{ON} < R_L$ here. The capacitor charges and discharges at different rates.
- **Geometric parameters :** The max. Operating frequency for a particular MOSFET depends on t_p (propagation delay), i.e; how fast will it be responding for the switch. T_p inturn depends on the R_{eq} and thus depends on the (W/L) ratio.
- **Max. operating frequency :**
  $f_{max} = 1/ t_p = 1 /(81.07 \text{ ns}) = 12.33 \text{ MHz}$
- **Dynamic power dissipation :**

$$P_D = C_L * (V_{gs} - V_t) * V_{DD} * f_{max}$$

= 0.225 mW

THE END