3@)

$V_{TN} = |V_{TP}| = 0.3V$

$V_{DD} = 1.2V$

a) which one consumes static power? at high input?

→ (i), (ii), (iii).

CMOS (iv), has no current flow due to presence of a PMOS (at OFF state)

In other cases, since NMOS is ON current flows ⇒ static power consumed

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b) Static power at low input?

⇒ None

→ No current is drawn, since ~~PMOS~~ NMOS are off state in every case

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(c) $V_{OH} = 1.2V$?

(i) (ii) (iv)

⇒ (i) MOS is off ⇒ no current

⇒ $\boxed{V_{out} = 1.2V}$ ✓

⇒ (ii) NMOS at bottom requires no current ⇒ $V_{GS} - V_T = 0$ (of top NMOS)

⇒ $\boxed{V_{out} = 0.9V}$ ✗

⇒ (iii) No current a bottom

$V_{GS} = V_T = 0V$

⇒ $\boxed{V_S = V_{out} = 1.2V}$ ✓

→ (iv) NMOS is open ⇒

no current is allowed

⇒ $\boxed{V_{out} = 1.2V}$ ✓

(d) $V_{OL} = 0V$?

(i) (iv)

Reason: Since both

For i, ii, iii ⇒ current is drawn

⇒ Vout is found by voltage divider network. ⇒ Hence $V_{out} \neq 0$

For CMOS:

PMOS is open ⇒ $V_{out} = 0$

(e) (i) (ii) (iii)

All except CMOS are dependent on size of devices