Storage in CPU

* Stack architecture
* Accumulator architecture
* General Purpose Register architecture(GPR)

**C=A + B**

**Stack:**

push A

push B

add

pop C

**Accumulator:**

load A

add B

store C

**GPR:-**

load R1, A

add R1,B

store R1,C

GPR can be subdivide into 3 classifications:

Memory-memory arch

Register-memory arch

Load store arch

Instructions in GPR arch can be either fixed length or variable length

SPARC project

MIPS project

Load R1,A

Load R2, A

Load R2,B

Add R3,R1,R2

Store C,R3

Opcode only (zero address instruction)

Opcode +1 addr

Opcode +2 addr

Opcode +3 addr

Operations that are not commutative

3+7\*2

Prefix -operation followed by the operands

Infix- operand, operator, operand

Postfix – operands followed by the operations

Prefix is also called Polish notation

Postfix is also called reverse Polish notation(RPN)

2 (7-3)

2 7 3 -\* (RPN version)

Consider 16-bit instruction format with 4 bit opcode

* - - -| - - - - |- - - - | - - - -

Opcode addr1 addr2 addr3

* - - -|---------------------------

Opcode addr

0000 R1 R2 R3

. . .

1110 R1 R2 R3

1111 0000 R1 R2

. . .

1111 1101 R1 R2

1111 1110 0000 R1

. . .

1111 1111 1110 R1

1111 1111 1111 R1

. . .

1111 1111 1111 R1

If (leftmost 4 bits <= 1110)

Execute 3-adddr instruction

Else if(leftmost 8 bits<=1111 1101)

Execute 2-addr instruction

Else if(leftmost 12 bits<1111 1111 1110)

Execute 1-addr instruction

Else

Execute 0-addr instruction