Two Wired Interface (TWI) / Inter IC (I^2C)

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Microprocessor Laboratory EE 337

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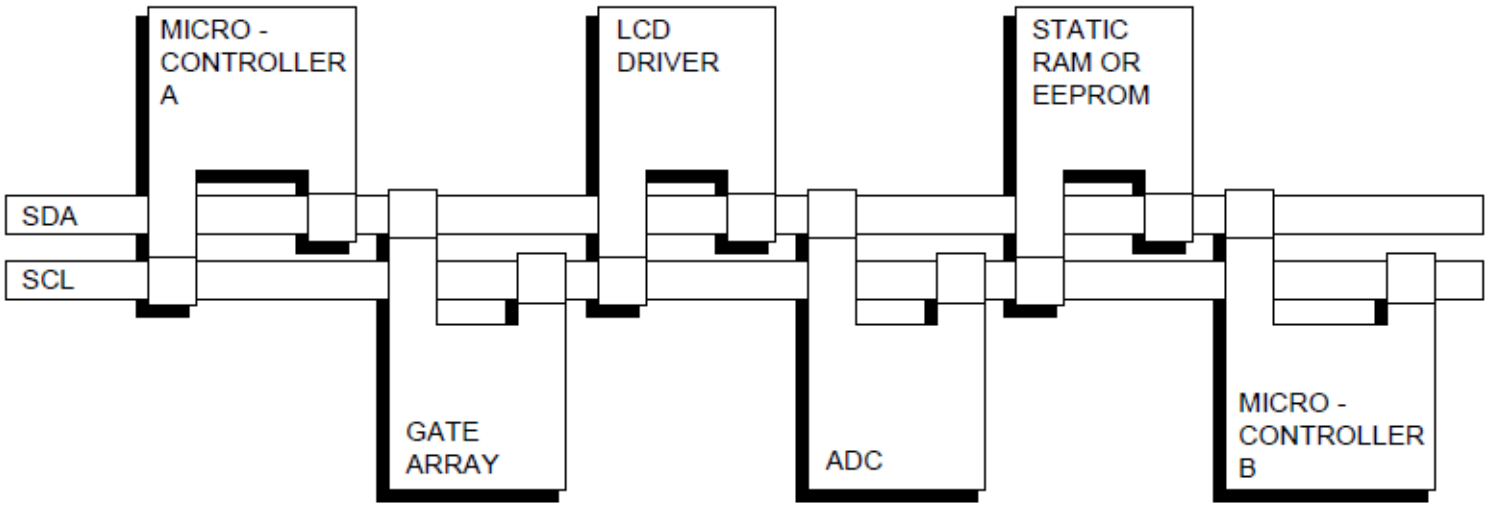
I^2C

I^2C is a two-wired, half-duplex serial mode of communication.

Here are some of the features of the I^2C-(Inter IC):

- Only **two** bus lines are required; a serial data line (SDA) and a serial clock line (SCL).
- **Master** alone determines the clock speed.
- It is **Multi-master** – **Multi-slave** type of communication.
- 8-bit oriented, **bidirectional** data transfers up to:
  - 100 kbps in Standard-mode.
  - 400 kbps in Fast-mode.
  - 1 Mbps in Fast-mode Plus.
  - 3.4 Mbps in High-speed mode.
- **Unidirectional** data transfers up to 5 Mbps in Ultra Fast-mode
- Clock synchronization using **clock stretching**.

I²C Network



7/10 bit addressing modes. The number of ICs that can be connected to the same bus is limited only by the maximum bus capacitance.

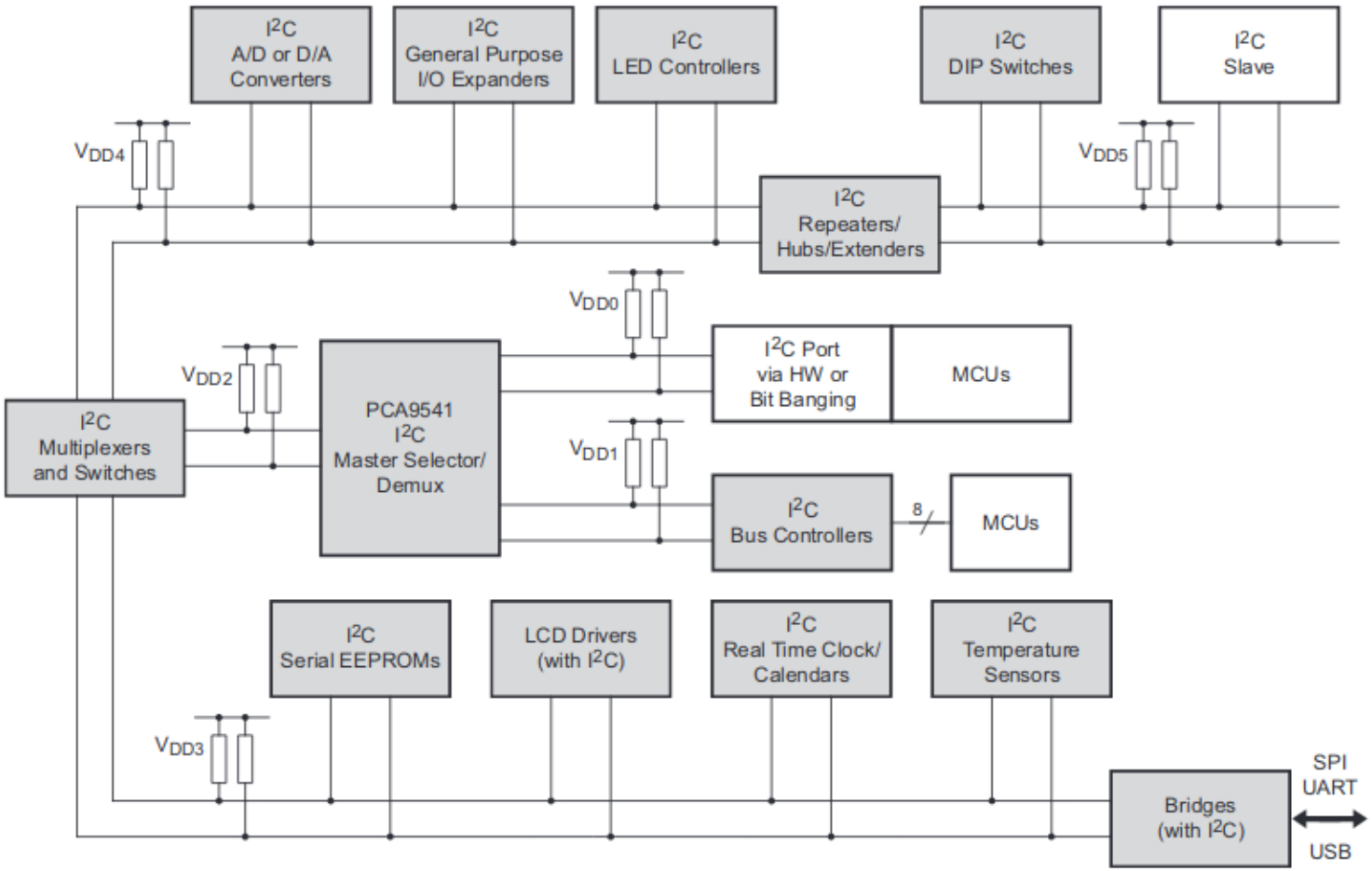
Comparison with UART and SPI

Speed: SPI > I^2C > UART

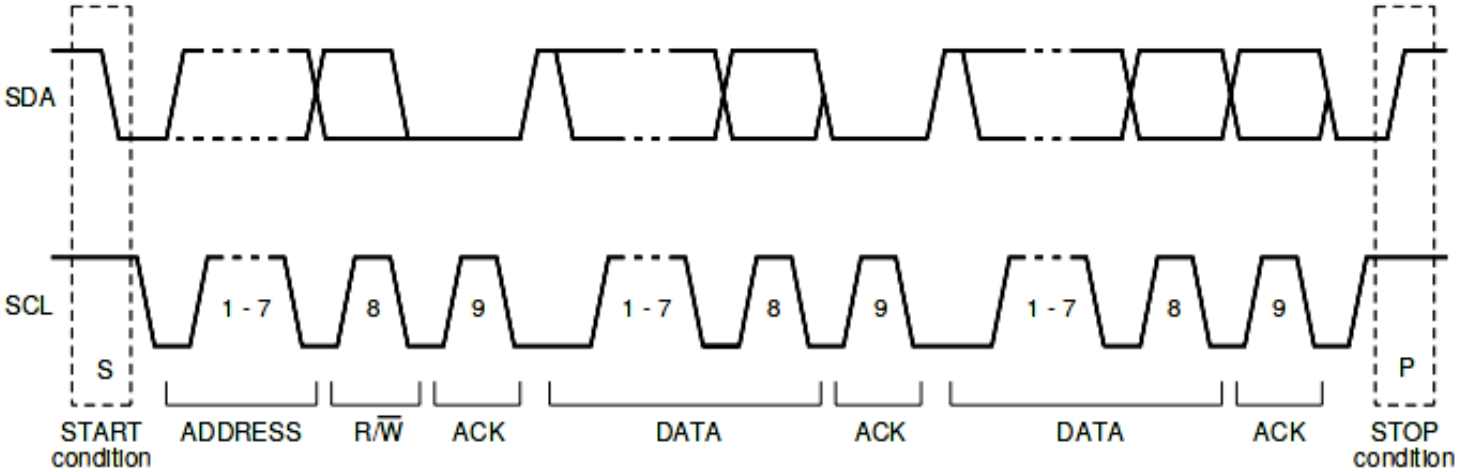
Doesn't require slave-select lines

Multiple Master and Multiple Slave all at once !

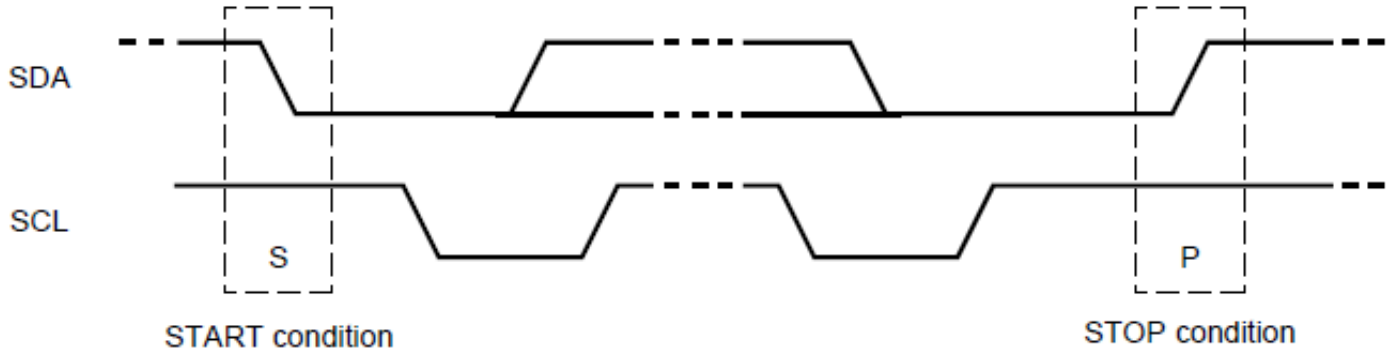
Applications



Data Transfer



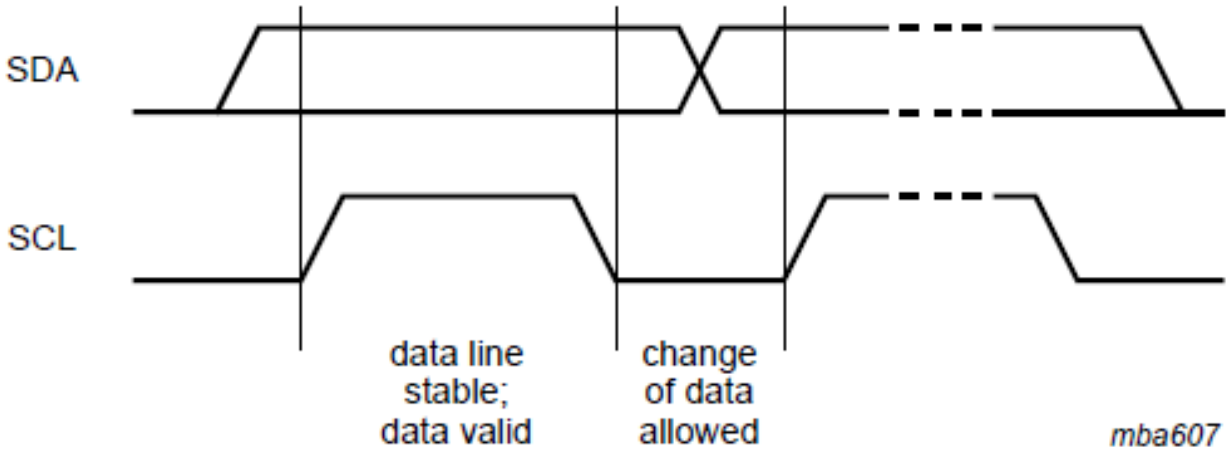
Start and Stop Condition



Transitions on SDA only when SCL is held High.

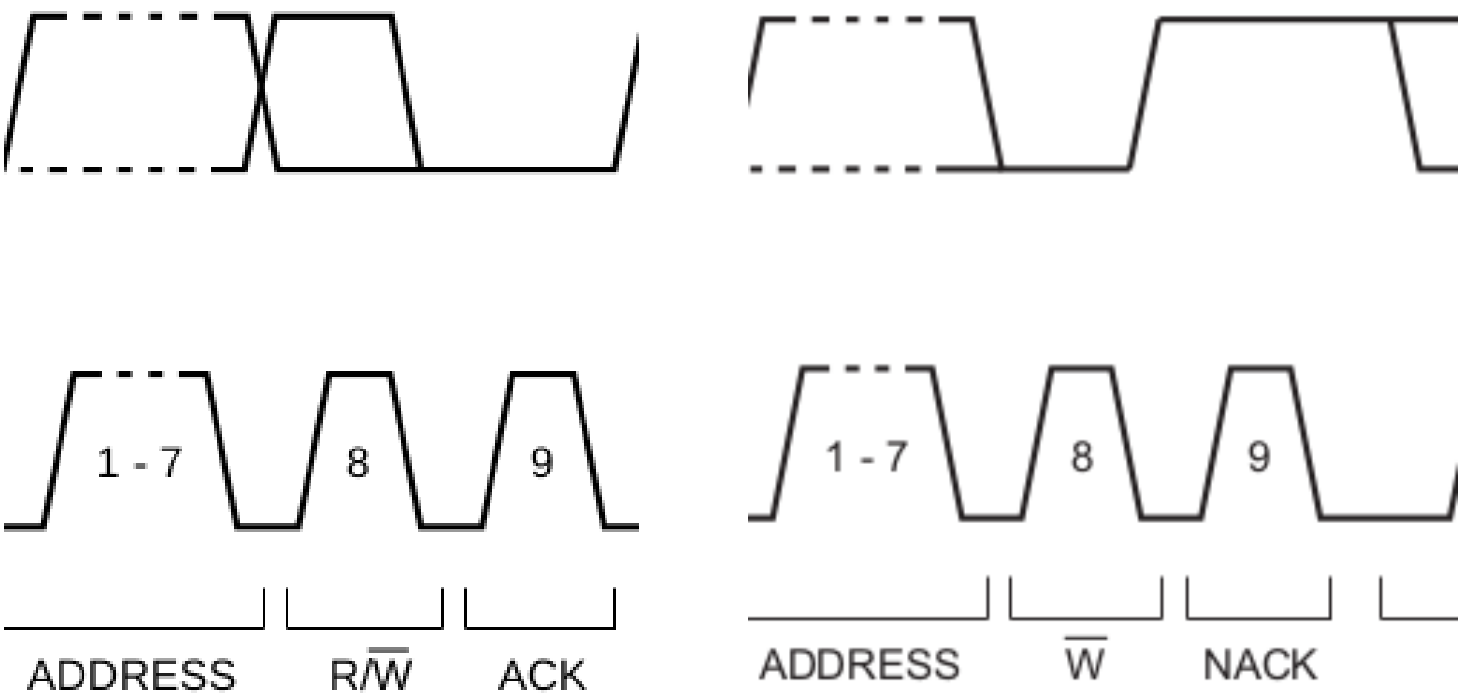
- High -> Low : Start bit
- Low -> High : Stop bit

Data Validity



Transitions on SDA only when SCL is held Low.

Acknowledge and Not Acknowledge



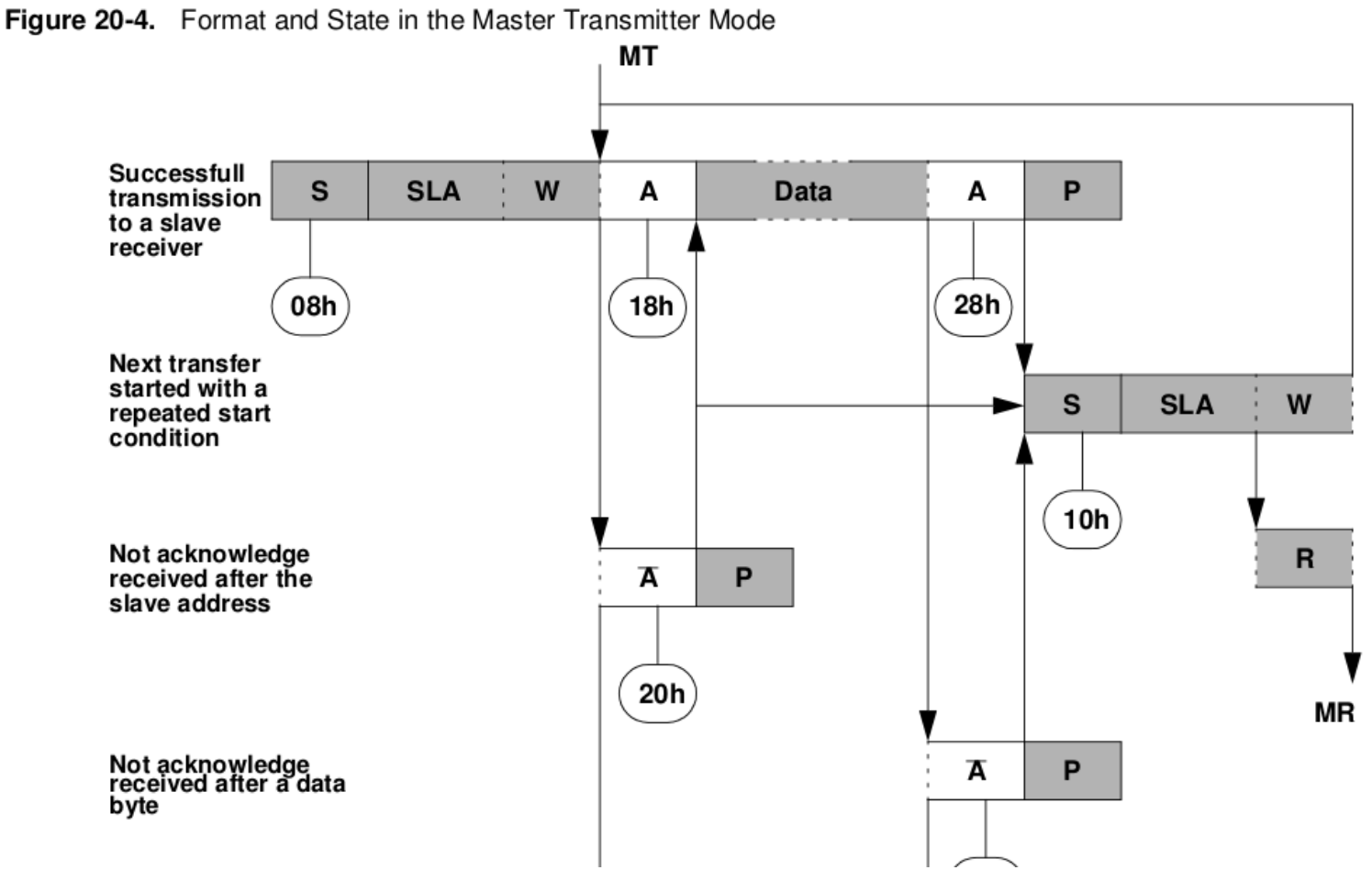
SDA line held Low and High respectively for ACK and NACK on the **9th** clock pulse on SCL line.

AT89C5131A I^2C Interfacing

Refer Page 102 of AT895131A Datasheet.

- Configure SDA and SCL pins as inputs.
- Initialize the following AT89c5131A Registers:
  - SSCON - to enable the TWI interface, to program the bit rate, to enable slave modes, to acknowledge or not a received data, to send a START or a STOP condition on the 2-wire bus, and to acknowledge a serial interrupt.
  - Interrupt SFR's - To enable and decide priority of external interrupt from OPT and TWI interrupt
  - TCON - To decide nature of interrupt to be served
- Read SSCS register to figure-out what type of TWI interrupt occurred(refer SSCS register map)
- SSDAT contains the Data to be transmitted/Received

SSCS Register



SSCS Register

Table 20-5. Status in Master Transmitter Mode

SSCS Status Code SSSTA	Status of the Two-wire Bus and Two-wire Hardware	Application software response					Next Action Taken by Two-wire Hardware
		To/From SSDAT	To SSCON				
			SSSTA	SSSTO	SSI	SSAA	
08h	A START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
10h	A repeated START condition has been transmitted	Write SLA+W	X	0	0	X	SLA+W will be transmitted.
		Write SLA+R	X	0	0	X	SLA+R will be transmitted. Logic will switch to master receiver mode
18h	SLA+W has been transmitted; ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.
		No SSDAT action	1	1	0	X	STOP condition followed by a START condition will be transmitted and SSSTO flag will be reset.
20h	SLA+W has been transmitted; NOT ACK has been received	Write data byte	0	0	0	X	Data byte will be transmitted.
		No SSDAT action	1	0	0	X	Repeated START will be transmitted.
		No SSDAT action	0	1	0	X	STOP condition will be transmitted and SSSTO flag will be reset.

Question/Comments

For any queries regarding I^2C feel free to contact us.

THANK YOU !