Design Compiler® User Guide

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SYNOPSYS®

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About This Manual

The Synopsys Design Compiler® tool provides basic synthesis information for users of the Design Compiler tools. This manual describes synthesis concepts and commands, and presents examples for basic synthesis strategies.

This manual does not cover asynchronous design, I/O pad synthesis, test synthesis, simulation, or back-annotation of physical design information.

The information presented here supplements the Synopsys synthesis reference manuals but does not replace them. See other Synopsys documentation for details about topics not covered in this manual.

This manual supports the Synopsys synthesis tools, whether they are running under the UNIX operating system or the Linux operating system. The main text of this manual describes UNIX operation.

This manual is intended for logic designers and engineers who use the Synopsys synthesis tools with the VHDL or Verilog hardware description language (HDL). Before using this manual, you should be familiar with the following topics:

- High-level design techniques
- ASIC design principles
- Timing analysis principles
- Functional partitioning techniques

This preface includes the following topics:

New in This Release

Information about new features, enhancements, and changes, known limitations, and resolved Synopsys Technical Action Requests (STARs) is available in the Design Compiler Release Notes on the SolvNetPlus site.

Feedback

Related Products, Publications, and Trademarks

For additional information about the Design Compiler tool, see the documentation on the Synopsys SolvNetPlus support site at the following address:

https://solvnetplus.synopsys.com

You might also want to see the documentation for the following related Synopsys products:

- Design Vision™
- DesignWare® components
- TestMAX™ DFT and DFTMAX™
- DC Explorer
- HDL Compiler™
- IC Compiler™
- IC Compiler™ II
- Power Compiler™
- PrimeTime®

Conventions

The following conventions are used in Synopsys documentation.

Convention	Description
`Courier`	Indicates syntax, such as `write_file`
`Courier italic`	Indicates a user-defined value in syntax, such as `write_file` *`design_list`*
`Courier bold`	Indicates user input—text you type verbatim—in examples, such as `prompt>` **`write_file top`**
`Purple`	• Within an example, indicates information of special interest. • Within a command-syntax section, indicates a default, such as `include_enclosing = true | false`
[ ]	Denotes optional arguments in syntax, such as `write_file [-format` *`fmt`*`]`

Feedback

Convention	Description
...	Indicates that arguments can be repeated as many times as needed, such as *pin1 pin2 ... pinN*.
|	Indicates a choice among alternatives, such as `low | medium | high`
\	Indicates a continuation of a command line.
/	Indicates levels of directory structure.
Bold	Indicates a graphical user interface (GUI) element that has an action associated with it.
Edit > Copy	Indicates a path to a menu command, such as opening the **Edit** menu and choosing **Copy**.
Ctrl+C	Indicates a keyboard combination, such as holding down the Ctrl key and pressing C.

Customer Support

Customer support is available through SolvNetPlus.

Accessing SolvNetPlus

The SolvNetPlus site includes a knowledge base of technical articles and answers to frequently asked questions about Synopsys tools. The SolvNetPlus site also gives you access to a wide range of Synopsys online services including software downloads, documentation, and technical support.

To access the SolvNetPlus site, go to the following address:

https://solvnetplus.synopsys.com

If prompted, enter your user name and password. If you do not have a Synopsys user name and password, follow the instructions to sign up for an account.

If you need help using the SolvNetPlus site, click REGISTRATION HELP in the top-right menu bar.

Contacting Customer Support

To contact Customer Support, go to https://solvnetplus.synopsys.com.

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Design Compiler Introduction

The Design Compiler product is the core of the Synopsys synthesis products. Design Compiler optimizes designs to provide the smallest and fastest logical representation of a given function. It comprises tools that synthesize your HDL descriptions into optimized, technology-dependent, gate-level designs. It supports a wide range of flat and hierarchical design styles and can optimize both combinational and sequential designs for speed, area, and power.

For an introduction to logic- and gate-level designs, the Design Compiler product, the design flow, and the Design Compiler family of products, see

- About Design Compiler
- The Design Compiler Family
- Design Compiler in the Design Flow
- High-Level Design Flow Tasks
- Design Terminology
- Selecting and Using a Compile Strategy
- Optimization Basics

About Design Compiler

The Design Compiler product consists of the following:

- Design Compiler NXT
- Design Compiler Graphical
- DC Ultra
- DC Expert

Feedback

Design Compiler NXT

Design Compiler NXT provides all the Design Compiler Graphical, DC Ultra, and DC Expert features plus additional features. Design Compiler NXT provides

- Better QoR through advanced optimizations
- Enhanced physical guidance to IC Compiler II, with improved RC and timing correlation
- Faster runtime, with improved multithreading synthesis for better scalability
- Plug-and-play user interface and script compatibility with Design Compiler Graphical

The following Design Compiler NXT features are provided in addition to the Design Compiler Graphical, DC Ultra, and DC Expert features:

- Buffering-aware placement
- Automatic timing control
- Congestion-driven restructuring
- Better QoR with high performance cores

Running Design Compiler NXT requires a Design-Compiler-NXT license.

To invoke Design Compiler NXT, run the `dcnxt_shell` command with the `-topographical_mode` option in the UNIX or Linux shell. For information about using topographical mode, see Design Compiler Modes. To perform synthesis, use the `compile_ultra` command with the `-spg` option.

See Also

- Using Design Compiler NXT

Design Compiler Graphical

Design Compiler Graphical provides all the DC Ultra and DC Expert features plus additional features. Design Compiler Graphical

- Optimizes multicorner-multimode designs
- Reduces routing congestion
- Improves correlation with IC Compiler and IC Compiler II
- Improves runtime in IC Compiler and IC Compiler II by using Synopsys physical guidance
- Allows you to create and modify floorplans

Feedback

In addition, Design Compiler Graphical lets you create and modify floorplans using floorplan exploration.

The following Design Compiler Graphical features are provided in addition to the DC Expert and DC Ultra features:

- Optimization for multicorner-multimode designs
- Reduction of routing congestion during synthesis
- Improved area and timing correlation with IC Compiler
- Improved runtime and routability in IC Compiler
- Ability to create and modify floorplans using floorplan exploration
- Physical guidance technology, which includes enhanced placement and the capability to pass seed placement to IC Compiler to improve quality of results (QoR), correlation, and routability

Running Design Compiler Graphical requires a DC Ultra license and a Design Compiler Graphical license.

To invoke Design Compiler Graphical, run the `dc_shell` command with the `-topographical_mode` option in the UNIX or Linux shell. For information about using topographical mode, see Design Compiler Modes. To perform synthesis, use the `compile_ultra` command with the `-spg` option.

See Also

- Using Design Compiler Graphical

DC Ultra

At the core of the Synopsys RTL synthesis solution is DC Ultra. DC Ultra provides all the DC Expert features plus additional features. It provides concurrent optimization of timing, area, power, and test for today's high performance designs. DC Ultra provides advanced delay and arithmetic optimization, automatic leakage power optimization, advanced timing analysis, register retiming, and more. By default, DC Ultra runs in wire load mode, which uses wire load models for delay estimation.

In addition, DC Ultra provides topographical technology, which allows you to accurately predict post-layout timing, area, and power during RTL synthesis without the need for timing approximations based on wire load models. This ensures better correlation with the final physical design. Topographical technology generates a better starting point for place and route, eliminating costly iterations.