BUCK CONVERTER DESIGN #1

$$D = \frac{V_{out}}{V_{in}} \qquad L = \frac{(V_{IN} - V_{OUT}) \cdot D}{f_S \cdot \Delta I_L} \qquad I_{L(\text{peak})} = I_{OUT(\max)} + \frac{\Delta I_L}{2}$$

$$C_{OUT} = \frac{\Delta I_L}{8 \cdot f_S \cdot \Delta V_{OUT}}$$

Parameter	Value
Input Voltage (Vin)	12 V
Output Voltage (Vout)	5 V
Maximum Output Current (Iomax)	1 A
Switching Frequency (Fs)	500 kHz
Output Voltage Ripple (ΔVout)	50 mV
Inductor Current Ripple (ΔIL)	30% of Iomax ~ 0.3 A

Parameter	Calculations	Value
T	1/0.5M	2 us
D	5 / 12	0.417
Ton	0.417 * 2u	0.834 us
L	(12-5) * 0.417 / (0.5Meg*0.3)	19.44 uH
IL(peak)	1 + 0.3 / 2	1.15 A
Cout	0.3 / (8*0.5Meg*50m)	1.5 uF
RL	Vout/ Iomax = 5 / 1	5 A

INDUCTOR SELECTION

Criterion	Value / Range
Value	Closest to calculated value ~20 uH
Peak current	20-30% more than IL(peak) => 1.3 * 1.15, >1.5A
Series Resistance	Low as possible to reduce conduction loss.
Material / Frequency	High-frequency power inductor is essential to minimize core loss.

CAPACITOR SELECTION

Criterion	Value / Range
Equivalent resistance (Rser)	ΔVout = ΔIL * Rser => Rser < ΔVout / ΔIL = 50m/0.3 , <167mΩ.
Temperature / Voltage Stability	Ceramic capacitors lose capacitance when a DC bias voltage is applied and when the temperature changes. **X7R** is the **standard recommendation** for decoupling and filtering in power supplies.
Voltage rating	>2*Vout = >2*5 = >10 V
Equivalent series inductance	ESL causes high-frequency ringing and is minimized by using small case sizes (e.g., 0805 or 0603) and good PCB layout.

DIODE SELECTION

Parameter	Formula / Typical Range	Value
Type		Schottky Diode
Breakdown Voltage (Vbkdn)	1.2 × Vin(max)	14.4 V
Average Current (Iave)	1.2 × (1 - D) × Iout	0.7 A
Saturation current (Is)	10^{-9} to 10^{-6} A	High
Emission Coefficient (N)	1.0 to 1.7	Low close to 1
Series Resistance (Rs)	10 mΩ to 100 mΩ	Low

Zero-Bias Junction Capacitance (CJO)	10 pF to 100 pF	Low (otherwise it leads to ringing)

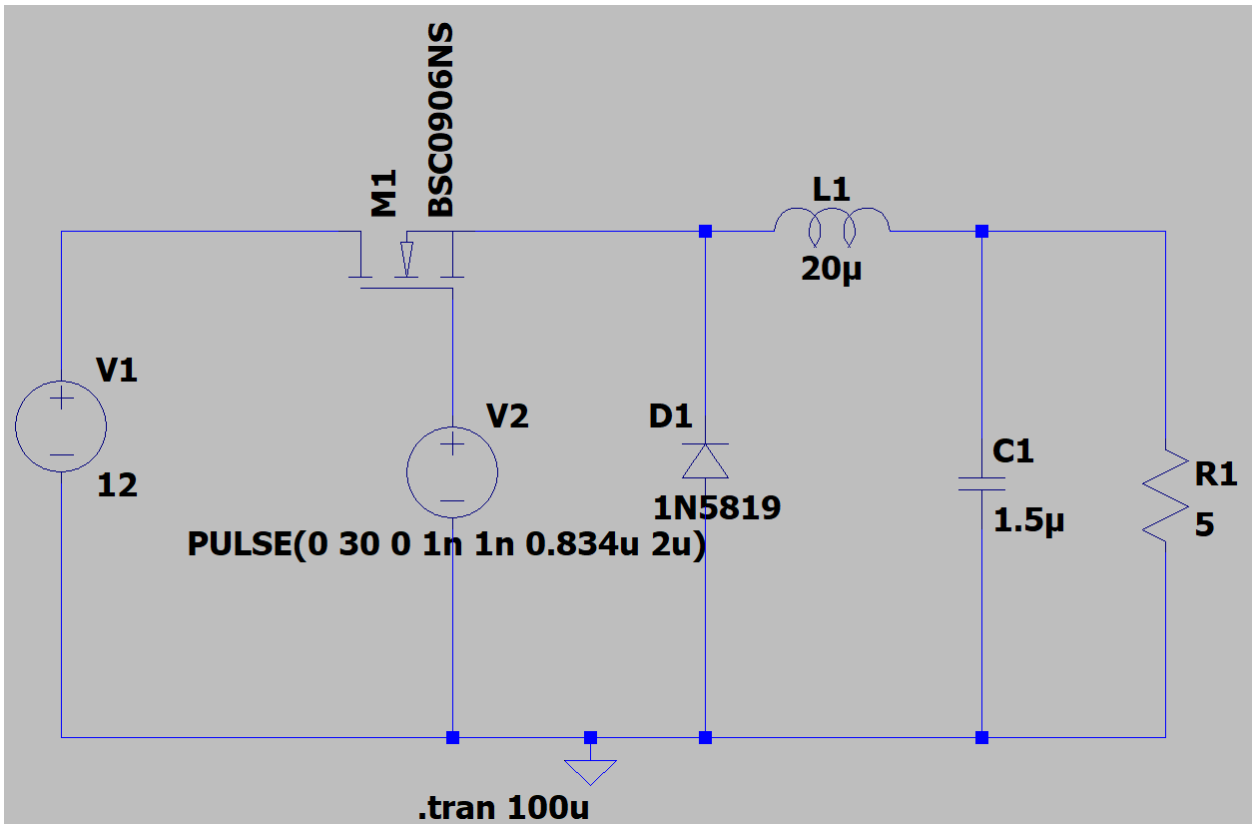
General Schottky Barrier Diodes (SBDs) used:

Series / Part Example	**Package Types**	**Key Feature / Application**
1N58xx	DO-41 (Axial), SMA/SMB (SMD)	Industry Standard, Low Cost. Excellent choice for low-power bucks
MBR/MBRS Series	DO-201, SMA/SMB/SMC (SMD)	Very Common SMD parts (e.g., MBRS140, MBRS360).
PDS/SD Series	TO-220, PowerDI, DPAK	Used for **medium-power** buck converters and general rectification.
SS/B58xx Series	SMC/SMB/SMA (SMD)	High-volume equivalents to MBR parts, often with slightly improved performance.

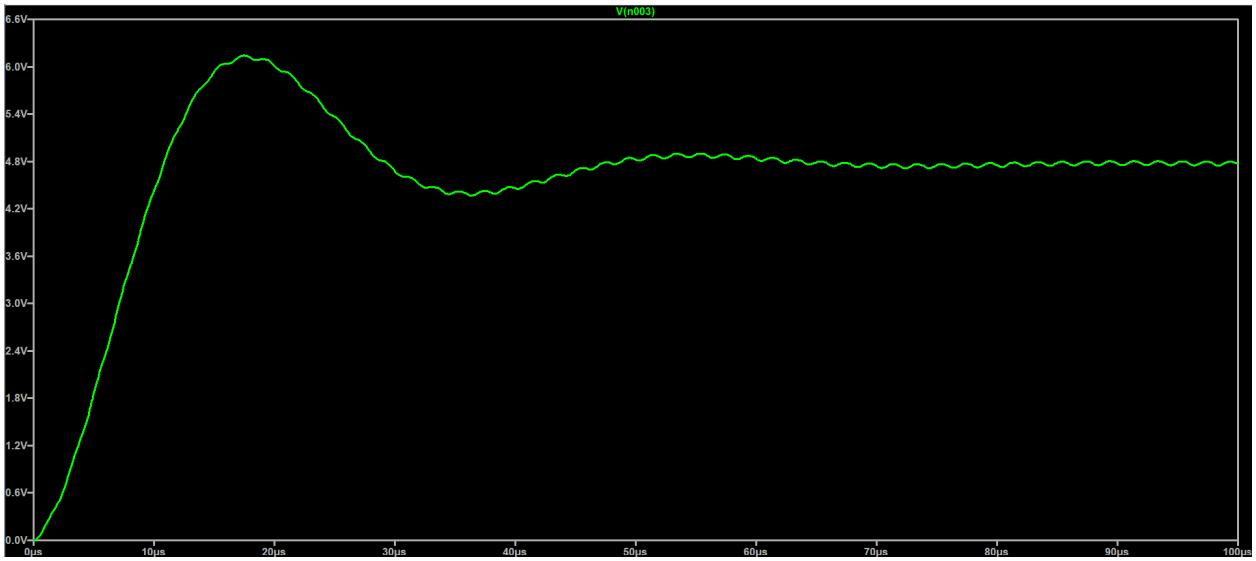
MOSFET SELECTION

Parameter	**Value**	**Reason**
Drain source voltage (Vds)	Vds > 1.2 * Vin(max) = 14.4 V	The MOSFET must block the full input voltage.
Max Current (Id)	Id > 1.5 * IL(peak) ~ 1.7 A	The MOSFET handles the full inductor current.
Gate-Source Voltage (Vgs)	Vgs (<2V)	
Type	N-channel	N-channel FETs have lower resistance and are standard for the low-side switch
On resistance Rds(on)	Lowest possible (< 50 mΩ)	Dominant factor for efficiency.
Gate source capacitance (Cgs)	Low	
Gate drain miller capacitance (Cgd)	Low	

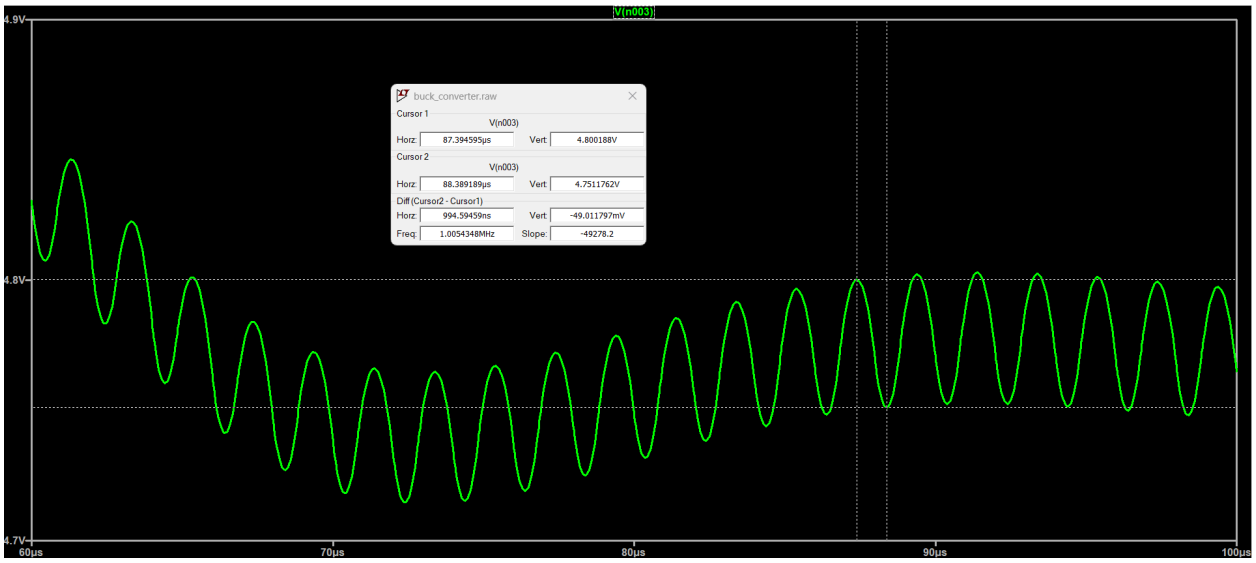
SIMULATION CIRCUIT



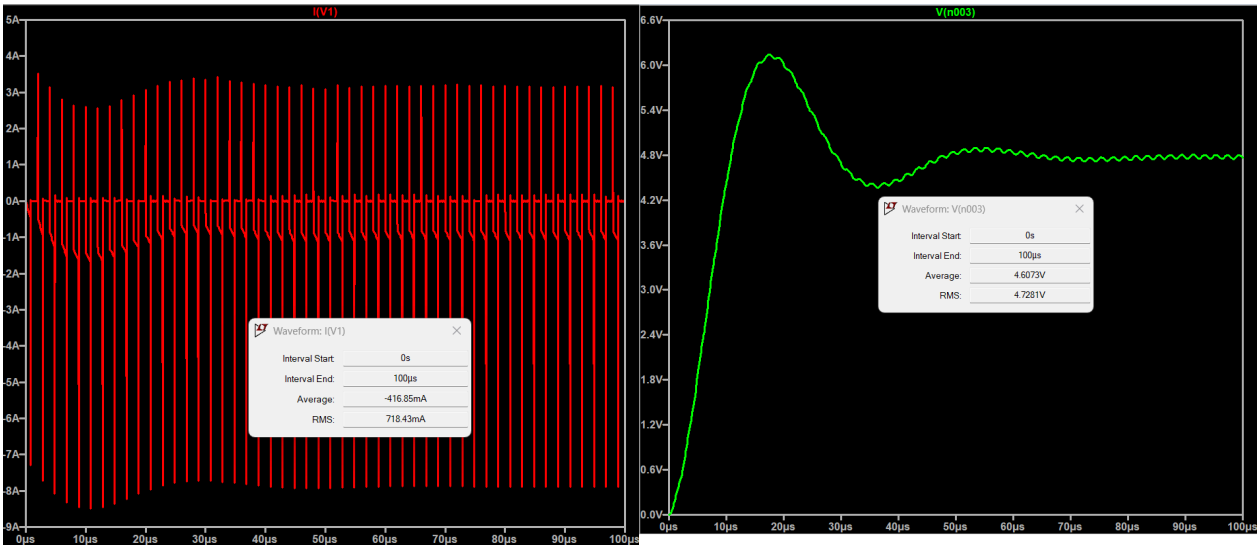
PLOTS



RIPPLE VOLTAGE

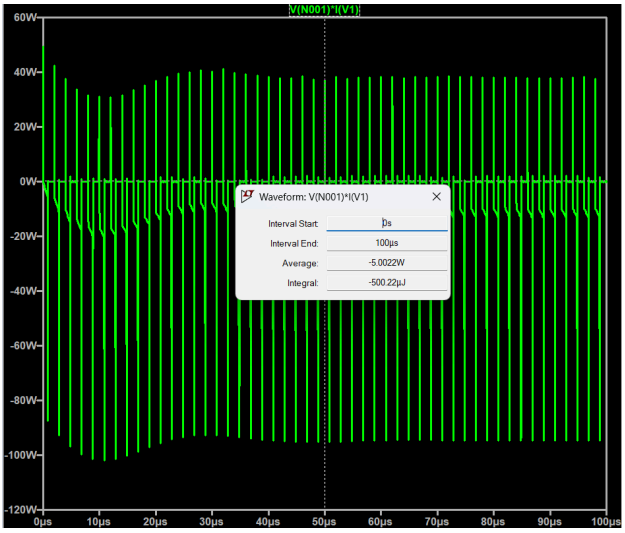


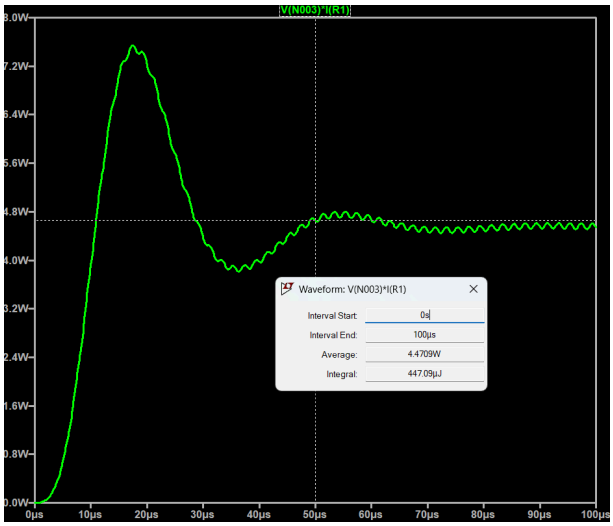
EFFICIENCY CALCULATION



Quantity	Calculation	Value
Iin(avg)	Observed (-ve sign due to LTSPICE convention for current leaving positive terminal	-416.85 mA
Pin(avg)	Vin(avg)*Iin(avg) = 12 * 416.85m	5.0022 W
Vout(avg)	Observed	4.6073V
Pout(avg)	Vout(avg)^2/RL = 4.6073**2 / 5	4.245 W
Efficiency	Pout(avg) / Pin(avg) * 100 = 4.245 / 5.0022 * 100	**84.87%**

ANALYZING COMPONENT LOSSES





Similarly, average power losses are computed for other components.

Quantity	**Calculation**	**Value**
Pin(avg)	Observed	5.0022 W
Pout(avg)	Observed	4.4709 W
P(mosfet)	Observed	324.6 mW
P(diode)	Observed	243 mW
P(inductor)	Observed	94.82 mW
P(capacitor)	Observed	171.21 mW
P(gate driver source)	Observed	-298.48mW (supplying power)
Pout (calculated)	Pin - P(Mosfet) - P(Diode) - P(inductor) - P(gate)	4.0413 W
Simulation Gap	Pout(waveform) - Pout(calculated)	0.4296 W

Rule: When calculating steady-state efficiency, you should **exclude the capacitor's average power** (or model its loss through ESR} only, which is typically tiny).

Since the P(gate driver source) is so high we vary V(pulse) and obtain following results

V(pulse)	P(pulse)	V(out)	Efficiency
10	-7.9918m	2.8796	33.17
15	-23.106m	4.5834	84.03
20	-301.82m	4.6073	84.91

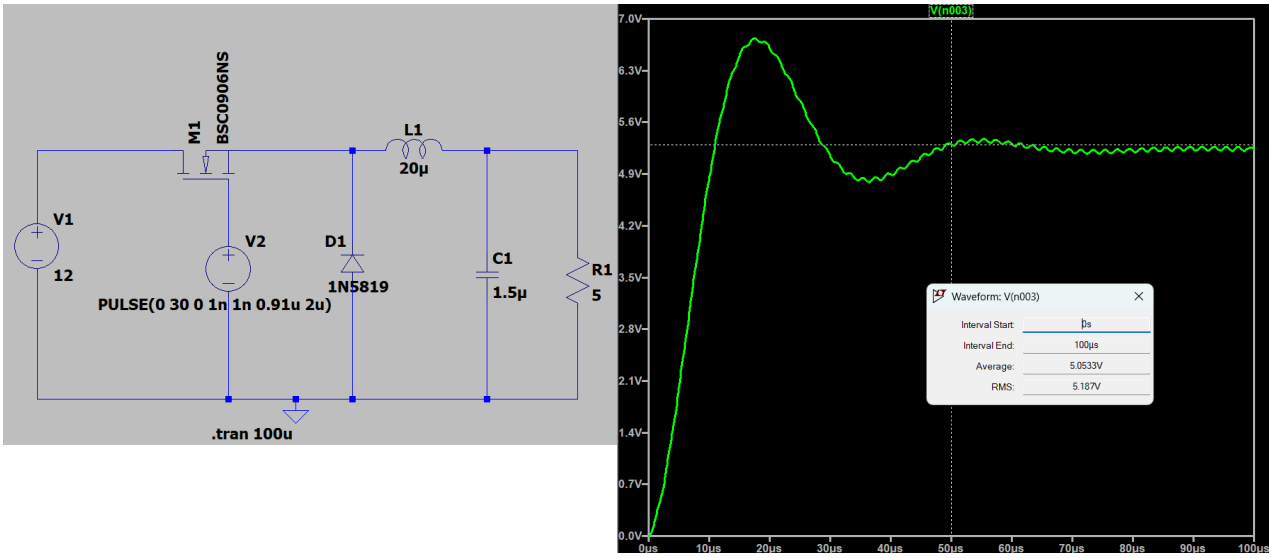
So V(pulse) of 15 V is selected.

FINAL MODIFICATIONS TO DUTY CYCLE TO HIT TARGET VOLTAGE

$$D_{new} = D_{current} \times \frac{V_{out,\,target}}{V_{out,\,current}}$$

Quantity	**Calculation**	**Value**
D(new)	0.417 * 5 / 4.5834	0.4549
Ton	D * T = 0.459 * 2u	9.1 us

FINAL RESULTS



Result: Vout (average) = 5.0533V.