

COMMON Emitter AMPLIFIER

VOLTAGE DIVIDER CIRCUIT

LOAD POINT CALCULATIONS

Given:

Quantity	Description	Value
Vcc	Dc Supply voltage	15V
Ic	Capacitor current at Q-point	3mA
B \ Hfe	Current Gain	200 (2N2222)
Vbe	Bias-Emitter Voltage	0.7V

Practical Assumptions:

Quantity	Formula	Substitutions	Value
Vre	10% of Vcc	0.1 * 15	1.5V
Vrc	40% of Vcc	0.4 * 15	6V
Vceq	50% of Vcc	0.5 * 15	7.5V
Vce	Vcc - Vrc	15 - 6	9V

Terminal Resistances:

Quantity	Formula	Substitutions	Value
Ie	$\sim I_c$		3mA
Re	$V_{re} / I_e \sim V_{re} / I_c$	$1.5 / 3m$	$0.5k\Omega$
Rc	V_{rc} / I_c	$6 / 3m$	$2k\Omega$

Base Terminal & Divider calculations:

Quantity	Formula	Substitutions	Value
Vb	$V_{re} + V_{be}$	$1.5 + 0.7$	2.2V
Ib	I_c / B	$3m / 200$	15uA

Idiv	$10 * I_b$	$10 * 15\mu$	150 μ A
Rb1	$(V_{cc} - V_b) / Idiv$	$(15 - 2.2) / 150\mu$	85.33k Ω
Rb2	$V_b / Idiv$	$2.2 / 150\mu$	14.67k Ω

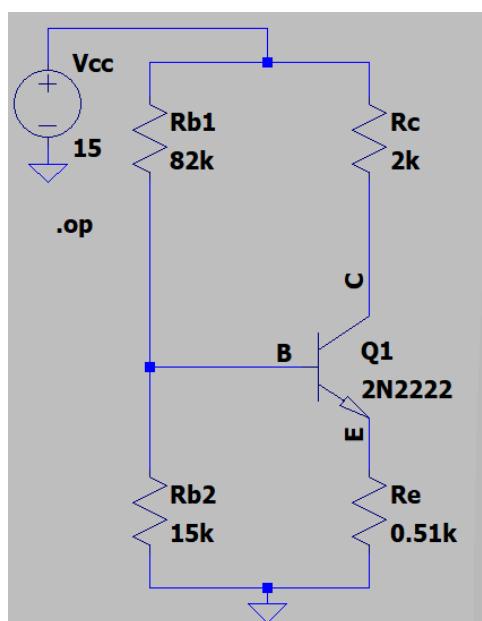
Swapping calculated resistor values to closest E24 series resistors (offers 5% tolerance)

Quantity	Original	Closes Standard value	Change (%)
R _e	500	510	2
R _c	2k	2k	0
R _{b1}	85.33k	82k	3.9
R _{b2}	14.67k	15k	2.25

Expected Q point shift:

Quantity	Formula	Substitutions	Value
R _b	R _{b1} + R _{b2}	82k + 15k	97k Ω
V _b	V _{cc} * [R _{b2} / (R _{b1} + R _{b2})]	15 * [15k / (82k + 15k)]	2.32V
I _e ~ I _c	(V _b - V _{be}) / R _e	(2.32 - 0.7) / 510	3.18mA

Results:



--- Operating Point ---

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V(b) : 2.14862 voltage
V(c) : 9.27352 voltage
V(e) : 1.46713 voltage
V(n001) : 15 voltage
I(Rb1) : 0.000156724 device_current
I(Rb2) : 0.000143241 device_current
I(Rc) : 0.00286324 device_current
I(Re) : 0.00287672 device_current
I(Vcc) : -0.00301996 device_current
Ib(Q1) : 1.34832e-05 device_current
Ic(Q1) : 0.00286324 device_current
Ie(Q1) : -0.00287672 device_current
Is(Q1) : 0 device_current

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Based on assumptions made above, an error of 10-15% is permissible.

Quantity	Calculated	Simulated	Absolute Difference	Error %
Vb	2.32	2.14862	0.17138	7.39
Vc	9	9.27352	0.27352	3.04
Ve	1.5	1.46713	0.03287	2.19
Vce	7.5	9.57937-1.36151=7.806 39	0.30639	4.01

AC PARAMETERS CALCULATIONS

Quantity	Description	Calculations	Value
Dynamic emitter resistance (re')	Thermal Voltage / Collector current	$Vt / Ic = 25mV / 3.18mA$	7.86Ω
AC base resistance [Rin (base)]	Resistance of the emitter circuit "reflected" to the base by the current gain.	$B * re' = 200 * 7.86$	$1.572k\Omega$
Input Impedance	The parallel combination of the two base-biasing resistors ($Rb1$ & $Rb2$) and the AC resistance looking into the base Rin (base).	$Rb1 \parallel Rb2 \parallel Rin$ (base) = $82k \parallel 15k \parallel 1.572k$	$1.398k\Omega$
Output Impedance	$\sim R_c$		$2k\Omega$
Ideal Voltage Gain (Av) [emitter resistor bypassed]	Gain produced in output voltage	$-R_c / re' = -2k / 7.86$	-254.45
Coupling Capacitors	High-pass filters, setting the low-frequency cutoff (f_L)	$C = 1/(2\pi f_L R)$	$f_L = 20Hz$
Input resistance (Rin)		R_s (source series resistance) + $Z_{in} = 50 + 1.398$	$1.448k\Omega$

Input coupling Capacitor (Cin)		$1/(2\pi R_{in} f_c) = 1/(2\pi \cdot 1.448 \cdot 20)$	22uF
Output coupling Capacitor (Cout)		$1/(2\pi (R_L + Z_{out}) f_c) = 1/(2\pi \cdot (1k + 2k) \cdot 20)$	10.6uF ~ 10uF or 15uF
Emitter Bypass Capacitor (Ce)	Ce is also a high-pass filter that determines a low-frequency cutoff (f _c e). It must be large enough so that its reactance is much smaller than R _e at the lowest operating frequency (f _L).	$R_{seen} \approx r_e' + (R_{b1} + R_{b2}) / \beta = 7.86 + 12.86k / 200 = 71.26\Omega$ $C_e = 1 / (2\pi f_c R_{seen}) = 1/(2\pi \times 5 \times 71.26)$	446uF ~ 470uF

Expected Results:

Quantity	Description	Calculations	Value
AC Collector Resistance (rc)		$R_c \parallel R_L = 2k \parallel 1k$	0.667kΩ
Actual Loaded Gain [Av (loaded)] (without Ce)	Emitter resistor unbypassed	$-rc / (r_e' + R_e) = -667 / (7.86 + 510)$	-1.288
Actual Loaded Gain [Av (loaded)] (with Ce)	Emitter resistor bypassed	$-rc / r_e' = 667 / 7.86$	-84.86
Maximum Output Swing (ΔV_{out}):	Minimum of distance from cutoff and saturation region	Saturation: $V_{ce} - V_{ce(sat)} = 7.5 - 0.2 = 7.3V$ Cutoff: $V_{cc} - V_{ce} = 15 - 7.5 = 7.5V$	7.3V (peak)
Maximum Input Voltage [Vin (peak)]		$\Delta V_{out} / Av(\text{loaded}) = 7.3 / 84.86$	86mV

NOTE: With given parameters the Vin (peak) which can be amplified without distortion is ~5mV. This is due to the non-linear characteristic of the BJT's base-emitter junction (the r_{e'} resistance) which becomes very pronounced when the emitter is bypassed.

A general rule of thumb for BJT amplifiers to remain in the linear small-signal region is that the AC emitter current i_e must be small enough that the AC voltage across r_e' is much less than the thermal voltage, V_t :

$$V_e = i_e \cdot r_e' \ll V_t \text{ (25mV)}$$

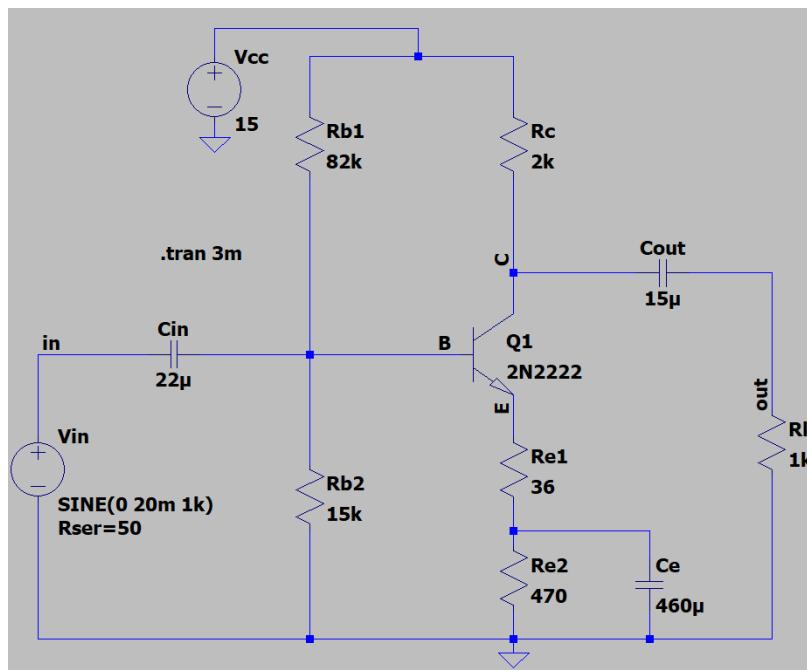
Since $v_{in} \sim v_{be} = v_e$

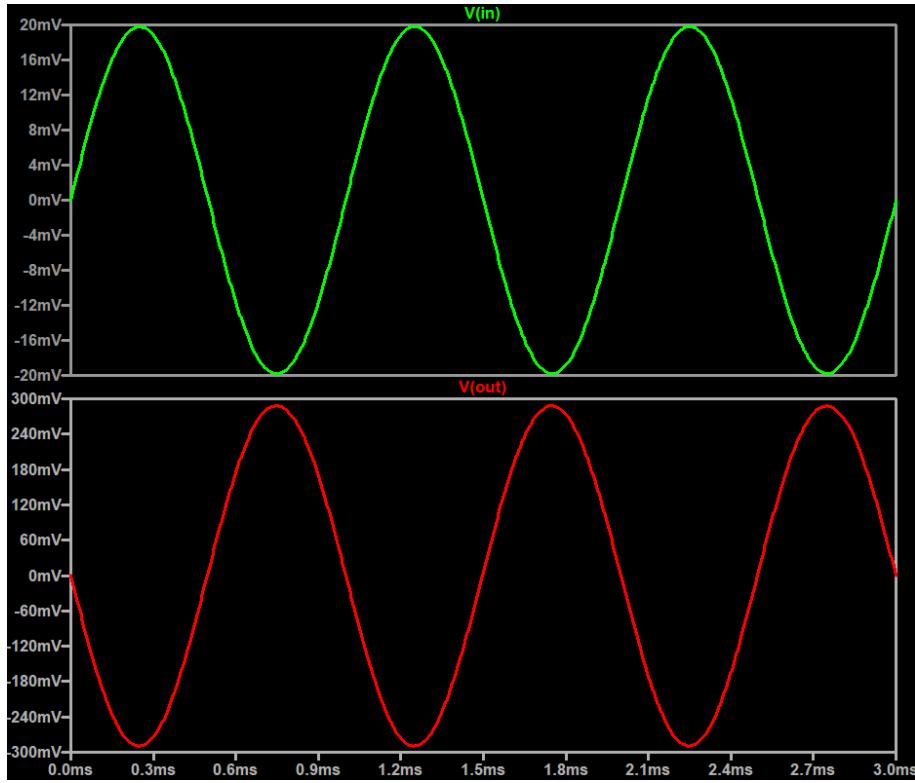
$$V_{in(\text{peak})} \ll 25\text{mV}$$

Typically, the limit for acceptable distortion in a fully bypassed CE stage is around 5mV to 10mV peak.

Ac negative feedback:

Quantity	Description	Calculations	Value
$V_{in(\text{peak})}$	New permissible input peak voltage		50mV
$A_v(\text{new})$	More realistic gain for better linearity		-15
R_{e1}	unbypassed to provide AC feedback and linearity	$A_v(\text{new}) = -rc / (r_e + R_{e1})$ $\Rightarrow R_{e1} = -rc/A(\text{new}) - r_e = 667 / 15 - 7.86$	$36.6 \sim 36\Omega$
R_{e2}	Bypassed by C_e for DC stability	$R_e - R_{e1} = 510 - 36$	$474 \sim 470\Omega$





FREQUENCY RESPONSE ANALYSIS

Low Frequency Analysis

Quantity	Description	Calculations	Value
Transistor's base resistance (Rin(base))		$B \cdot (r_e' + R_{e1}) = 200 \cdot (7.86 + 300)$	8.77kΩ
Input Impedance (Zin)		$R_{b1} \parallel R_{b2} \parallel R_{in(base)} = 82k \parallel 15k \parallel 8.77k$	5.18kΩ
fc (in)		$1 / (2\pi C_{in} (Z_{in} + R_s)) = 1/(2\pi \cdot 22 \cdot 10^{-6} \cdot (5180 + 50))$	1.39Hz
fc (out)		$1 / (2\pi C_{out} (Z_{out} + R_l)) = 1/(2\pi \cdot 15 \cdot 10^{-6} \cdot (2k + 1k))$	3.54Hz
Rseen	The resistance seen by Ce	$R_{e2} \parallel (r_e' + (R_{b1} \parallel R_{b2} \parallel R_s) / (B+1)) = 470 \parallel (7.86 + (82k \parallel 15k \parallel 50) (200 + 1))$	8Ω

fce		$1 / (2\pi C_e R_{seen}) = 1/(2\pi \cdot 460 \cdot 10^{-6} \cdot 8)$	*43.3Hz
fL	low-frequency cutoff	*max(fc(in), fc(out))	3.54Hz

*Calculated fce is very high and should be close to fc (in) and fc (out) and therefore ignored

High frequency analysis

High-frequency cutoff is determined by the parasitic capacitances within the transistor and any stray wiring capacitance. These capacitances act as low-pass filters.

Quantity	Description	Calculations	Value
Cbe	Base emitter capacitance, effects the input	2N2222	25pF
Cbc	Base collector capacitance, effects both input and output due to the Miller effect.	2N2222	8pF
Cmiller (Cm)		$C_{bc} \cdot (1 - A_v) = 8p \cdot (1 - (-15))$	128pF
Cin (total)		$C_{be} + C_m = 25p + 128p$	153pF
Rth		$R_s \parallel R_{b1} \parallel R_{b2} = 50 \parallel 82k \parallel 15k$	50
fH	high-frequency cutoff	$1/(2\pi R_{th} C_{in(\text{total})}) = 1/(2\pi \cdot 50 \cdot 153p)$	20.8MHz

Expected Results:

Quantity	Description	Calculations	Value
Gain (db)		$20 \cdot \log(15)$	23.5dB
Midband Range			3.54Hz - 20.8MHz
Midband Phase	-180° across the midband		
Low-Frequency Phase Shift	In high-pass filters the output voltage leads the input current as the frequency drops		-90°
High-Frequency	In a low-pass filter, the		-270°

Phase Shift	output voltage lags the input voltage.		
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