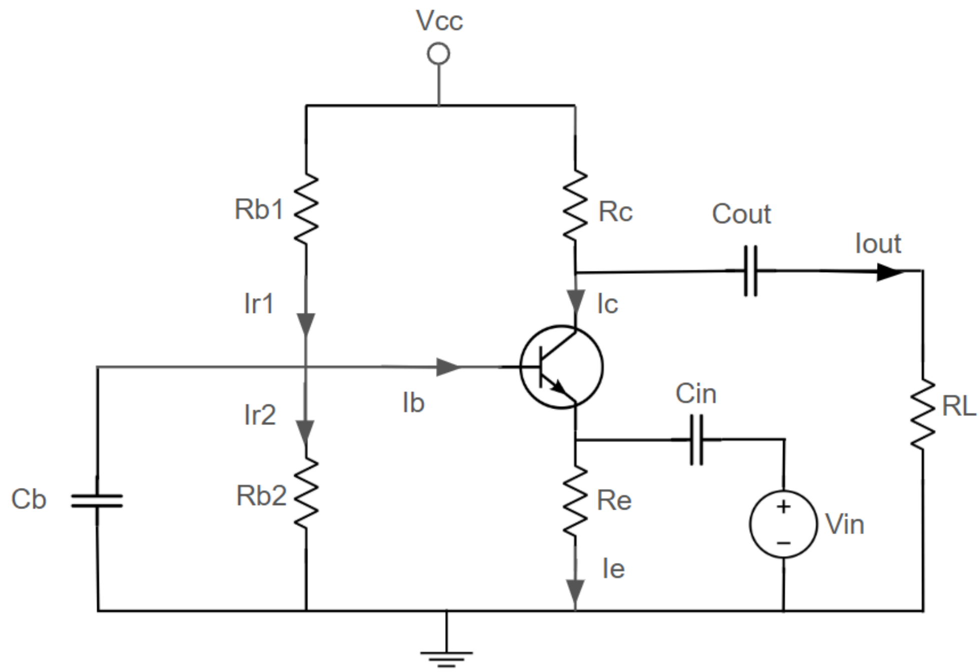
COMMON BASE AMPLIFIER

Theory



Transistor Operating Region

- Base-Emitter junction forward biased: 0.7V
- Base-Collector junction reversed biased: Vcb > 0
- Ic = β Ib

Quiescent Collector-Emitter Voltage: Vceq = ½ Vcc

Quiescent Collector Current:

- **Required AC Output Current:** It must be large enough to supply the AC load current without dipping into the cutoff region.
- **Transistor Power Dissipation:** Pd = Vceq * Icq. It must be kept below the transistor's maximum power rating. (Pd,max from datasheet)

Emitter Resistor Voltage Drop (Ve): It is set to improve bias stability against variations in β and temperature. General rule of thumb: Ve ~ 0.1Vcc

Since input impedance is quite low, Ac dynamic resistance is kept set equal to Rseries of voltage source.

LOAD POINT CALCULATIONS

Circuit pre-defined parameters

Component	Description	Value
Vcc	Collector Saturation Voltage	15V
Rseries	Voltage source series resistance	50Ω
re’	Dynamic emitter resistance	50Ω
Vce	Q-point collector emitter voltage	7.5V
Vbe	Forward bias base-emitter junction voltage	0.7V
β	2N2222 Transistor current gain	200
Ve	To stabilize the Q-point against variations in β, we typically ensure that the voltage across the emitter resistor Ve > Vbe	2

Emitter & Collector Resistor Calculations

Quantity	Calculation	Value
Ie	Vt / re’ = 25m / 50	0.5m
Ic	Ic ~ Ie	0.5m
Re	Ve / Ie = 2 / 0.5m	4kΩ
Vc	Vce + Ve = 7.5 + 2	9.5
Rc	(Vcc - Vc) / Ic = (15-9.5) / 0.5m	11kΩ
Vb	Ve + Vbe = 2 + 0.7	2.7V
Ib	Ic / β = 0.5m / 200	2.5uA

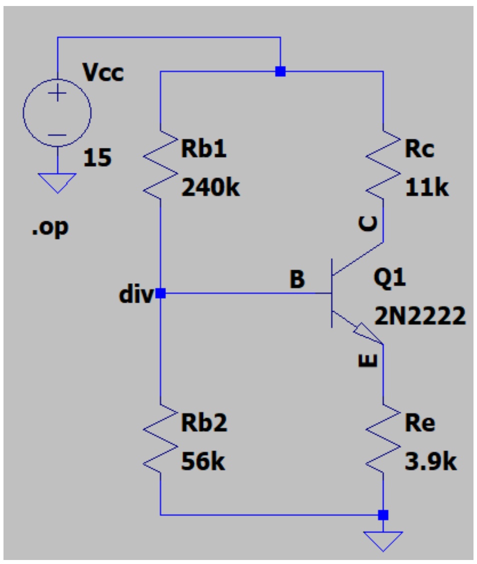
Bias Resistor Calculations

Important: Idiv = k * Ib, Here k has to be varied, so that simulation Vb matches the calculated Vb. (i.e. designing of Rb1 and Rb2 is trial and error)
Here we assume Idiv = 20 * Ib = 20 * 2.5uA = 50uA

Quantity	Calculation	Value
Rb1	(Vcc - Vb) / Idiv = (15-2.7) / 50u	246kΩ
Rb2	Vb / Idiv = 2.7 / 50u	54kΩ

Using E24 series (5% tolerance)

Quantity	Ideal	Standard	% change
Re	4k	3.9k	2.5
Rc	11k	11k	0
Rb1	246k	240k	2.5
Rb2	54k	56k	3.7




```
V(b):        2.72404       voltage
V(c):        9.14214       voltage
V(e):        2.08665       voltage
V(n001):     15            voltage
I(Rb1):      5.11498e-05   device_current
I(Rb2):      4.86436e-05   device_current
I(Rc):       0.000532533   device_current
I(Re):       0.000535039   device_current
I(Vcc):      -0.000583683  device_current
Ib(Q1):      2.50625e-06   device_current
Ic(Q1):      0.000532533   device_current
Ie(Q1):      -0.000535039  device_current
Is(Q1):      0             device_current
```

Ideal vs Simulation

Quantity	Ideal	Standard	% change
Vb	2.7	2.72404	0.89
Vc	9.5	9.14214	3.77
Ve	2	2.08665	4.33
Idiv	50u	51.1498u	2.3
Ib	2.5u	2.50625u	0.25
Ic	0.5m	0.532533m	6.5

AC PARAMETERS

Quantity	Description	Value
Rl	Load resistance	10kΩ
α	Current gain (β / (β + 1))	0.995
re’	Simulate dynamic emitter resistance (Vt / Ie)	46.7
Ie	Simulated emitter current	0.535m

Ac Parameter Design

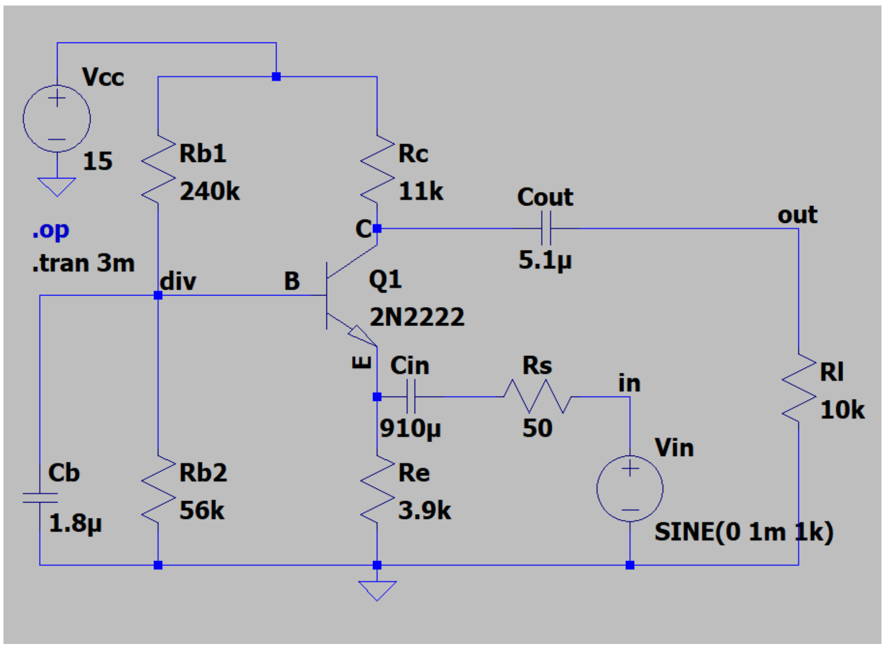
Quantity	Calculation	Value
Zin	Re || re’ = 3.9k || 46.7 (confirms low input impedance of CB configuration)	46.15Ω
Zout	Rc || Rl = 11k || 10k (confirms high input impedance of CB configuration)	5.24kΩ
Av (loaded voltage gain)	α * (Zout / Zin) = 0.995 * 5.24k / 46.15 (high voltage gain)	112.98
Avs (overall system gain)	Av * (Zin / (Zin + Rs)) = 112.98 * 46.15 / (46.1 + 50)	54.26
Cin	1 / (2 * pi * (fL / 10) * (Rs + Zin)) = 1 / (2 * pi * (20/10) * (50 + 46.15)	827.64uF~910uF
Cout	1 / (2 * pi * (fL / 10) * (Zout + Rc)) = 1 / (2 * pi * 20/10 * (5.24k + 10k))	4.9uF ~ 5.1uF
Rbypass	Rb1 || Rb2 = 240k || 56k	45.41kΩ
Ce	1 / (2 * pi * (fL / 10) * Rbypass) = 1 / (2 * pi * 20/10 * 45.41k)	1.75uF~1.8uF

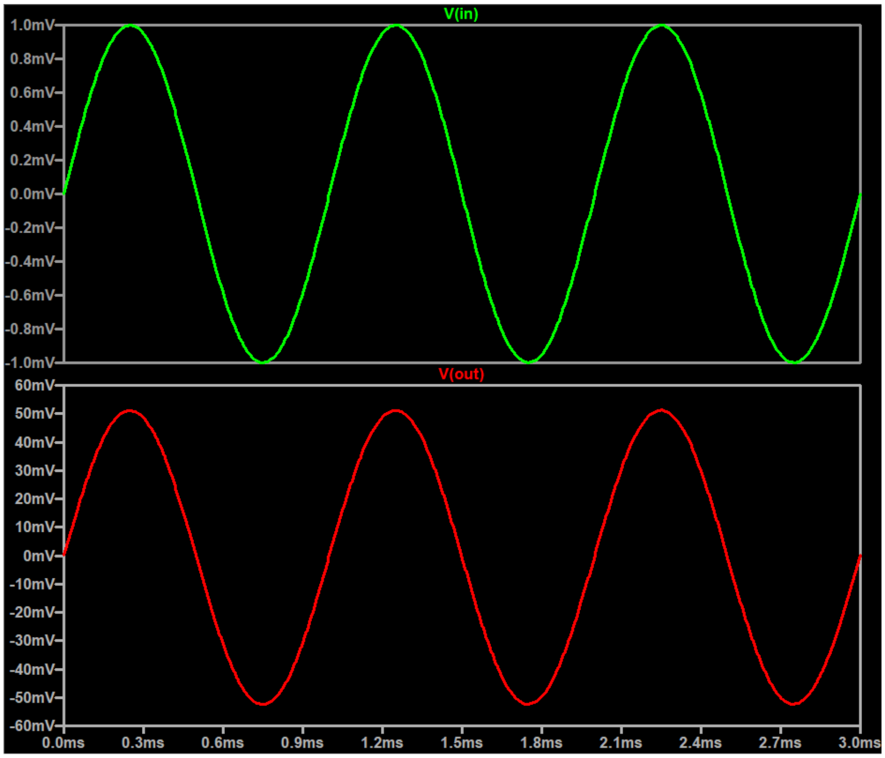
Frequency Analysis

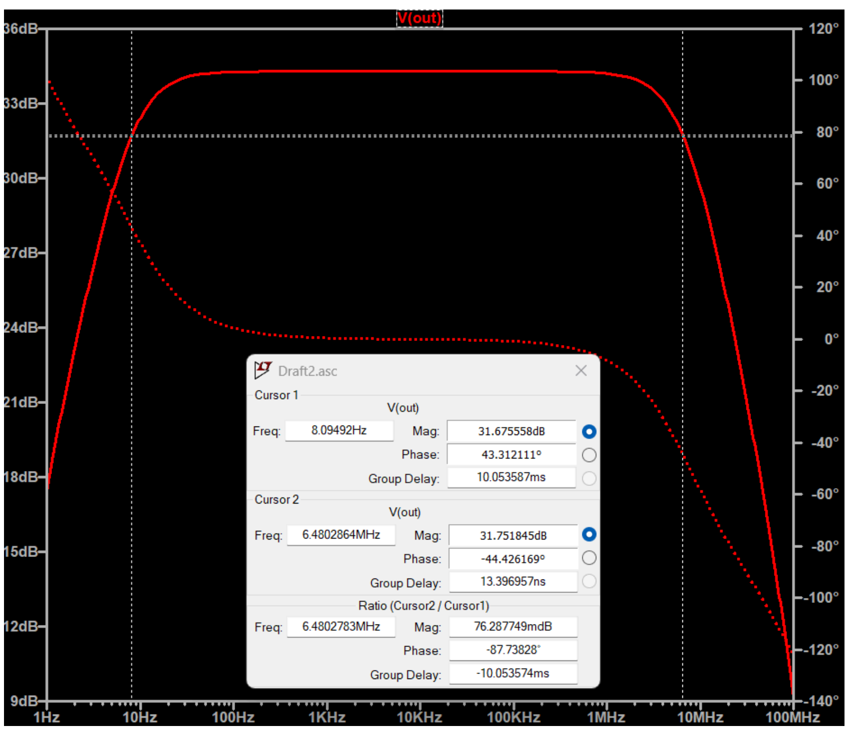
Quantity	Calculation	Value
fL1	1/(2*pi*(Rs+Zin)*Cin) = 1/(2*pi*96.1*910u)	1.82Hz
fL2	1/(2*pi*(Zout+Rl)*Cout) = 1/(2*pi*(5.24k+10k)*5.1u)	1.92Hz
fLB	1/(2*pi*Rbypass*Ce) = 1/(2*pi*45.41k*1.8u)	1.94Hz
Avs(dB)	20log10(Avs) = 20log10(54.26)	34.69dB

Cu	Output Capacitance for 2N2222	4.7pF
Cpi	Input Capacitance for 2N2222	25pF
fHout	1/(2*pi*Zout*Cu) = 1/(2*pi*5.24k*4.7p)	6.48MHz
fHin	1/(2*pi*(Rs||Zin)*Cpi) = 1/(2*pi*(50||46.7)*25p)	264.16MHz
fH	min(fHout, fHin) = min(3.79M, 264.16M)	6.48MHz

Results







Mismatch of fL: In theory, the overall fL is the highest single pole frequency. In practice, when all three frequencies (fL1, fL2, fL3) are close together, they interact and cause the overall cutoff frequency to shift higher than the highest single pole.