



Academic year 2023-2024 (ODD Sem)

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DEPARTMENT OF
COMPUTER SCIENCE & ENGINEERING

Date	22 nd Jan 2024	Maximum Marks	50
Course Code	MCE361T	Duration	90 Min
Sem	III Semester M.Tech CSE	CIE-1	

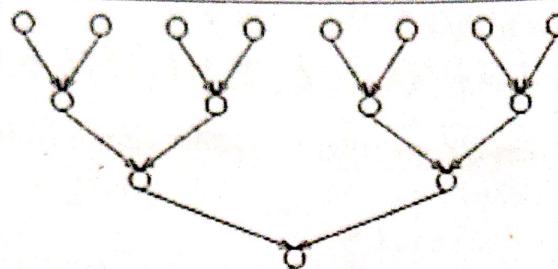
HIGH PERFORMANCE COMPUTING ARCHITECTURES

Sl. No.	Quiz	M	BT	CO
1	Consider the following measurements. Frequency of FP operations is 40%, average CPI of FP operations is 4.0 and average CPI of other instructions is 1.25. Calculate the total CPI.	2	L2	3
2.	Find the die yield for die that is 1.5 cm on a side assuming defect density of 0.4 per cm ² and $\alpha=4$	2	L1	2
3.	Compare speculative decomposition with exploratory technique	2	L2	1
4.	Identify the distinguishing characteristics of servers	2	L1	1
5.	Microprocessor today is designed to have adjustable voltage, so 15% reduction in voltage results in 15% reduction in frequency. Find the impact on dynamic power.	2	L2	2

Sl. No.	Questions	M	BT	CO
1. a	Consider the Frequency of FP operations to be 25%, Average CPI of FP operations to be 4.0, Average CPI of other instructions is 1.33, Frequency of FPSQR to be 2%, CPI of FPSQR as 20. Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5. Compare these two design alternative using the processor performance equation.	06	L3	3
.b	Identify the factors that are essential to find the speedup obtained from any enhancement made to the original system as per Amdahl's law.	04	L1	1
2.a	Discuss the various quantitative principles of computer design	06	L1	1
b	Assume that a web server is enhanced, new processor is 20 times faster on computation in the Web serving application than the original processor. Assuming that the original processor is busy with computation 50% of the time and is waiting for I/O 50% of the time, what is the overall speedup gained by incorporating the enhancement?	04	L2	2
3	For the task graphs given below, determine the following	07	L3	2



Academic year 2023-2024 (ODD Sem)



- i. Maximum degree of concurrency. 8
- ii. Critical path length.
- iii. Maximum achievable speedup over one process assuming that an arbitrarily large number of processes is available.
- iv. The minimum number of processes needed to obtain the maximum possible speedup. 4
- v. The maximum achievable speedup if the number of processes is limited to 2, 4 and 8.

3.b	Justify the effect of Moore's Law on the evolution of parallel programming paradigm	03	L3	1
4.	Analyze the commonly used decomposition techniques that are applied to broad classes of problems. <i>Recursive, Data, Exploratory, Spatial, Hybrid.</i>	10	L2	2
5. a	<p>Assume a disk subsystem with the following components and MTTF:</p> <ul style="list-style-type: none"> • 10 disks, each rated at 1,000,000-hour MTTF • 1 ATA controller, 500,000-hour MTTF • 1 power supply, 200,000-hour MTTF • 1 fan, 200,000-hour MTTF • 1 ATA cable, 1,000,000-hour MTTF <p>Using the simplifying assumptions that the lifetimes are exponentially distributed and that failures are independent, compute the MTTF of the system as a whole.</p>	05	L3	2
5.b	Apply recursive decomposition technique using quicksort for the data given below: 5,12,11,1,10,6,8,3,7,4,9,2 with a supporting task graph.	05	L3	4

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	17	30	08	05	14	20	26	-	-	-



Academic year 2023-2024 (ODD Sem)

DEPARTMENT OF
COMPUTER SCIENCE & ENGINEERING

Date	7 th March 2024	Maximum Marks	50
Course Code	MCE361T	Duration	90 Min
Sem	III Semester M.Tech CSE	CIE-2	

HIGH PERFORMANCE COMPUTING ARCHITECTURES

Sl. No.	Quiz	M	BT	CO
1.	Identify the characteristics of tasks in a parallel algorithm.	2	L1	1
2.	Define chunk scheduling. Identify the problems associated with chunk scheduling.	2	L2	1
3.	Any pattern of interaction with some structure that can be exploited for efficient implementation is	1	L1	1
4.	Examine MPI_ALL_Gather function with an example	2	L2	4
5.	API can be used where one root process send a different piece of the data to each one of the other processes	1	L1	3
6.	What purpose does a communicator serve in an MPI environment?	2	L2	2

Sl. No.	Questions	M	BT	CO
1.	Analyze the various methods used for containing interaction overheads in parallel programs.	10	L3	2
2.a	Analyze the commonly used parallel algorithm models	06	L1	1
2.b	Briefly Discuss the primitives provided by MPI for non-blocking communication <i>MPI_Isend, MPI_Irecv, MPI_Trecv, MPI_Wrecv</i>	04	L2	3
3.	Demonstrate any five collective communication and computation operations used in MPI. <i>Barrier, Broadcast, Reduction, Prefix, Gather, Scatter, AlltoAll</i>	10	L3	4
4.	Illustrate with an example deadlock occurrence using blocking communication primitives of MPI. Discuss how this could be avoided using non-blocking primitives. Indicate the key differences between the blocking operations and their non-blocking counterparts.	10	L2	2
5. a	Examine the various schemes for dynamic mapping of tasks onto processes	04	L1	1
5. b	Analyze cyclic and block cyclic distributions of mappings based on data partitioning with an example	06	L3	2

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	15	28	05	12	14	20	26	-	-	-



Academic year 2022-2023 (EVEN Sem)

DEPARTMENT OF
COMPUTER SCIENCE & ENGINEERING

Date	8 th April 2024	Maximum Marks	50
Course Code	MCE361T	Duration	90 Min
Sem	III Semester M.Tech CSE	Compensatory Test	

HIGH PERFORMANCE COMPUTING ARCHITECTURES

Sl. No.	Questions	M	BT	CO
1. a	Discuss the fork-join programming model supported by OpenMP	05	L2	1
1.b	With an example explain sections in OpenMP	05	L3	4
2.a	Write a C Code to demonstrate the parallel construct. Analyze the various clauses that are supported by parallel construct.	07	L3	4
2. b	Differentiate between LastPrivate and FirstPrivate clauses used in parallel loops of OpenMP	03	L2	2
3.	Write a sequential C code and a CUDA code for DAXPY loop	07	L4	4
3.b	Enumerate the three steps to the kernels parallelization process in OpenACC	03	L1	1
4. a	Identify the several innovations Fermi introduced to bring GPUs closer to mainstream system processors than Tesla and previous generations of GPU architectures	07	L2	2
4.b	Identify the three levels of parallelism in OpenACC execution model.	03	L1	2
5.	Consider the loop given below: for (i=0; i<100; i=i+1) { A[i+1] = A[i] + C[i]; /* S1 */ B[i+1] = B[i] + A[i+1]; /* S2 */ } Assume that A, B, and C are distinct, non-overlapping arrays. What are the data dependences among the statements S1 and S2 in the loop?	05	L3	3
5.b	Briefly Discuss FPGAs (Field Programmable Gate Arrays) with their benefits	05	L2	1

Course Outcomes:

CO1: Explore the fundamental concepts of parallel computer architecture

CO2: Analyze the performance of parallel programming

CO3: Design parallel computing constructs for solving complex problems.

CO4: Demonstrate parallel computing concepts for suitable applications

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	13	12	05	20	06	19	18	07	-	-
