April / May-2025 PG Examinations

USN 1 RV 23 SC S[redacted]

MCE361T

RV COLLEGE OF ENGINEERING®

(An Autonomous Institution affiliated to VTU, Belagavi)

III Semester Master of Technology (Computer Science Engineering)

HIGH PERFORMANCE COMPUTING ARCHITECTURE

Time: 03 Hours ***Maximum Marks: 100***

Instructions to candidates:

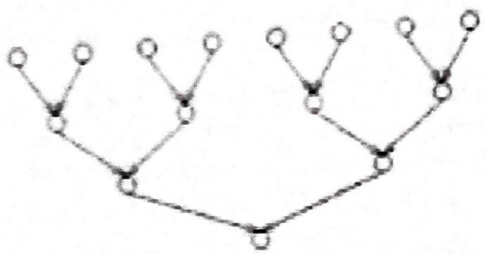
1. Answer FIVE full questions selecting one from each unit(1 to 5).
2. Each unit consisting of two questions of 20 marks each.

UNIT-1

			M	BT	CO
1	a	Square root is used in graphics processors and implementations of floating –point (FP) square root vary significantly in performance, if FP square root (FPSQR) is responsible for 20% of the execution time of a critical graphics benchmark. One option is to enhance the FPSQR hardware and speed up this operation by a factor of 10. The other option is to make all FP instructions in the graphics processor run faster by a factor of 1.6; FP instructions are responsible for half of the execution time for the application. The design team believes that they can make all FP instructions run 1.6 times faster with the same effort as required for the fast square root. Compare these two design alternatives.	06	2	1
	b	Discuss quantitative principles of computer design.	08	1	1
	c	State Amdahl's Law. Identify the factors that are essential to find the speedup obtained from any enhancement made to the original system as per Amdahl's law.	06	1	1
		OR			
2	a	Consider the Frequency of FP operations to be 25%, Average CPI of FP operations to be 4.0, Average CPI of other instructions is 1.33, Frequency of FPSQR to be 2%,CPI of FPSQR as 20. Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5.Compare these two design alternative using the processor performance equation.	08	3	2
	b	Examine the different types of parallelism. Write the Flynn's classification of computers into different categories.	08	1	1
	c	A web server is enhanced, new processor is 10 times faster on computation in the Web serving application than the original processor. Assuming that the original processor is busy with computation 40% of the time and is waiting for I/O 60% of the time, what is the overall speedup gained by incorporating the enhancement?	04	2	1

UNIT-2

3	a	Illustrate different types of data decomposition in detail with suitable examples.	09	2	1
	b	Differentiate between Static and Dynamic Mapping techniques used in parallel algorithms.	04	2	2
	c	Discuss some of the commonly used parallel algorithm models.	07	2	1
		OR			

4	a	For the task graphs given below, determine the following:  i) Maximum degree of concurrency. ii) Critical path length. iii) Maximum achievable speedup over one process assuming that an arbitrarily large number of processes is available. iv) The minimum number of processes needed to obtain the maximum possible speedup. v) The maximum achievable speedup if the number of processes is limited to (a) 2, (b)4, and (c) 8.	07	2	2
	b	Discuss the various characteristics of tasks and inter-task interactions that affect the choice of a good mapping.	10	2	2
	c	Write the differences between task interaction graph and task dependency graph.	03	2	2

UNIT-3

5	a	Write the syntax and use of any five collective communication and computation operations used in MPI.	10	3	3
	b	Write an MPI program to perform parallel odd-even sort.	10	3	4
		OR			
6	a	Illustrate with an example deadlock occurrence using blocking communication primitives of MPI. Discuss how this could be avoided using non-blocking primitives. Indicate the key differences between the blocking operations and their non-blocking counterparts.	10	3	2
	b	Write the syntax and the calling sequences of the functions used in MPI for partitioning the group of processes that belong to a communicator into subgroups each corresponding to a different communicator.	06	3	3
	c	Differentiate between Gather and Scatter operations used in MPI.	04	2	2

UNIT-4

7	a	Discuss the fork-join programming model supported by OpenMPI.	06	2	1
	b	Examine the need for single construct in OpenMP. Write the syntax and an example code using single construct.	06	2	3

	c	Consider a loop like this one:
		for(i=0;i<100;i=i+1)
		{
		A[i]=A[i]+B[i];/*S1*/
		B[i+1]=C[i]+D[i];/*S2*/
		}
		What are the dependences between S1 and S2? Is this loop parallel? If not, show how to make it parallel.
			08	3	2

		OR			

8	a	With an example explain sections in OpenMP.	06	3	1
	b	Illustrate a Multithreaded SIMD Processor with a simplified block diagram.	06	3	1
	c	Illustrate several innovations Fermi introduced to bring GPUs closer to mainstream system processors	08	2	1

UNIT-5

9	a	Illustrate the benefits and limitations of FPGAs(Field Programmable Gate Arrays)	06	2	2
	b	Typically two ways to offload work to co-processors in OpenACC are parallel and kernel regions. Discuss both of them with example.	08	3	3
	c	Write a parallel program using OpenACC to perform matrix multiplication.	06	2	4
		OR			
10	a	Identify the three levels of parallelism in OpenACC execution model	07	2	1
	b	Examine the use of Look Up Tables in FPGAs	03	2	2
	c	Explain any five data clauses of OpenACC	10	2	3