



Memory Managment - Part I

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- ▶ **Program** must be brought (from disk) into **memory** and placed within a **process** for it to be run.
 - **Machine instructions** may take **memory addresses** as arguments, but **not** disk addresses.
- ▶ The CPU fetches **instructions** from memory according to the value of the **program counter**.



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- ▶ Cache sits between main memory and registers.



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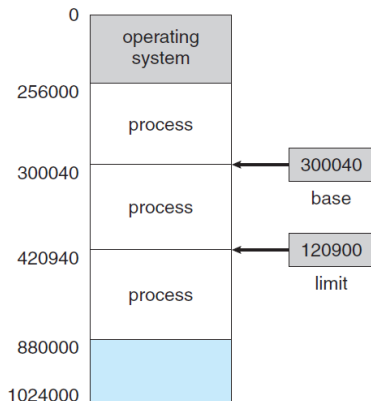


Address Protection

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- ▶ A separate memory space for each process.
 - Determining the range of legal addresses that the process may access.

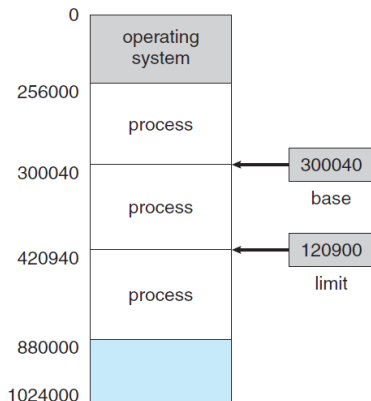
Base and Limit Registers

- ▶ A pair of **base** and **limit** registers define the **logical address space**.



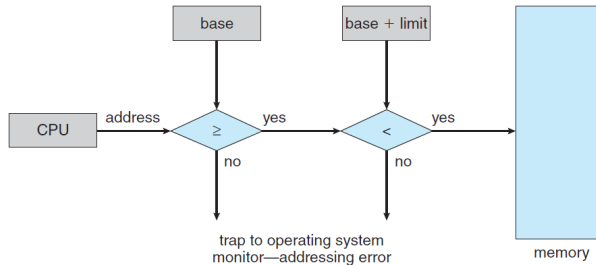
Base and Limit Registers

- ▶ A pair of **base** and **limit** registers define the **logical address space**.
- ▶ CPU must check every memory **access generated** in user mode to be sure it is **between base and limit** for that user.



Hardware Address Protection

- Any attempt by a user program to **access** OS memory or other users' memory results in a **trap to the OS**, which treats the attempt as a **fatal error**.



Address Binding



Address Binding

- ▶ Programs on **disk**, ready to be brought into **memory** to execute form an **input queue**.

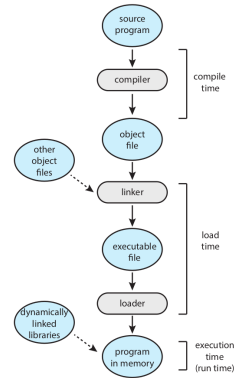


Address Binding

- ▶ Programs on **disk**, ready to be brought into **memory** to execute form an **input queue**.
- ▶ A user process can reside in any part of the **physical memory**.

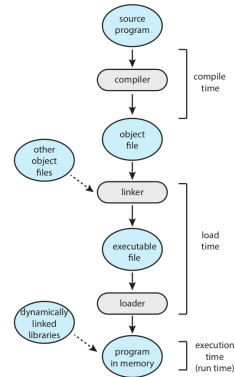
Binding of Instructions and Data to Memory (1/3)

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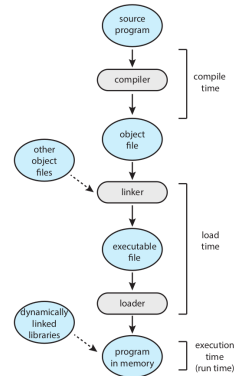
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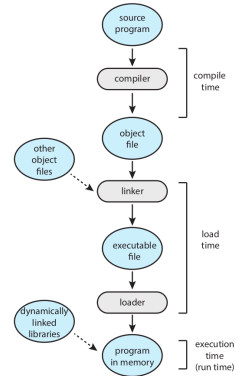
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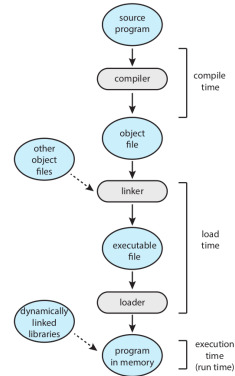
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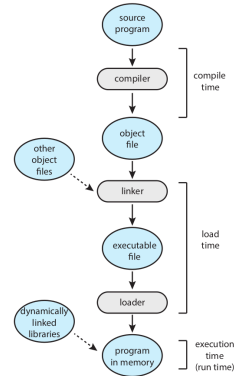
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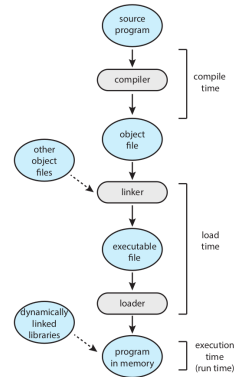
Binding of Instructions and Data to Memory (2/3)

- **Load time:** must generate **relocatable code** if memory location is not known at **compile time**.
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 - If the **starting address changes**, we need only **reload** the user code to incorporate this changed value.



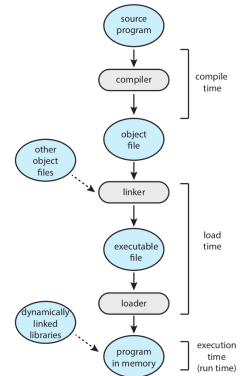
Binding of Instructions and Data to Memory (3/3)

- **Execution time:** binding delayed until run time if the process can be moved during its **execution** from one memory segment to another.
 - Need **hardware support**



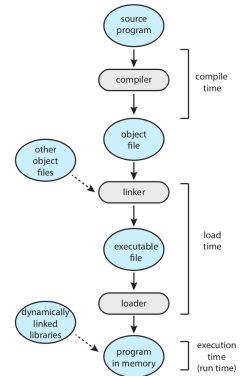
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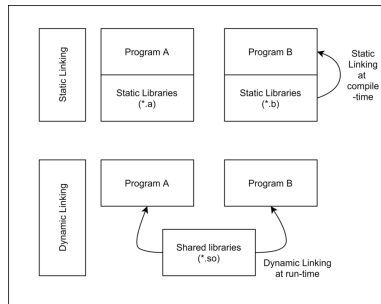
Linking and Loading

- ▶ **Linking:** connecting **all the modules** or the function of a program for **program execution**.
- ▶ **Loading:** loading the program from **disk to the main memory** for execution.



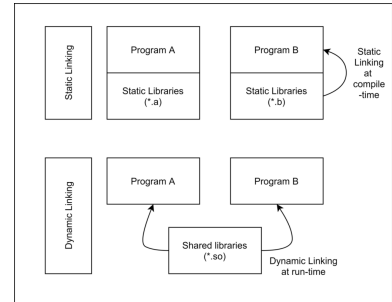
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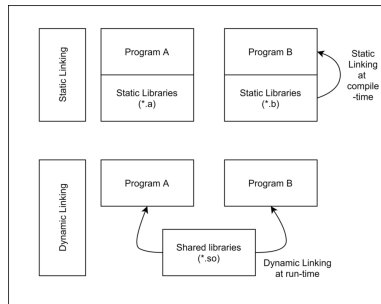
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- ▶ **Dynamic linking:** linking postponed until execution time.
 - Useful for shared libraries.





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- ▶ The main program is loaded into memory and is executed.
- ▶ When a routine is needed, if it has not been loaded, the loader loads the routine into memory.
- ▶ Better memory-space utilization; unused routine is never loaded.

Logical and Physical Address Space



Logical vs. Physical Address Space

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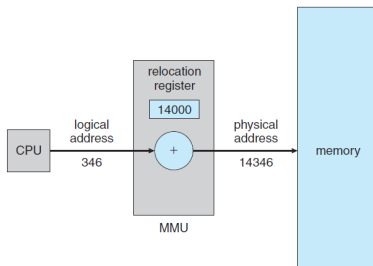


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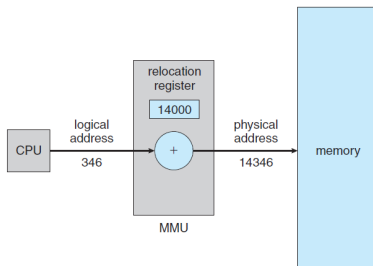
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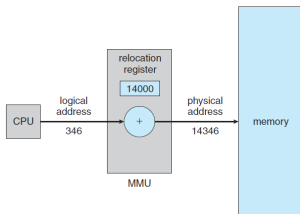
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 - Base register now called relocation register.



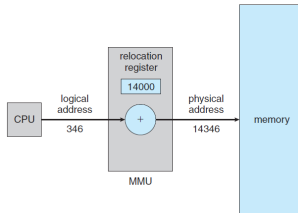
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 - Logical addresses: range 0 to max
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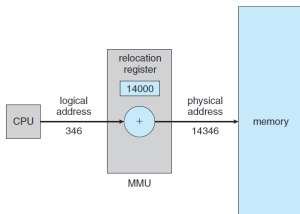
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- ▶ The user program generates only logical addresses and thinks that the process runs in locations 0 to max.
- ▶ These logical addresses must be mapped to physical addresses before they are used.



Swapping

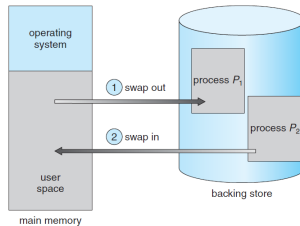


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- ▶ A process can be swapped temporarily out of memory to disk, and then brought back into memory for continued execution.

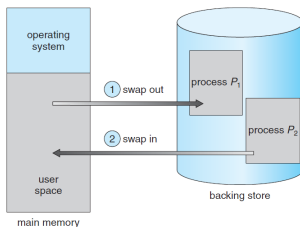
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- ▶ Major part of **swap time** is **transfer time**.





Swapping on Mobile Systems (1/2)

- ▶ Not typically supported.



Swapping on Mobile Systems (1/2)

- ▶ Not typically supported.
- ▶ Flash memory based
 - Small amount of space
 - Limited number of write cycles
 - Poor throughput between flash memory and CPU on mobile platform



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- ▶ **Android** **terminates** apps if low free memory, but first writes **application state** to flash for fast restart.

Contiguous Memory Allocation



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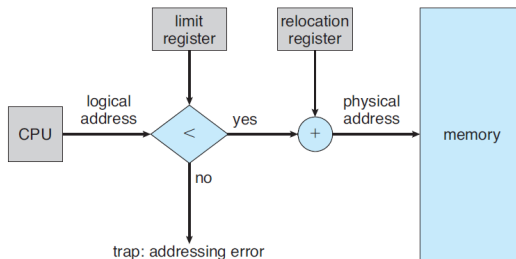


Contiguous Allocation (1/2)

- ▶ Main memory must support both OS and user processes.
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- ▶ Main memory usually into two partitions:
 - Resident OS and user processes memory address.
 - Each process contained in single contiguous section of memory.

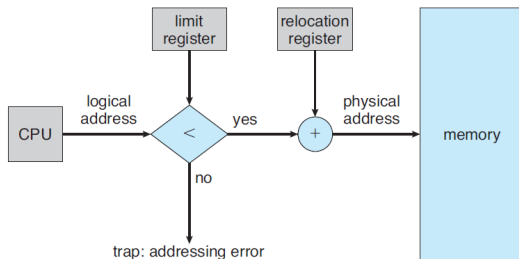
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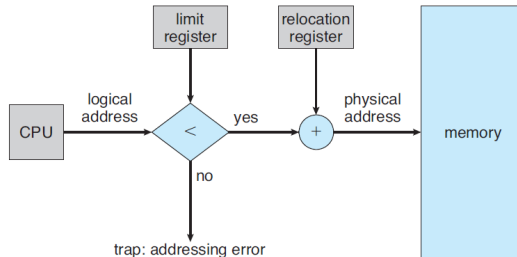
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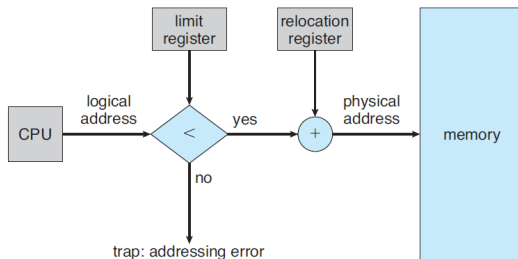
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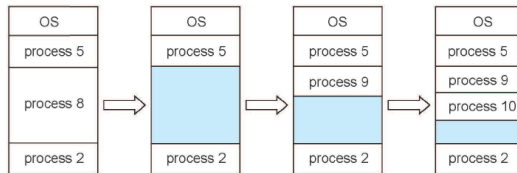
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 - **MMU** maps logical address **dynamically**.



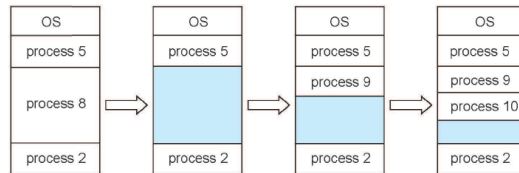
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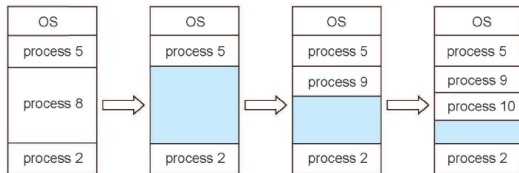
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- ▶ **Each partition** may contain **exactly one process**.
- ▶ When a partition is **free**, a process is selected from the input queue and is loaded into the **free partition**.





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- ▶ When a process arrives, it is allocated memory from a **hole large enough** to accommodate it.
- ▶ Process exiting **frees its partition**, **adjacent free partitions** combined.



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- ▶ **Worst-fit**: allocate the **largest hole**
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 - Produces the **largest leftover hole**.
- ▶ **First-fit** and **best-fit** **better** than **worst-fit** in terms of **speed and storage utilization**.



Fragmentation

- ▶ **External fragmentation:** total memory space exists to satisfy a request, but it is not contiguous.



Fragmentation

- ▶ **External fragmentation:** total memory space exists to satisfy a request, but it is not contiguous.
- ▶ **Internal fragmentation:** allocated memory may be slightly larger than requested memory; this size difference is memory internal to a partition, but not being used.



External Fragmentation

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- ▶ Another possible solution to the **external fragmentation** problem: permit the **logical address space** of the processes to be **noncontiguous**.

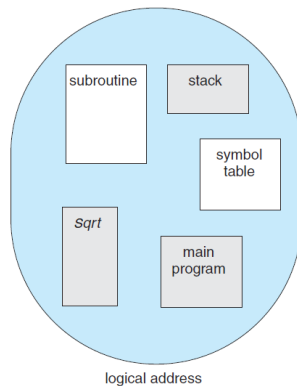
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- ▶ Two techniques:
 - **Segmentation**
 - **Paging**

Segmentation

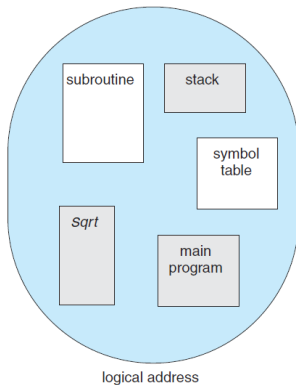
Segmentation

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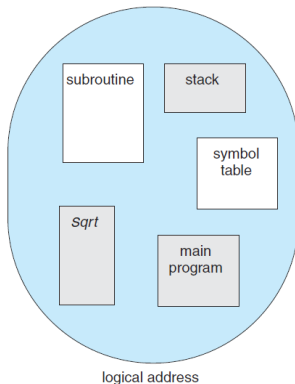
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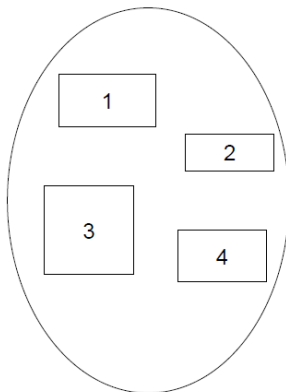


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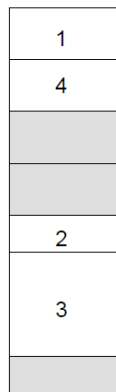
- ▶ Memory-management scheme supports **user view of memory**.
- ▶ A **program** is a collection of **segments**.
- ▶ A **segment** is a **logical unit** such as:
 - Main program
 - Procedure
 - Function
 - Object
 - ...



Logical View of Segmentation



user space



physical memory space



Segmentation Architecture

- ▶ **Logical address** consists of a tuple: $\langle \text{segment_number}, \text{offset} \rangle$



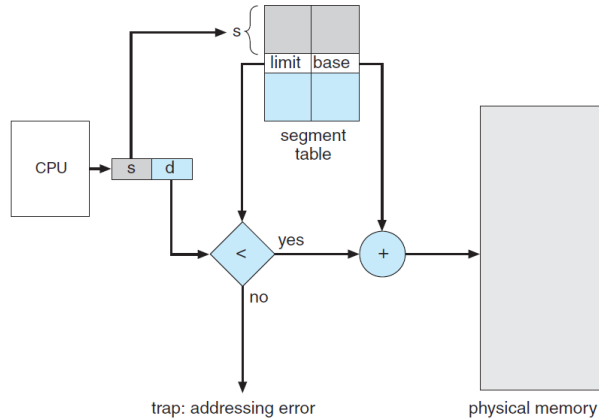
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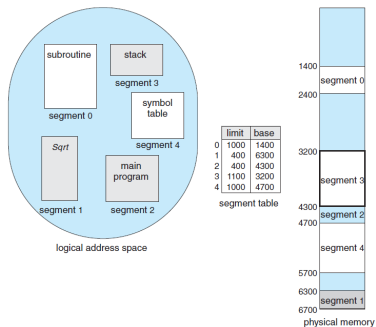
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- ▶ **Segment table**: maps **two-dimensional** user-defined addresses into **one-dimensional** physical address.
- ▶ Each table entry has:
 - **Base**: contains the **starting physical address** where the segments reside in memory.
 - **Limit**: specifies the **length** of the segment.

Segmentation Hardware

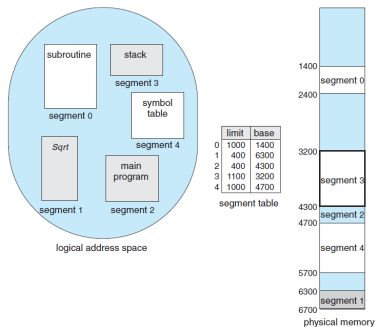


Segmentation Example



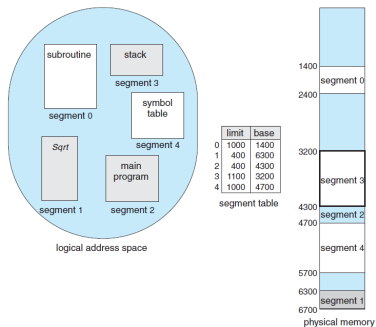
- A reference to byte 53 of segment 2:

Segmentation Example



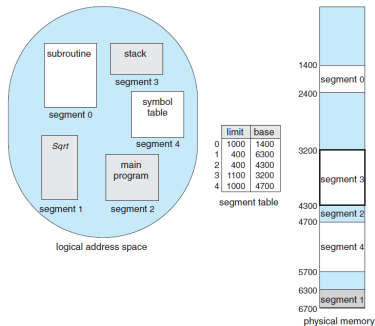
- A reference to byte 53 of segment 2: $4300 + 53 = 4353$

Segmentation Example



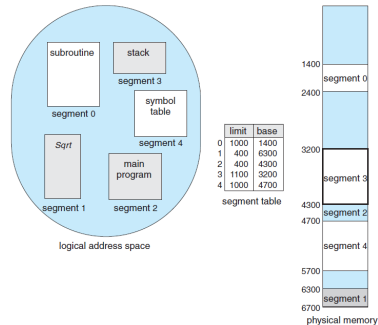
- ▶ A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- ▶ A reference to byte 852 of segment 3:

Segmentation Example



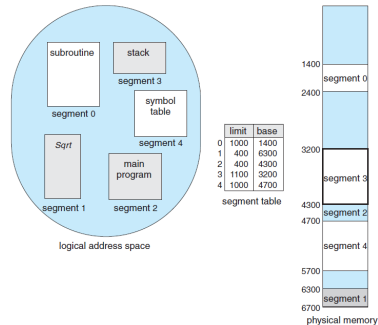
- ▶ A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- ▶ A reference to byte 852 of segment 3: $3200 + 852 = 4052$

Segmentation Example



- ▶ A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- ▶ A reference to byte 852 of segment 3: $3200 + 852 = 4052$
- ▶ A reference to byte 1222 of segment 0:

Segmentation Example



- ▶ A reference to byte 53 of segment 2: $4300 + 53 = 4353$
- ▶ A reference to byte 852 of segment 3: $3200 + 852 = 4052$
- ▶ A reference to byte 1222 of segment 0: **trap to OS**

Summary



Summary

- ▶ Main memory



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- ▶ Address protection: $\text{base} + \text{limit}$



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- ▶ External and internal fragmentation: compaction, segmentation, paging
- ▶ Segmentation: noncontiguous address, user view of memory

Questions?

Acknowledgements

Some slides were derived from Avi Silberschatz slides.