Memory Managment - Part II

Amir H. Payberah
payberah@kth.se
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Reminder

Reminder (1/3)

- External fragmentation vs. internal fragmentation

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- Compaction: shuffle memory contents to place all free memory together in one large block.

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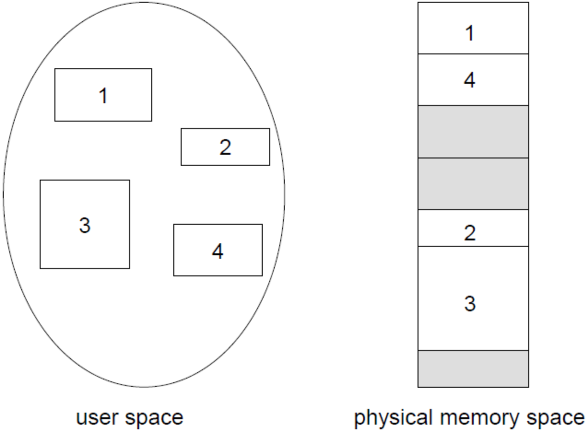
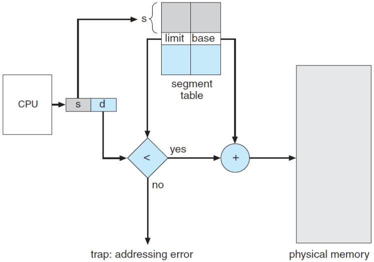
- External fragmentation vs. internal fragmentation
- Compaction: shuffle memory contents to place all free memory together in one large block.
- Other solutions:
  - Segmentation
  - Paging

Reminder (2/3)



Reminder (3/3)



s
limit
base
segment
table
CPU
s
d
<
yes
+
no
trap: addressing error
physical memory

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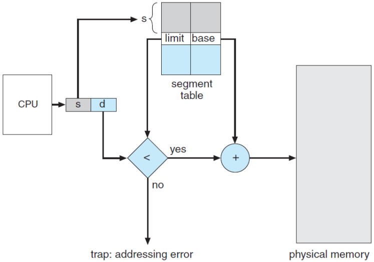
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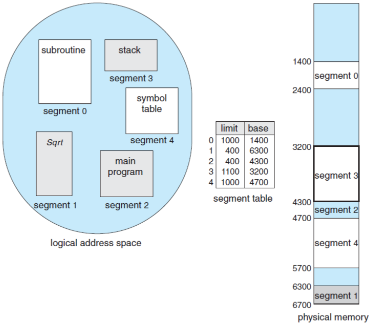
subroutine
stack
segment 3
symbol
table
segment 0
segment 4
Sqrt
main
program
segment 1
segment 2
logical address space
limit base
0 1000 1400
1 400 6300
2 400 4300
3 1100 3200
4 1000 4700
segment table
1400
segment 0
2400
3200
segment 3
4300
segment 2
4700
segment 4
5700
6300
segment 1
6700
physical memory

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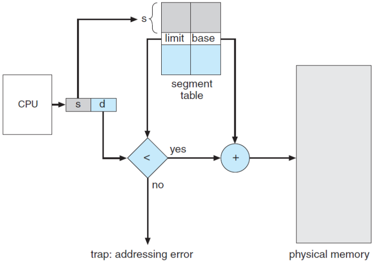

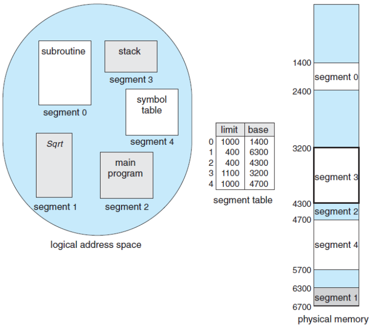

- A reference to byte 53 of segment 2:

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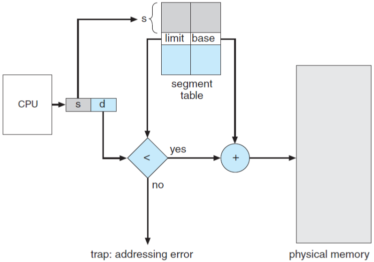

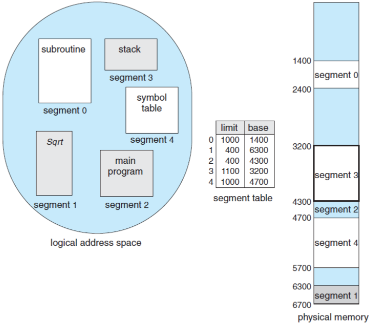

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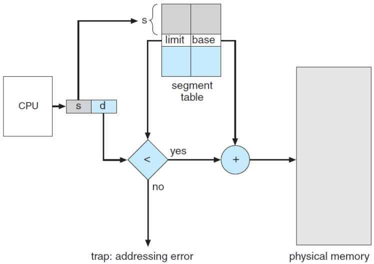

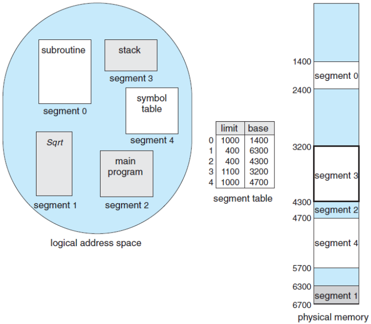

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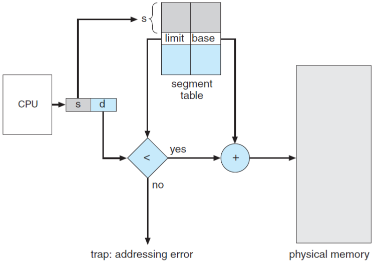

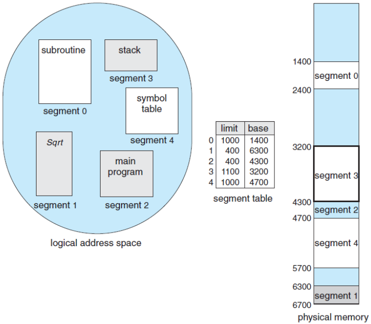

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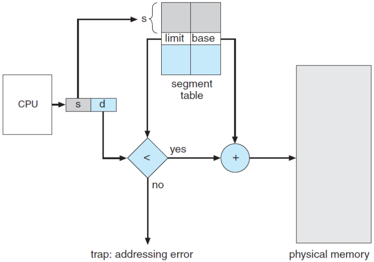

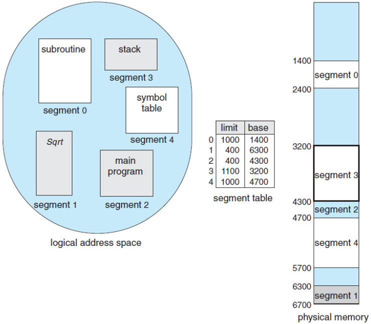

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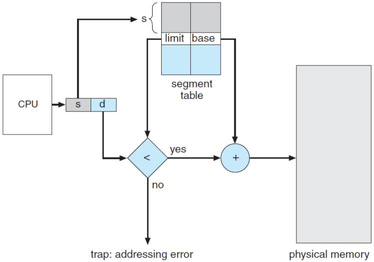

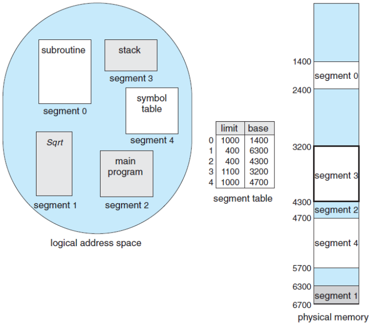

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Paging

Paging vs. Segmentation

- Segmentation and paging, both, permit the physical address space of a process to be noncontiguous.

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- Paging avoids external fragmentation and the need for compaction, whereas segmentation does not.

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- Divide physical memory into fixed-sized blocks called frames.
  - Size is power of 2, between 512 bytes and 16 Mbytes.
- Divide logical memory into blocks of same size called pages.

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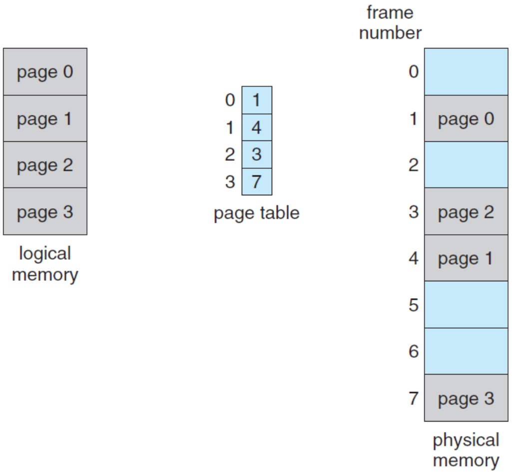
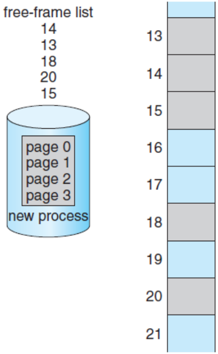
- To run a program of size N pages, need to find N free frames and load program.
- Set up a page table to translate logical to physical addresses.

Paging Model of Logical and Physical Memory

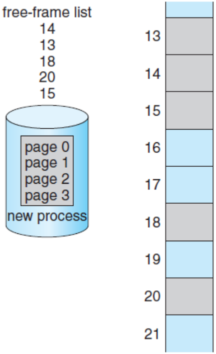


Free Frames

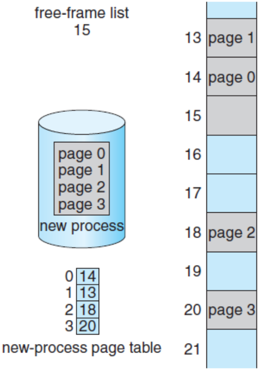


free-frame list
14
13
18
20
15
page 0
page 1
page 2
page 3
new process
13
14
15
16
17
18
19
20
21

Free Frames



before allocation



after allocation

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page number	page offset
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$m - n$	n

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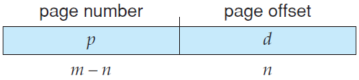
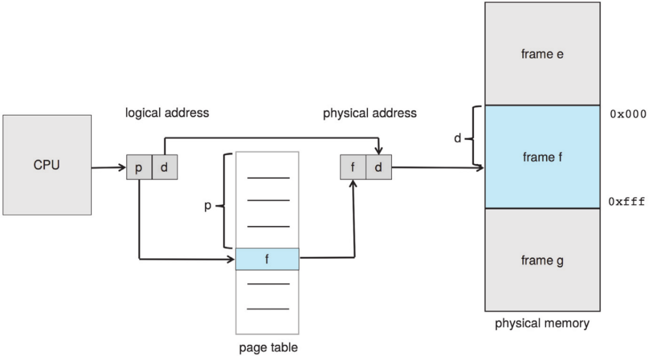


- For given logical address space 2^m and page size 2^n.

Paging Hardware



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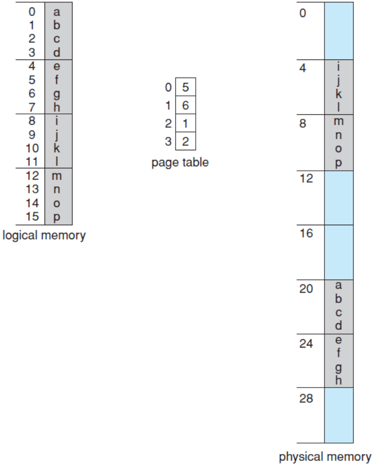

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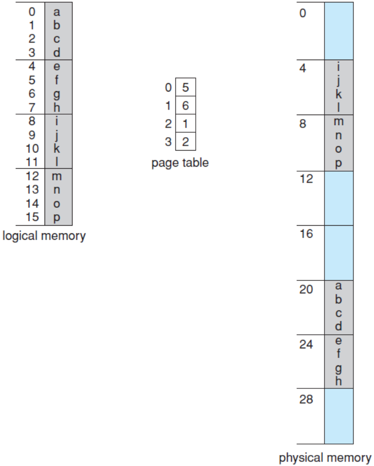
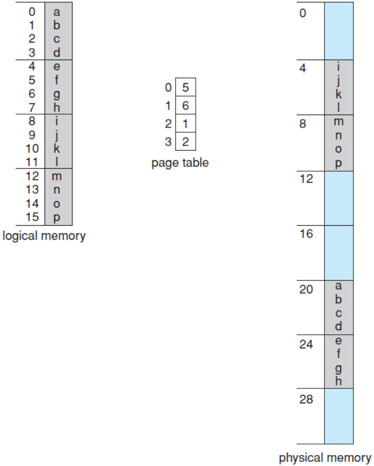


- The logical address:

Paging Example

- The logical address: $m = 4$ and $n = 2$



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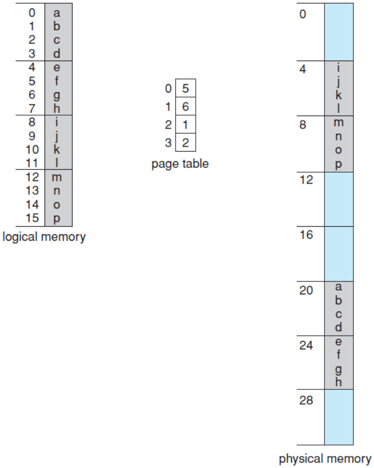

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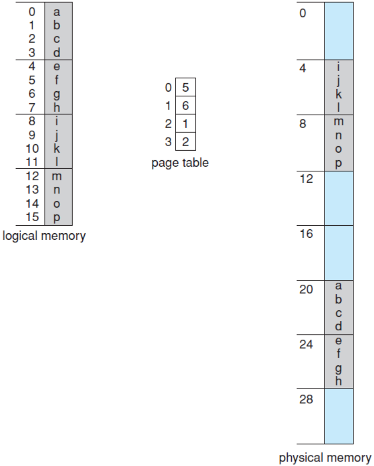

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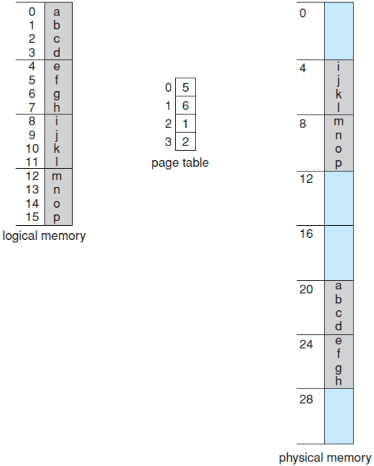

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- Logical address 10:

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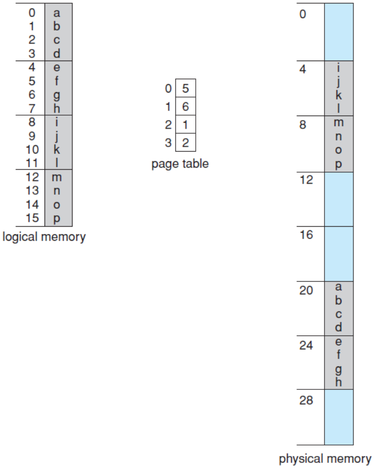

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- Logical address 10: $1 \times 4 + 2 = 6$

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- Pages typically are between 4 KB and 8 KB in size.

```
getconf PAGESIZE
```

Page Table Implementation

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- Page-table base register (PTBR) points to the page table.
- Page-table length register (PTLR) indicates size of the page table.
- In this scheme every data/instruction access requires two memory accesses.
  - One for the page table and one for the data/instruction.

Translation Look-aside Buffers (1/2)

- The two memory access problem can be solved by the use of a special fast-lookup hardware cache called translation look-aside buffers (TLBs).

Translation Look-aside Buffers (2/2)

- TLB

Page #	Frame #

Translation Look-aside Buffers (2/2)

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Translation Look-aside Buffers (2/2)

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Translation Look-aside Buffers (2/2)

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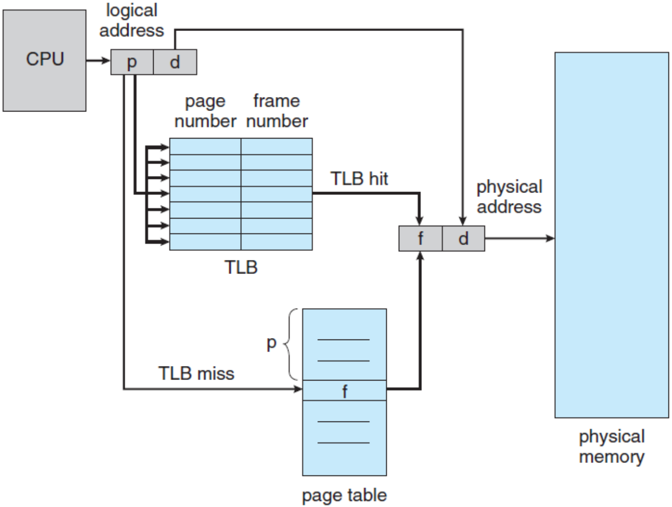
- Address translation (p, d)
  - If p is in TLB, get *frame#* out.
  - Otherwise, get *frame#* from page table.

Paging Hardware With TLB



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  - Don't want to allocate that contiguously in main memory.

Structure of the Page Table (2/2)

- Hashed Page Tables
- Hierarchical Paging

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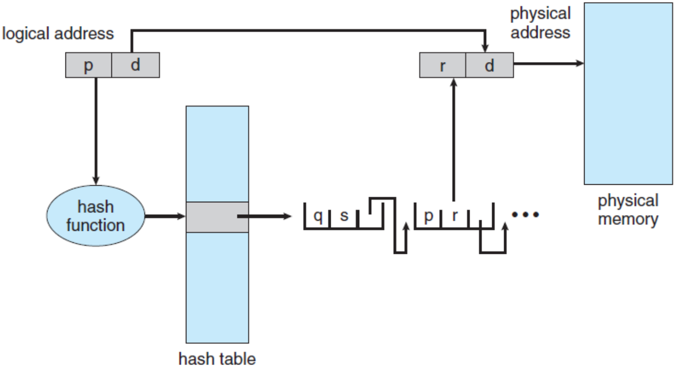
  3. A pointer to the next element

Hashed Page Table Architecture



Hierarchical Paging

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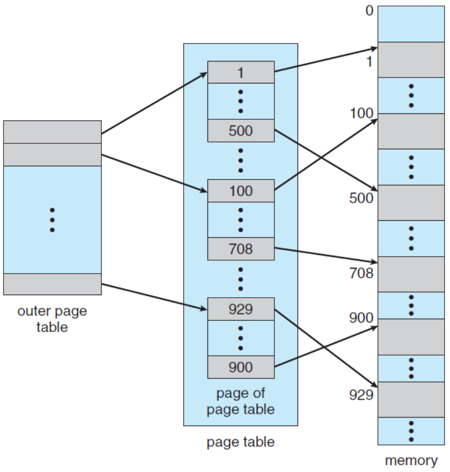
- We then page the page table.

Two-Level Page-Table Scheme



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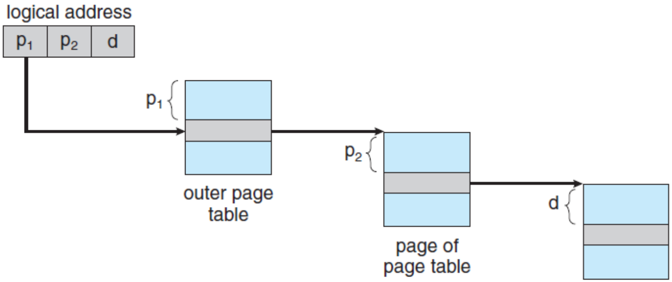
- Known as forward-mapped page table.

Address-Translation Scheme



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- Page table: translates logical to physical addresses
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- Page table structure: hierarchical paging, hashed page tables

Questions?

Acknowledgements

Some slides were derived from Avi Silberschatz slides.