MATLAB Transient Circuit Simulator

ECEN 751: Advanced Computational Methods for Integrated System Design

Project 01

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***Abstract*— In this project a Transient Circuit Simulator was developed using Matlab 2015b which performs transient analysis on circuits containing linear elements (resistors, capacitors, inductors, ideal current sources and ideal voltage sources) as well as nonlinear elements (MOS transistors). Forward Euler, Backward Euler and Trapezoidal integration methods were implemented for the linear transient simulator. The linear transient simulator was extended to a nonlinear transient simulator. The multi-dimensional Newton- Raphson method was implemented to obtain the nonlinear transient analysis. The nonlinear DC solution was obtained using gmin stepping. In the developed circuit simulator a simplified version of SPICE level 1 MOS model was used. The parasitic capacitors in the MOS model were assumed to be linear.**

Keywords— circuit simulator; transient analysis; Newton-Raphson method; gmin stepping; parasitic capacitors

I. INTRODUCTION

Circuit simulation is an essential and routinely used design tool for verifying the design of electrical and electronic circuits and systems. Circuit simulation involves the combination of the following: (a) mathematical modeling of the circuit elements, (b) formulation of the circuit equations, and (c) techniques for solution of these equations. The first general- purpose circuit simulator was SPICE (Simulation Program with Integrated Circuit Emphasis), developed at the University of California, Berkeley, which experienced widespread usage.

Most general purpose circuit simulators provide the capabilities of performing Linear DC analysis, Nonlinear DC analysis, Linear AC analysis, Small Signal AC analysis, Linear Transient analysis and Nonlinear Transient analysis. The behavior of a circuit is captured by a set of equations that are formulated by combining the device model equations and Kirchoff's Current and Voltage Laws (KCL and KVL). A popular approach for a systematic and automatic equation formulation is the Modified Nodal Analysis (MNA).

In this project a transient circuit simulator was developed. The circuit was loaded in the form of a simple netlist. Section 2 describes the techniques of device modeling, equation formulation and solution involved in Linear DC and Transient Analysis. Section 3 explains the techniques used in Non Linear DC and Transient Analysis. Section 4 discusses the experiments and results obtained using the benchmark circuits.

II. LINEAR DC AND TRANSIENT ANALYSIS

A. Linear DC Anayslsis

Linear DC analysis gives the circuit solution at time =0. The linear elements of the circuit are stamped one at a time to get a set of equations which resemble the equations of KVL and KCL. The set of equations obtained reduces to solving the linear system

$$\mathbf{Y}\, v = \boldsymbol{J}$$

While computing the DC Solution, the capacitors are replaced by open circuits (a current source with I = 0) and the inductors are replaced by short circuits (a voltage source with V=0).

B. Linear Transient Anayslsis

Transient analysis involves computing the waveforms of a circuit as a function of time. The challenge in transient analysis is to move forward in time by integrating the currents of capacitors (*dv/dt*) and the voltage of inductors (*di/dt*). In this project one–step integration approximations were implemented for the capacitors and the inductors. The methods of one-step integration approximations that were implemented include Forward Euler (FE), Backward Euler (BE) and Trapezoidal Integration (TR). The general flow of Linear Transient Analysis is shown in Figure 1.

A resistor of value R between nodes N+ and N- is stamped as shown in Figure 2. A current source with branch current Ik from node N+ to node N- is stamped to the right hand side J vector as shown in Figure 3. Independent voltage sources are stamped using Modified Nodal analysis where a new variable i_k is introduced which represents the voltage source current. A new voltage constraint is added which represents the equation below

$$V_{N+} - V_{N-} = V\_k$$

where, V_k is the value of the voltage source, N+ and N- are the nodes of the voltage source. The procedure for stamping voltage source is depicted in Figure 4.

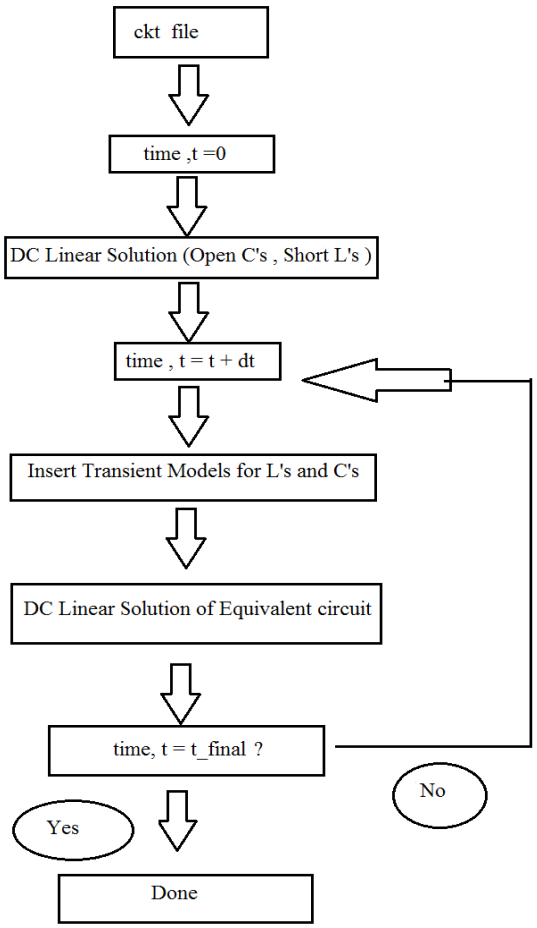


Figure 1: General Flow of Linear Transient Circuit Simulator

MNA Matrix

	N+	N-
N+	1/R	-1/R
N-	-1/R	1/R

Figure 2: Resistor Stamp

RHS J vector

N+	-Ik
N-	+Ik

Figure 3: Stamping current source

MNA Matrix

	N+	N-	i_k
N+			+1
N-			-1
i_k	+1	-1	

J vector

V_k

Figure 4: Stamping of independent voltage Source

The stamping of the capacitor during transient analysis was performed using three techniques, namely, Forward Euler (FE), Backward Euler (BE) and Trapezoidal Integration (TR). The capacitor voltage in terms of the integral of the capacitor current is given below

$$v(t + \Delta t) = v(t) + \frac{1}{C}\int_{t}^{t+\Delta t} i(\tau)d\tau$$

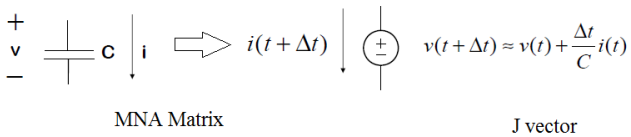
The equations for Forward Euler, Backward Euler and Trapezoidal Integration of a capacitor are given below

$$v(t + \Delta t) \approx v(t) + \frac{1}{C}\Delta t\,.\,i(t) \quad \text{(FE)}$$

$$v(t + \Delta t) \approx v(t) + \frac{1}{C}\Delta t\,.\,i(t + \Delta t) \quad \text{(BE)}$$

$$v(t + \Delta t) \approx v(t) + \frac{\Delta t}{2C}[i(t) + i(t + \Delta t)] \quad \text{(TR)}$$

The FE, BE and TR Thevenin and Norton models for a capacitor along with the stamping implemented are shown in Figure 5, Figure 6 and Figure 7 respectively. The Trapezoidal integration is in general more accurate than either FE or BE and it lies between the two in terms of its stability behavior.



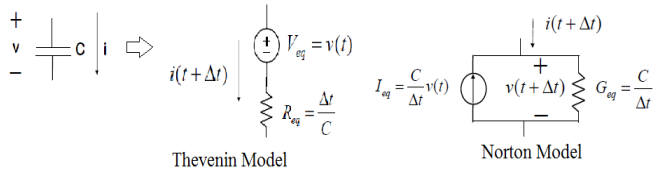
MNA Matrix

	N+	N-	i_k
N+			+1
N-			-1
i_k	+1	-1	

J vector

v(t) + dt i(t)/C

Figure 5: Forward Euler Model of Capacitor



MNA Matrix

	N+	N-	i_k
N+			+1
N-			-1
i_k	C/h	-C/h	-1

J vector

(C/ h) v(t-h)

Figure 6: Backward Euler Model of Capacitor

Similar procedure is adopted in stamping an inductor during transient analysis. The integral equation of the current of an inductor is given below

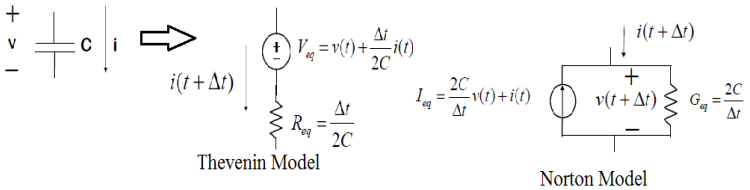
$$i(t + \Delta t) = i(t) + \frac{1}{\mathbf{L}} \int_{t}^{t+\Delta t} v(\tau) dt$$

The equations for Forward Euler, Backward Euler and Trapezoidal Integration for an inductor are given below

$$i(t + \Delta t) \approx i(t) + \tfrac{1}{\mathbf{L}} \Delta t \,.\, v(t) \quad \text{(FE)}$$

$$i(t + \Delta t) \approx i(t) + \tfrac{1}{\mathbf{L}} \Delta t \,.\, v(t + \Delta t) \quad \text{(BE)}$$

$$i(t + \Delta t) \approx i(t) + \tfrac{\Delta t}{\mathbf{2L}} [v(t) + v(t + \Delta t)] \quad \text{(TR)}$$



MNA Matrix

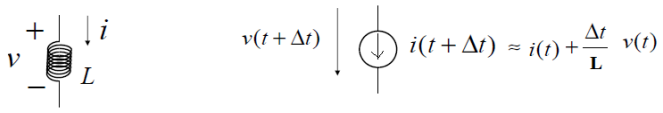
	N+	N-	i_k
N+			+1
N-			-1
i_k	2 C/h	-2C/h	-1

J vector

(2C/h) v(t-h) + i(t-h)

Figure 7: Trapezoidal Integration model of Capacitor

The FE, BE and TR Thevenin and Norton models for an inductor along with the stamping implemented are shown in Figure 8, Figure 9 and Figure 10.



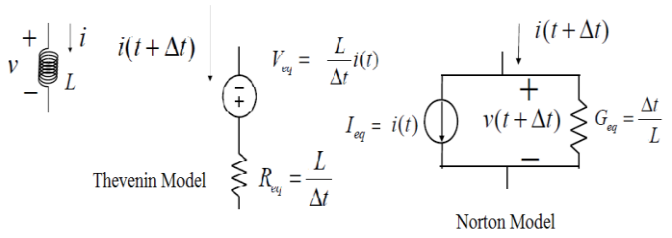
MNA Matrix

	N+	N-	i_k
N+			+1
N-			-1
i_k			+1

J vector

i (t - h) + (h/L) v(t- h)

Figure 8: Forward Euler Model of Inductor



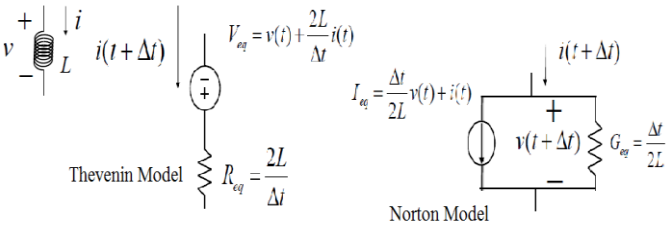
MNA Matrix

	N+	N-	i_k
N+			+1
N-			-1
i_k	+1	-1	-L / h

J vector

- (L/h) i(t-h)

Figure 9: Backward Euler Model for an Inductor



MNA Matrix

	N+	N-	i_k
N+			+1
N-			-1
i_k	+1	-1	- 2L/h

J vector

-(2L/h) i(t-h) + (- v(t-h))

Figure 10: Trapezoidal Integration Model for an inductor

III. Nonlinear DC and Transient Analysis

The Linear Transient Simulator was extended to a Nonlinear Transient Simulator. The technique of gmin stepping was used to obtain the DC Nonlinear Solution. The Nonlinear Transient Analysis was achieved using multi-dimensional Newton Raphson method in the inner loop to do the nonlinear iterations.

A. *Nonlinear DC Solution*

The challenge in Nonlinear DC analysis lies in the dealing with the floating points in the circuits due to the nonlinear elements. If the method used in Linear DC analysis is directly applied to find the Nonlinear DC solution the MNA matrix obtained would be singular. The technique of gmin stepping is used to overcome this problem. It is a special trick which involves finding the initial guess by attaching a small "dummy" conductance between each node and the ground to aid the nonlinear DC solution convergence. The procedure of gmin stepping is described as follows:

(a) Connect R= 1/g between each node and the ground.

(b) Assign a large value to g (say R = 0. 1Ω).

(c) Perform Newton- Raphson iterations for the assigned value of g after linearizing the nonlinear elements in the circuit.

(d) Increase R from 0.1Ω to 1Ω, (equivalent to decreasing g) and repeat Newton- Raphson iterations for the new value of R with the initial guess as the solution obtained in previous step.

(e) Keep increasing R (decreasing g) and solve every time.

(f) When R = 10^{12} Ω, which is as good as open circuit, stop the procedure.

The solution obtained after step (f) is considered as the DC Nonlinear solution for the original circuit.

B. *Nonlinear Transient Analysis*

During the transient analysis, the multi-dimensional Newton Raphson iterative process repeats for each individual time step. The Newton- Raphson procedure is summarized as follows

(a) Guess circuit voltages at time =t.
(b) Obtain the linearized models for all the nonlinear elements about their presumed operating points.
(c) Formulate nodal equations that characterize the linearized circuit and solve them for the new presumed operating points.
(d) Return to step (a) using the solution of step (c) as "guesses" unless the change from the last iteration is less than the error tolerance. If the change is smaller than the error tolerance, then the iteration terminates successfully. If the number of iterations has exceeded a predetermined number of iterations, then the solution procedure has failed.

Figure 11 shows the general flow of the Nonlinear Transient Analysis.

The MOSFET models used in the project correspond to the simplified version of SPICE level 1 MOS model. The model formulae for NMOS is given below

Cut-off: $Vgs \leq Vt$

$Ids = 0$

Linear: $Vgs > Vt \; and \; Vds \leq Vgs - Vt$

$$Ids = \mu \, Cox \, \frac{W}{L} \left((Vgs - Vt)Vds - \frac{1}{2} Vds^2 \right) (1 + \lambda \, Vds)$$

Saturation: $Vgs > Vt \; and \; Vds > Vgs - Vt$

$$Ids = \frac{1}{2}\,\mu Cox\,\frac{W}{L}\,(Vgs - Vt)^2\,(1 + \lambda\, Vds)$$

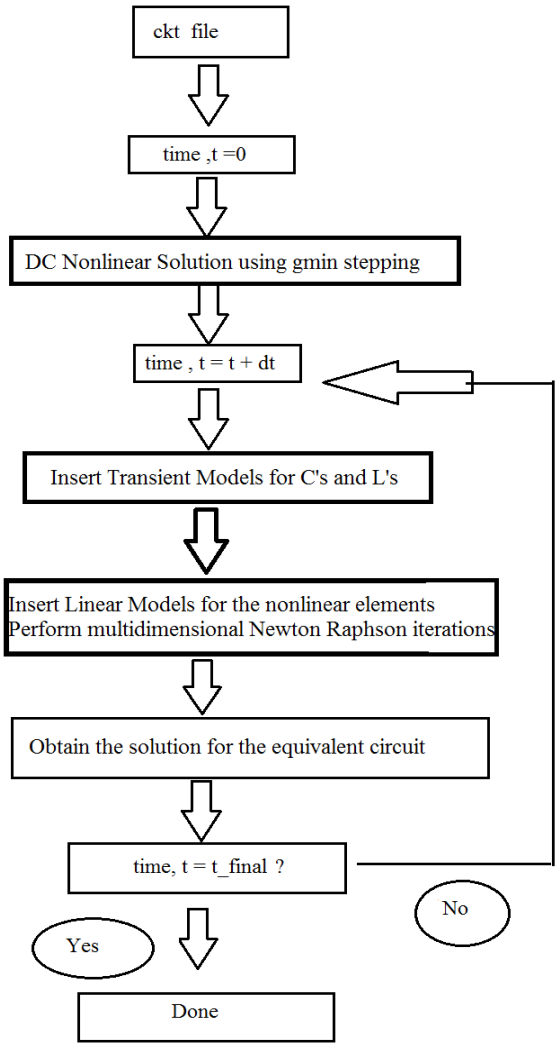


Figure 11: Nonlinear Transient Analysis General Flow

The model formulae for PMOS is given below

Cut-off: $Vsg \leq -Vt$

$$Isd = 0$$

Linear: $Vsg > -Vt \; and \; Vsd \leq Vsg - (-Vt)$

$$Isd = \mu\, Cox\,\frac{W}{L}\left((Vsg - (-Vt))Vsd - \frac{1}{2}\,Vsd^2\right)(1 + \lambda\, Vsd)$$

Saturation: $Vsg > -Vt \; and \; Vsd > Vsg - (-Vt)$

$$Isd = \frac{1}{2}\,\mu Cox\,\frac{W}{L}\,(Vsg - (-Vt))^2\,(1 + \lambda\, Vsd)$$

The Jacobian was constructed in terms of the linearized stamps that represent the MOSFET models. At each N-R iteration, the node voltage solution in the previous solution is used to compute the appropriate derivatives. The equations involved in linearizing the NMOS model is given below

$$ig = f_1(Vgs, Vds) = 0$$

$$id = f_2(Vgs, Vds) = ids$$

$$is = -ig - id = -ids$$

$$ig^k + \Delta ig^k = 0$$

$$id^k + \Delta id^k = f_2(Vgs^k, Vds^k) + \frac{df_2}{dVgs}\,(Vgs^{k+1} - Vgs^k) + \frac{df_2}{dVds}\,(Vds^{k+1} - Vds^k)$$

$$is^k + \Delta\, is^k = -(id^k + \Delta id^k)$$

where, the partial derivatives are known as the small-signal transconductance

$$\frac{df_2}{dVgs} = \frac{ids}{dVgs} = gm$$

and the small- signal drain to source conductance

$$\frac{df_2}{dVds} = \frac{ids}{dVds} = Gds$$

The final N-R linearized NMOSFET model implemented is described by the equation given below

$$ids^{k+1} = ids^k + gm^k\,(Vgs^{k+1} - Vgs^k) + Gds^k\,(Vds^{k+1} - Vds^k)$$

Similarly, the N-R linearized model for a PMOSFET is given by the equation given below

$$isd^{k+1} = isd^k + gm^k\,(Vsg^{k+1} - Vsg^k) + Gsd^k\,(Vsd^{k+1} - Vsd^k)$$

The linearized models of NMOS and PMOS are shown in Figure 12 and 13 respectively.

$$i_{ds}^{k+1} = i_{ds}^k + g_m \Delta v_{gs}^k + G_{ds}^k \cdot \Delta v_{ds}^k \qquad \Delta v_{gs}^k = \left(v_{gs}^{k+1} - v_{gs}^k\right)$$

$$Ieq^k = ids^k + gm^k\,(-Vgs^k) + Gds^k\,(-Vds^k) \qquad \Delta v_{ds}^k = \left(v_{ds}^{k+1} - v_{ds}^k\right)$$

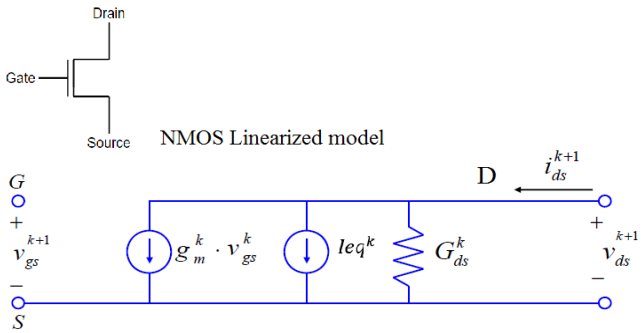


Figure 12: N-R Linearized NMOSFET model

$$i_{sd}^{k+1} = i_{sd}^k + g_m \Delta v_{sg}^k + G_{sd}^k \cdot \Delta v_{sd}^k \qquad \Delta v_{sg}^k = \left(v_{sg}^{k+1} - v_{sg}^k\right)$$

$$Ieq^k = isd^k + gm^k\,(-Vsg^k) + Gsd^k\,(-Vsd^k) \qquad \Delta v_{sd}^k = \left(v_{sd}^{k+1} - v_{sd}^k\right)$$

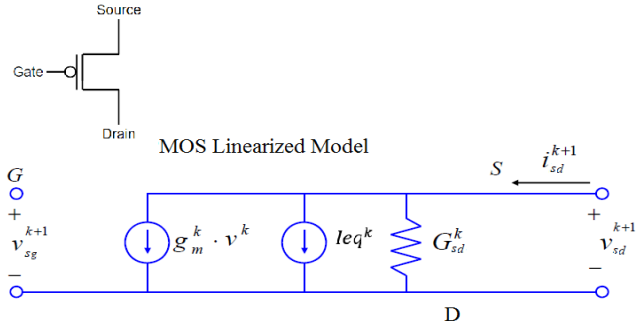


Figure 13: N-R Linearized PMOSFET model

The MOSFET parasitic capacitances were assumed to be linear and included before the Newton Raphson iterations. The formulae of the parasitic capacitances that were included are given below:

Gate – Source capacitance: $Cgs = \frac{1}{2} Cox\, WL$

Gate- Drain capacitance: $Cds = \frac{1}{2} Cox\, WL$

Source/Drain to ground junction capacitance:

$$Cd = Cs = Cjo$$

IV. Experiments and Results

The Transient Circuit Simulator was built using Matlab 2015b (Mathworks, USA). The circuit simulator was tested using the benchmark circuits. The circuit simulator was able to successfully simulate the benchmark circuits (linear and nonlinear benchmark circuits) and produced accurate results. The plots of node voltages and the plot of the branch currents generated from simulating the benchmark circuits are shown in this section.

A. Linear Benchmark Circuits

rc_line

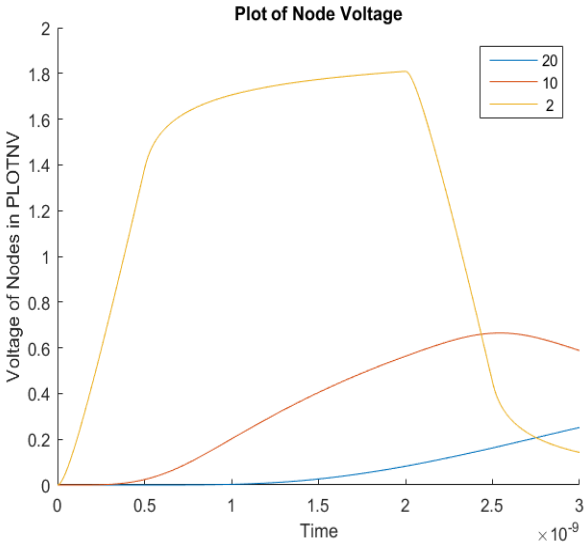


Figure 14: Plot of the results obtained from rc_line.dat

rcmesh20

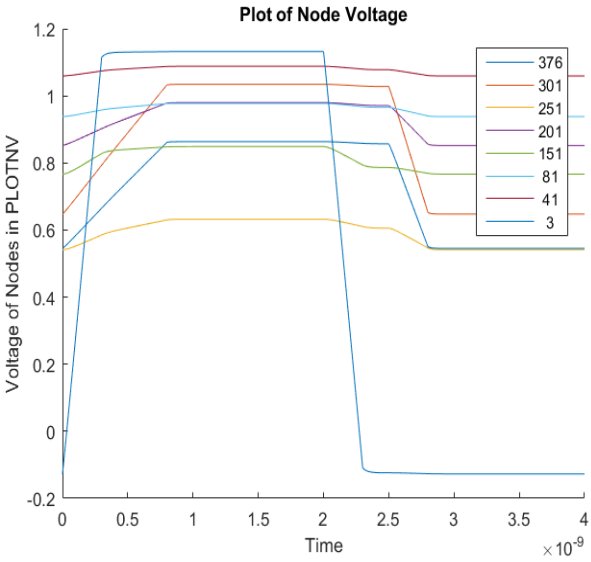


Figure 15: Plot of the results obtained from rcmesh20.dat

rlc_line

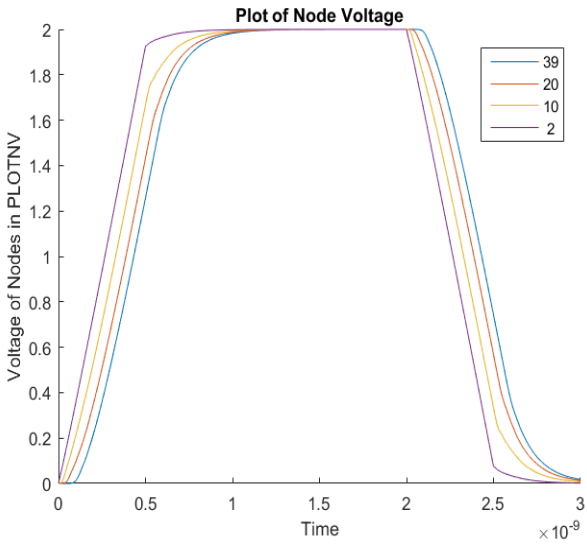


Figure 16: Plot of the results obtained from rlc_line.dat

B. Nonlinear Benchmark Circuits

test_inv

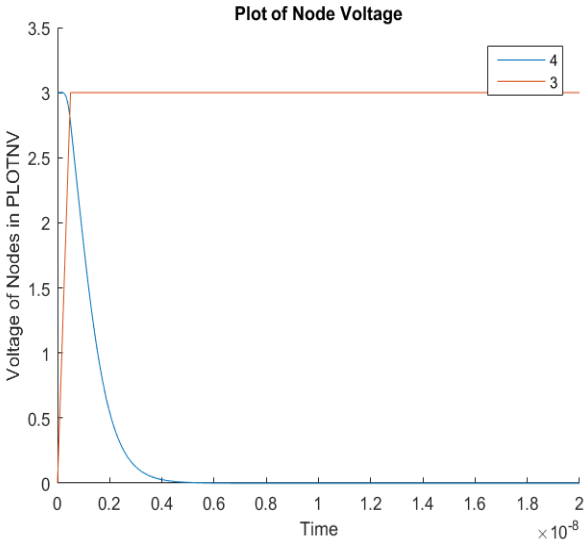


Figure 17: Plot of the results corresponding to the node voltages obtained from test_inv.dat

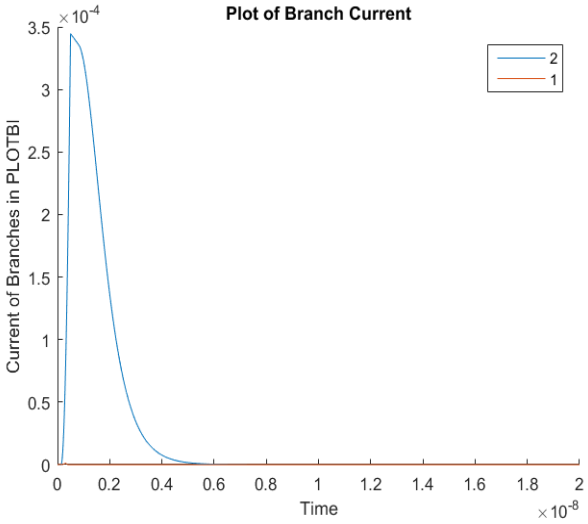


Figure 18: Plot of the results corresponding to the branch currents obtained from test_inv.dat

Transmux

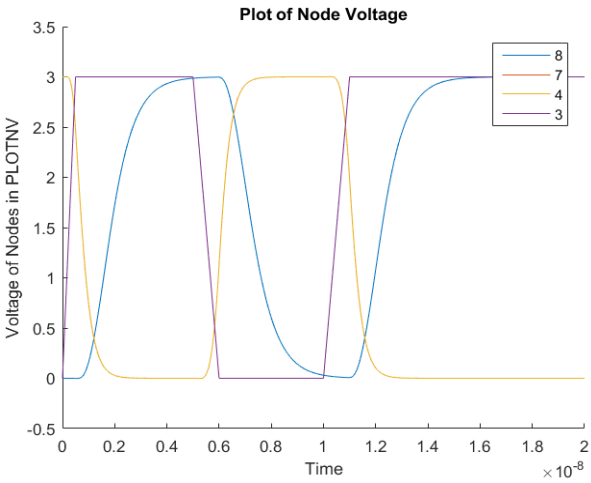


Figure 19: Plot of the results corresponding to the node voltages obtained from transmux.dat

nand3

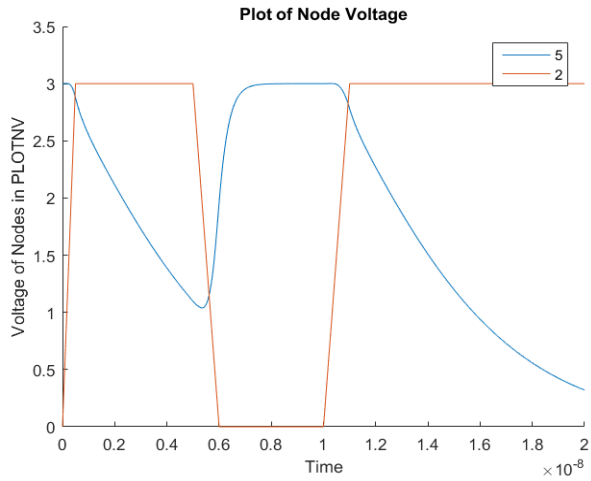


Figure 20: Plot of the results corresponding to the node voltages obtained from nand3.dat

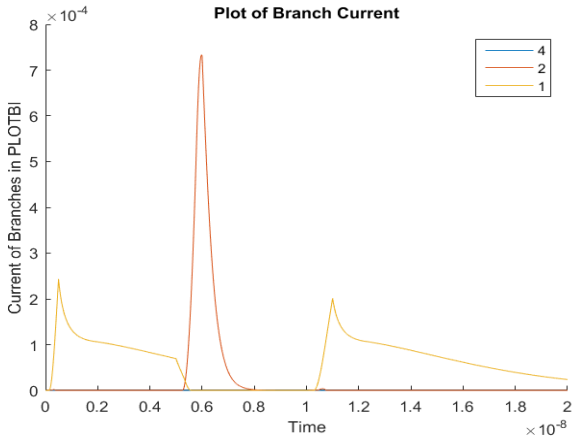


Figure 21: Plot of the results corresponding to the branch currents obtained from nand3.dat

clocktree

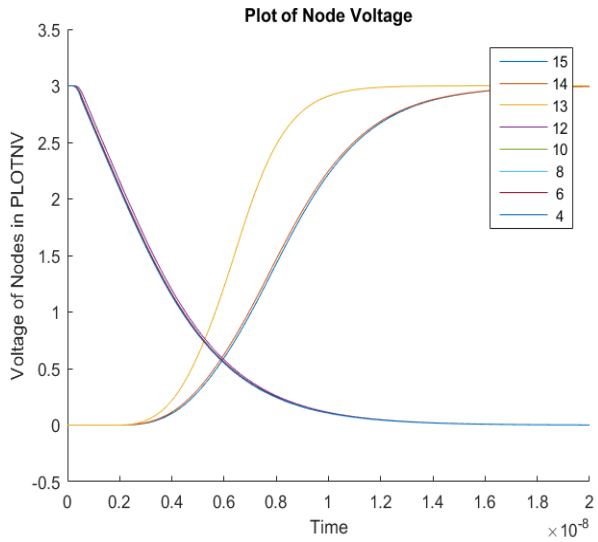


Figure 22: Plot of the results corresponding to the node voltages obtained from clocktree.dat

CONCLUSION

In this project a transient circuit simulator was successfully built using Matlab 2015b. The simulator performs DC and transient analysis on circuits containing linear and nonlinear elements. For linear transient analysis Forward Euler, Backward Euler and Trapezoidal Integration methods were explored. The technique of gmin stepping was applied to obtain the nonlinear DC solution. For nonlinear transient analysis multi-dimensional Newton-Raphson method was implemented. The circuit simulator works effectively with all the benchmark circuits.

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