```
module ALU_tb;
    reg [3:0] A, B;         // Test Inputs
    reg [2:0] Opcode;       // Test Opcode
    wire [3:0] Result;      // Output Result
    wire CarryOut;          // Output CarryOut

    // Instantiate ALU
    ALU uut (
        .A(A),
        .B(B),
        .Opcode(Opcode),
        .Result(Result),
        .CarryOut(CarryOut)
    );

    initial begin
        // Test Addition
        A = 4'b0011; B = 4'b0001; Opcode =
3'b000;
        #10;
        // Test Subtraction
```

```
        A = 4'b0100; B = 4'b0010; Opcode =
3'b001;
        #10;
        // Test AND
        A = 4'b1100; B = 4'b1010; Opcode =
3'b010;
        #10;
        // Test OR
        A = 4'b1100; B = 4'b0011; Opcode =
3'b011;
        #10;
        // Test NOT
        A = 4'b1010; Opcode = 3'b100;
        #10;
        // Finish Simulation
        $finish;
    end

    initial begin
        $monitor("Time=%0d A=%b B=%b
Opcode=%b Result=%b CarryOut=%b",
```

```
                $time, A, B, Opcode, Result,
CarryOut);
    end
endmodule
```