MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : BCAC202 Computer Architecture

UPID : 200052

Time Allotted : 3 Hours *Full Marks : 70*

The Figures in the margin indicate full marks.
Candidate are required to give their answers in their own words as far as practicable

Group-A (Very Short Answer Type Question)

1. Answer any ten of the following : [1 × 10 = 10]

(I) In which one of the following addressing modes is the actual operand provides as a part of the instruction?

1. Direct
2. Immediate
3. Indirect
4. Relative

(II) What is micro-operation?

(III) Convert the infix notation A × B + C × D + E × F into Postfix Notation or Reverse Polish Notation?

(IV) What is the full form of SISD?

(V) Input or output devices that are connected to computer are called _____.

(VI) What is Tag Field?

(VII) Which one of the following most correctly describes the functionality of the control unit in a CPU?

a. To perform arithmetic operations based on decoded program instruction
b. To store program instruction
c. To perform logic operations based on decoded program instruction
d. To generate control signals based on decoded program instruction.

(VIII) What is micro programmed control?

(IX) The electrical circuits/lines that you see on the motherboard that is used to transfer data is known as _____.

(X) What is the Hazard in pipeline?

(XI) The sign magnitude representation of -1 is _____.

(XII) The subtraction result of -7 and 1 in 2's complement form is_____

Group-B (Short Answer Type Question)

Answer any three of the following : [5 x 3 = 15]

2. Multiply (20) AND (-19) Using BOOTH'S Algorithm with register size 6. [5]
3. Derive the control gates associated with program counter PC in the basic computer? [5]
4. Find out the $10^{'s}$ complement of 54670. [5]
5. Draw the typical RAM & ROM chip with proper explanation. [5]
6. Convert binary number 1101010 into hexadecimal number. [5]

Group-C (Long Answer Type Question)

Answer any three of the following : [15 x 3 = 45]

7. Explain Booth's algorithm with the flow chart.
   Multiply (-5) and (4) using booth's algorithm with register size 4. [5+10]
8. Explain stack register.
   Write down the micro-operations for push & pop.
   Explain reverse polish notation with a example. [5+5+5]
9. Explain the rules for converting a decimal number into floating point.
   Explain IEEE 754 format to represent floating point data.
   Convert 39887.5625 to IEEE 32-bit floating point format. [5+5+5]
10. What is rise instruction format?
    Explain different type of addressing modes.
    What is subroutine call. [3+8+4]

11. What is speed up, efficiency, and throughput of a pipeline system? [6+9]
Consider a pipeline having 4 phases with duration 60,50,90 and 80 ns. Given latch delay is 10 ns. Calculate- pipeline cycle time, non-pipeline execution time and speed up ratio.

*** END OF PAPER ***