CS/BCAN/Odd/SEM-1/BCAN-101(New)/2018-19



MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code: BCAN-101

DIGITAL ELECTRONICS

Time Allotted: 3 Hours Full Marks: 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

Group - A (Multiple Choice Type Questions)

Į,	Unoose the	correct and	manye tor	and ten or	me rondwing

1×10=10

http://www.makaut.com

- (i) In a multiplexer, the output depends on its
 - (a) Data inputs

(b) Select inputs

(c) Select outputs

- (d) None of these
- (ii) Which of the following condition is not allowed in SR flip-flop?
 - (a) S=0 R=0

(b) S=0 R=1

(c) S=1 R=0

- (d) S=1 R=1
- (iii) The logical expression Y=A+AB+AB'C+A'BC'D+1 is equivalent to
 - (a) A + C'

(b) 1

(c) A'

(d) A

- (iv) A flip-flop has ______.
 - (a) one stable state

(b) no stable states

(c) two stable states

(d) None of these

8481 Turn Over

CS/BCAN/Odd/SEM-1/BCAN-101(New)/2018-19

(v)	The dual of a Boolean expression is obtained by						
	(a) interchanging all 0s and 1s						
	 (b) interchanging all 0s and 1s, all + and '.' signs (c) interchanging all 0s and 1s, all + and '.' signs and complementing all the variables 						
(d) interchanging all + and '.' signs and complementing all the variables							
(vi)	A + A' B is equal to						
	(a) A+B	(b)	A				
	(c) B	(d)	A'+B				
(vii)	11101+1100 is equal to						
	(a) 10.1101 ·	(b)	100.1101				
	(c) 10.01101 °	(J)	None of these				
(viii)	In general, a sequential logic circuit consists of						
	(a) only flip-flops		only gates				
	(c) flip-flops and combinational logic circuits	(đ)	only combinational logic circuits				
(ix)	Race condition arises in		tie				
	(a) S-R Latch		S-R F/F				
	(c) J-K F/F	(d)	TEF				
(x)	When two n bit binary mumbers are added, the sum will contain at most						
	(a) n bits	(b)	n+1 bits				
	(c) n+2 bits	(d)	n+n bits				
(xi)	While performing BCD addition, if the value of each 4-bit group becomes with that group						
	(a) greuter than 9	(b)	greater or equal to 9				
	(c) greater than 6						
	Group - B						
	(Short Answer Type		ions)				
	Answer mo three of th		i e	5×3=1			

- Difference between Synchronous and Asynchronous counters.
- 3. Simplify the expressions:

(i) A = XYZ + XY'Z + XD'

(ii) B = P + P'Q + P'Q'R + P'Q'R'S

2+3=5

http://www.makaut.com

http://www.makaut.com

CS/BCAN/Odd/SEM-1/BCAN-101(New)/2018-19

4. Subtract (-33) from (-57) using 2's complement method.

Convert (4536)₁₀ to

- (i) 2421 code
- (ii) 5421 code

3+2=5

- Draw the truth table and logic circuit of a full-subtractor. Using K-map find out the expression for difference (D) and borrow (B).
- 6. What is flip-flop? What is race condition?

1+4=5

Group - C

(Long Answer Type Questions)

Answer any three of the following.

15×3=45

7. (a) Using K-map method minimize the following expression:

$$F(w,x,y,x) = m\Sigma(1,5,6,12,13,14) + d\Sigma(2,4).$$

Implement the logic circuit using NAND gates only.

- (b) Implement Ex-OR gate using NAND Gate and NAND gate using NOR gate. (5+4)+(3+3)=15
- 8. (a) Define excitation table of flip-flop and propagation delay.
 - (b) Using the logic diagram convert a J-K flip-flop D flip-flop and T flip-flop.
 - (c) Design a J-K master-slave flip flop with circuit diagram and give the truth table. 5+5+5=15
- 9. (a) Write down the simplified Boolean expression in
 - (i) sum of product form and
 - (ii) product of sum form for

 $Y(A,B,C,D)=\Pi M(0,1,3,5,6,7,9,10,11,12,13,15)$

(b) Implement a full adder using 2 half adders.

(4+4)+7=15

- 10. (a) Design a curry look ahead adder. http://www.makaut.com
 - (b) Design a combinational logic circuit to implement 4-bit odd parity checker.

9+6=15

11. Write short notes on any three of the following:

5x3=15

(i) PIPO

http://www.makaut.com

- (ii) Ripple Counter
- (iii) 4-bit parallel adder
- (iv) Gray Code
- (v) Master slave J-K flip-flop

http://www.makaut.com Whatsapp @ 9300930012 Your old paper & get 10/-पुराने पेपर्स भेजे और 10 रूपये पार्ये, Paytm or Google Pay से

3