- MAY 2019

Total No. of Questions—8] [Total No. of Printed Pages—2

Seat No.	

[5559]-193

S.E. (Computer) (Second Semester) EXAMINATION, 2019

MICROPROCESSOR

(2015 PATTERN)

Time : 2 Hours **Maximum Marks : 50**

Instructions to the candidates:

i. Answer Question No. 1 OR 2, 3 OR 4, 5 OR 6 and 7 OR 8.

ii. Neat diagram must be drawn whenever necessary.

iii. Figures to the right indicate full marks.

iv. Assume suitable data, if necessary.

1) a) List fundamental data types of 80386. [02]

b) Describe following different flags defined in 80386 Processor - [04]
a) DF b) VM c) NT d) RF

c) Explain shift and rotate instructions of 80386. [06]

OR

2) a) Draw and explain the format of a selector. [02]

b) List and explain control registers of 80386. [04]

c) With help of diagram explain the 80386 mechanism to translate logical address to linear address. [06]

3) a) List aspects of protection related to pages. [02]

b) With appropriate diagram explain the concept of privilege levels in 80386. [04]

c) How Call gate descriptor is used to locate the procedure in another code segment? How protection is provided? [06]

OR

4) a) Define "Faults". [02]

b) Explain "How 80386 indentifies interrupts?" [04]

c) By which two ways, 80386 allows input/output to be performed? Explain each in details. [06]

P.T.O.

5) a) Explain features of "Virtual 8086 mode". [03]

b) Explain 80386 processor state after RESET. [04]

c) What all initializations required to start processor in protected mode after reset? [06]

OR

6) a) Write a short note on "Switching to protected mode". [02]

b) List the features of 80386 architecture that supports debugging. [05]

c) With the necessary diagrams explain entering and leaving V86 mode? [06]

7) a) Draw and explain read cycle with non-pipelined address timing. [08]

b) Which data types are supported by 80387? [05]

OR

8) a) Draw and explain write cycle with pipelined address timing. [08]

b) The 80387 instructions are divided in to which functional groups? Explain with one example of each. [05]