PIMPRI CHINCHWAD COLLEGE OF ENGINEERING
DEPARTMENT OF COMPUTER ENGINEERING

Academic Year 2017-18 Semester – I

Class : SE **Subject: Computer Organization and Architecture**

Sr. No.	Topic	Book	Book-wise detailed points
	CO, PO, PEO, mapping, Course Introduction		
1	**Unit I- Computer Evolution and Performance:** Computer Organization and Architecture, Structure and Function	T1	Chapter 1 Introduction 1.1Organization and Architecture 1.2Structure and Function 10
2	**Evolution** (a brief history) of computers, Designing for Performance, Evolution of Intel processor architecture- 4 bit to 64 bit, performance assessment.	T1	Chapter 2 Computer Evolution and Performance 2.1A Brief History of Computers 2.2Designing for Performance 2.3The Evolution of the Intel x86 Architecture 2.5Performance Assessment
3	**A top level view of Computer function and interconnection**- Computer Components, Computer Function, Interconnection structure, bus interconnection	T1	Chapter 3 A Top-Level View of Computer Function and Interconnection 65 3.1Computer Components 3.2Computer Function 3.3Interconnection Structures 3.4Bus Interconnection
4	**Computer Arithmetic-** The Arithmetic and Logic Unit, addition and subtraction of signed numbers	T1 T2	(T1)Chapter 9 Computer Arithmetic 9.1The Arithmetic and Logic Unit (ALU) (T2)Chapter 6 Arithmetic 6.1 Addition and Subtraction of Signed Numbers
5	design of adder and fast adder, carry look ahead addition	**T2**	(T2)Chapter 6 Arithmetic 6.2 Design of Fast Adders
6	multiplication of positive numbers, signed operand multiplication, booths algorithm	T2	(T2)Chapter 6 Arithmetic 6.3 Multiplication of Positive Numbers 6.4 Signed operand multiplication
7	fast multiplication, integer division	T2	(T2)Chapter 6 Arithmetic 6.5 Fast Multiplication 6.6 Integer Division
8	Floating point representation and operations – IEEE standard, arithmetic operations, guard bits and truncation	T2	(T2)Chapter 6 Arithmetic 6.7Floating-Point Numbers and Operations
9	**Unit II - Computer Memory System :** Characteristics of memory system, The memory hierarchy	T1	Chapter 4 Cache Memory 4.1Computer Memory System Overview
10	Cache Memory- Cache memory principles	T1	4.2 Cache Memory Principles
11	Elements of cache design- cache address, size, mapping functions	T1	4.3 Elements of Cache Design
12	replacement algorithms, write policy, line size		
13	number of cache, one level and two level cache, performance characteristics of two level cache- locality & operations		
14	Case Study- PentiumIV cache organization	T1	4.4 Pentium 4 Cache Organization
15	**Internal Memory**- semiconductor main memory, advanced DRAM organization	T1	Chapter 5 Internal Memory Technology 5.1Semiconductor Main Memory 5.3Advanced DRAM Organization
16	**External Memory**- Hard Disk organization, RAID- level 1 to level 6	T1	Chapter 6 External Memory 6.2RAID

17	**Unit III - Input and Output System:** External devices, I/O modules- Module function and I/O module structure	T1	Chapter 7 Input/Output 7.1External Devices 7.2I/O Modules
18	Programmed I/O- overview, I/O commands, I/O instructions, Interrupt driven I/O- interrupt processing, design issues	T1	7.3 Programmed I/O 7.4Interrupt-Driven I/O
19	Case Study- Study of Programmable Interrupt Controller Intel 82C59A in brief		
20	Direct Memory Access- drawbacks of programmed and interrupt driven I/O, DMA functions	T1	7.5 Direct Memory Access
21	Case Study- DMA Controller Intel 8237A-study in brief		
22	I/O channels and processors- evolution and characteristics	T1	7.6 I/O Channels and Processors
23	The external Interface- Thunderbolt and Infinite Band	T1	7.7 The External Interface: FireWire and Infiniband
24	**Unit IV - Instruction Sets: Characteristics and Functions-** machine instruction characteristics	T1	Chapter 10 Instruction Sets: Characteristics and Functions 10.1Machine Instruction Characteristics
25	types of operands, Case Study-Intel 8086	T1	10.2 Types of Operands 10.3Intel x86 and ARM Data Types
26	Types of operations- data transfer, arithmetic	T1	10.4 Types of Operations
27	logical, conversion, input-output, system control, and transfer of control		
28	Case Study-Intel 8086 operation types	T1	10.5 Intel x86 and ARM Operation Types
29	Addressing modes and Formats- Addressing modes- immediate, direct, indirect, register, register indirect, displacement and stack	T1	Chapter 11 Instruction Sets: Addressing Modes and Formats 11.1Addressing
30	Case Study-8086 addressing modes	T1	11.2x86 and ARM Addressing Modes
31	Instruction Formats- instruction length, allocation of bits, variable length instructions. Case Study- 8086 instruction formats	T1	11.3 Instruction Formats 11.4x86 and ARM Instruction Formats
32	**Unit V - Processor Organization:** Processor organization, Register organization- user visible registers, control and status registers	T1	Chapter 12 Processor Structure and Function 12.1Processor Organization 12.2Register Organization
33	Case Study- register organization of microprocessor 8086		
34	Instruction Cycle- The machine cycle and Data flow	T1	12.3 The Instruction Cycle
35	Instruction Pipelining- Pipelining Strategy, pipeline performance, pipeline hazards, dealing with branches	T1	12.4 Instruction Pipelining
36	Case Study- pipelining in Pentium		
37	**Instruction level parallelism and superscalar processors**- Super scalar verses super pipelined, constraints	T1	Chapter 14 Instruction-Level Parallelism and Superscalar Processors 14.1Overview

38	Design Issues- instruction level and machine parallelism, Instruction issue policy, register renaming, machine parallelism, branch	T1	14.2 Design Issues
39	Case study- Pentium IV.	T1	14.3 Pentium 4
40	**Unit VI - Basic Processing Unit:** Fundamental Concepts- register transfer, performing arithmetic or logic operations	T2	Chapter 7 Basic Processing Unit 7.1Some Fundamental Concepts
41	fetching a word from memory, storing a word in memory	T2	
42	Execution of a complete instruction- branch instructions	T2	7.2 Execution of a complete instruction
43	Hardwired control	T2	7.4 Hardwired control
44	Micro-programmed control- micro instructions, micro program sequencing, field	T2	7.5 Micro-programmed control
45	wide branch addressing, microinstruction with next address, pre-fetching microinstructions and emulation.	T2	

Text: 1. W. Stallings, —Computer Organization and Architecture: Designing for performance‖,Pearson Education/ Prentice Hall of India, 2003, ISBN 978-93-325-1870-4, 7 th Edition.

2. Zaky S, Hamacher, —Computer Organization‖, 5 th Edition, McGraw-Hill Publications,2001, ISBN- 978-1-25-900537-5, 5 th Edition.