Seat
No.

[4657]-579

S.E. (Computer Engineering) (Second Semester)

EXAMINATION, 2014

COMPUTER ORGANIZATION

(2012 PATTERN)

Time : Two Hours　　　　　　　　　Maximum Marks : 50

N.B. :— (*i*) Answer Q. **1** or Q. **2**, Q. **3** or Q. **4**, Q. **5** or Q. **6** and

Q. **7** or Q. **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right indicate full marks.

(*iv*) Use of calculator is allowed.

(*v*) Assume suitable data, if necessary.

1. (*a*) Draw and explain Von Neumann architecture. [6]

(*b*) Explain basic SOC (System on Chip) processor

architecture. [6]

P.T.O.

2. (*a*) Describe the features of RISC and CICS processors. [6]

(*b*) Multiply the following numbers using Booth's algorithm :

Multiplicand = +13

Multiplier = −6 (Show steps in detail). [6]

3. (*a*) Explain hardware organization and execution of 4 stage instruction pipeline. [6]

(*b*) State Microinstructions for Add (Rsrc)+, Rdst. [6]

Or

4. (*a*) Explain with example the steps involved in floating point addition and multiplication. [6]

(*b*) Compare hardwired and micro programmed control unit. [6]

5. (*a*) Compare memory mapped I/O with I/O mapped I/O. [6]

(*b*) Explain how data transfer takes place by USB. [7]

Or

6. (*a*) Compare NUMA and UMA multiprocessors. [6]

(*b*) Explain how data transfer takes place by SCSI Bus. [7]

7. (*a*) Draw the block diagram of AMD multicore opteron. [6]

(*b*) Draw NVDIA GPU architecture. [7]

Or

8. Explain with diagram Intel IA-64 architecture. [13]