# Final Technical Report: Atmospheric Energy Harvester Concept & Circuit Modeling

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## Abstract

This report presents the conceptual design, modeling, and preliminary simulation work for a hybrid atmospheric energy harvester. The device aims to capture weak electric currents from the atmosphere—through a resonant electrode structure—and convert them via a low-noise transimpedance amplifier into stored energy for ultra-low-power devices. We discuss the architecture, SPICE pseudo-models, circuit nets, simulation expectations, risks, and recommendations for future prototyping.

**Keywords:** atmospheric energy harvesting, transimpedance amplifier, SPICE modeling, low input current, electrode design

## Table of Contents

# 1. Introduction & Objectives

We explored a device that passively harvests the Earth-atmospheric electric potential through a resonant electrode structure to generate micro- or nano-level energy. This report documents:

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- The theory grounding the concept
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- Circuit architecture and amplifier design
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- Pseudo-SPICE modeling for LMC6001 with experimental parameter estimates
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- Simulation templates (netlists) and directive settings
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- Performance expectations and bottleneck analysis
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- Recommendations for the next phases of prototype development

# 2. Technical Background & Reference Data

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- **LMC6001 Amplifier**: According to its datasheet, the input bias current is up to ~ 25 fA at 25 °C; under adverse conditions can increase toward ~ 2 pA.
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- Noise, offset, and drift features from the datasheet inform the model's parameters.

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- Atmospheric electric fields are often ~100 V/m under calm conditions; air conductivity is extremely low, meaning harvested currents over electrode areas of ~1 $m^2$ are on the order of pico- to nanoamperes.

# 3. System Architecture and Circuit Topology

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- The core signal path: **Electrode → TIA (inverting input) → feedback network → output → rectifier / storage**

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- A **Transimpedance Amplifier (TIA)** is chosen to convert minute currents to measurable voltages, using RfR_fRf (feedback resistor) and CfC_fCf (compensation capacitor).

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- To suppress leakage, **guard rings / driven shields** surround high-impedance lines and connections.

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- The design anticipates integration of a rectification stage, storage (supercapacitors / battery), and protection circuits.

# 4. Pseudo-SPICE Models and Netlist Templates

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- We defined a .SUBCKT model for LMC6001 with example parameters:
  • Input bias currents ~10–25 fA
  • Offset voltage ~1 μV
  • Nonlinear leakage controlled in the model
  • Gain stage with amplification factor ~1×$10^6$
  • Output stage with approximate output resistance

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- Netlist template ensures that the TIA stage, current source, feedback elements, and amplifier subcircuit can be simulated together.

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- SPICE options such as abstol, gmin, and reltol configured for low-current regimes to avoid internal numeric shunting.

## 5. Simulation Expectations and Estimates

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- With a source current of ~10 pA and Rf=1 GΩR_f = 1\,\text{G}\OmegaRf=1GΩ, the output voltage could reach tens of millivolts (in ideal conditions).
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- At lower current levels (femto- to picoampere range), signal is extremely vulnerable to noise, offset drift, and leakage.
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- Parasitic elements (PCB leakage, stray capacitances, amplifier input leakage) will significantly reduce effective signal.
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- Reaching milliwatt power levels demands extraordinary enhancements: vast electrode area, ultra-low loss circuitry, extremely low noise design, and perhaps active gain stages.

## 6. Risks, Limitations, and Critical Factors

| Factor | Importance | Mitigation Strategy |
|---|---|---|
| Surface leakage and parasitics | Even tiny leakage paths can nullify signal | Guard rings, clean surfaces, ultra-high |

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|---|---|---|
| | | insulation |
| Amplifier noise & offset | At very low currents, noise may dominate | Select ultra-low noise devices, filtering, calibration |
| Stability / oscillation | High gain + reactive components can cause instability | Proper compensation (choose CfC_fCf carefully), phase margin checks |
| Parasitic capacitance / inductance | Distorts signal coupling and limits bandwidt | Careful layout, shielding, minimal trace lengths |

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| Scale requirement | Power output often extremely low | Larger electrodes, field enhancement, better materials |

## 7. Recommendations & Roadmap

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2. **Run simulations** using the provided netlist / model, sweeping source current, feedback parameters, leakage values to analyze sensitivity.

3.

4. **Build a physical prototype** of the TIA stage with guard ring, high-precision components, and shielding; measure input currents, output, offset, noise.

5.

6. **Calibrate the model** using real experimental results— adjust leakage, offset, gain, parasitic parameters.

7.

8. Add **parasitic elements** into simulation: electrode capacitance, PCB leakage, stray coupling.

9.

10. Explore electrode materials (e.g. graphene + Au coatings, nanostructures) to maximize harvesting efficacy.

11.

12. Optimize compensation networks (CfC_fCf), stability margins, possibly multi-stage amplification.

13.

14. Gradually **scale up** electrode area, integrate protective measures, and test in real atmospheric conditions.

# 8. References


1.

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# 9. Appendices

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- Appendix A: Netlist template
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- Appendix B: Pseudo-SUBCKT model code
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- Appendix C: Parameter definitions and units
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- Appendix D: Additional simulation configuration notes