# Swagat Bhattacharyya

[PHONE] | [ADDRESS] | [EMAIL]

## SUMMARY

With a strong foundation in electrical engineering, applied physics, and mathematics, my research portfolio spans neuromorphic systems, mixed-signal design, and signal processing. My master's work at Georgia Tech focused on developing neuromorphic approaches for asynchronous computing, culminating in multiple tapeouts across several tech nodes and the innovative circuits such as chaotic neurons and analog sorting circuits. My industrial experience, including roles at Renesas and Neurava, has honed my entrepreneurial skills and expertise in robust embedded systems development, translating into impactful products, like wearable seizure sensors.

## EDUCATION

**Georgia Institute of Technology** — Atlanta, GA | July 2024
Master of Science in Electrical Engineering | *Advisor: Prof. Jennifer O. Hasler* — **GPA: 3.90**
*Thesis: Neuromorphic Approaches for Asynchronous Computing and Sensing*

**Purdue University, Honors College** — West Lafayette, IN | May 2022
Triple Major: *BS Electrical Engineering, BS Applied Physics, & BS Mathematics* — **GPA: 3.96** (Highest Distinction)

## ACADEMIC RESEARCH EXPERIENCE [KEY: ● => Hardware | ○ => Software]

**NSF Graduate Research Fellow,** Integrated Computational Electronics Lab, *Georgia Tech* *Aug. 2022 – July 2024*

- Designed, laid out, and **taped out *three chips*** using floating-gate (FG) FETs in *28 nm*, *180 nm*, and *350 nm* CMOS; Ensured robust performance of the following **analog standard cells** across process nodes: 6-bit DAC, FG-based mixer, FG bootstrap source, I&F neurons, strongARM latch, and high-voltage decoders for FG programming.
- Successfully experimentally demonstrated signal conditioning circuits using glass-transferred RRAM devices.
- **Characterized cryogenic FG FETs** and developed robust FG FET programming methods in *65 nm* CMOS.
- Led a team demonstrating the first **analog sorting algorithm** (award-winning talk at IEEE ICRC 2023).
- Developed a **nonuniform ADC** leveraging extrema sampling for data reduction given a non-stationary input.
- Invented and demonstrated the simplest non-driven **chaotic CMOS oscillator** (a 6T FG-based I&F neuron).
- Led a team developing the first efficient C, Matlab, &Python models of transistor-based HH neuron networks.
- Led a team developing a fast simulation suite in Python for large-scale **analog architectural exploration**.

**Undergraduate Researcher,** Center for Implantable Devices, *Purdue University* *Jan. 2021 – May 2021*

- Designed, simulated, and characterized a high-order filter for a novel implantable gastric monitoring sensor.

**Undergraduate Researcher,** Computational Electronic Systems Lab, *West Virginia Univ.* *June 2014 – June 2022*

- Developed a quadrature, **OTA-C sine VCO** with the widest reported tuning range via a novel **envelope detector**.
- Designed a low-power in-sole **gait analyzer** to study the progression of Parkinson's Disease in a nonclinical setting.
- Developed **analog ML** algorithms to train an acoustic vehicle classifier on a field-programmable analog array.
- Developed **mixed-integer nonlinear programming algorithms** to optimize starved logic gate and ADC topologies.

## INDUSTRIAL EXPERIENCE [KEY: ●=> Hardware | ○=> Software | ❖ => Business Development]

**Field Applications Engineer,** Renesas Electronics America, *(Raleigh, NC & Boston, MA)* *Aug. 2024 – Current*

- Developed a broad range of skills in hardware, software, and sales for supporting existing Renesas customers and engaging new customers across Renesas's embedded processing, wireless connectivity, & mixed-signal portfolios.

**Embedded Design Engineer,** Lune Systems, *Atlanta, GA* *Oct. 2023 – Aug. 2024*

- Led **PCB design &testing** of a cost-effective smart insomnia aid, focused on optimal, user-centric performance.
- Conducted in-depth customer discovery to define **product specifications** as tailored to market needs &trends.
- Engineered robust embedded firmware to enhance the performance and the user interface of the aid.
- ❖ Played a pivotal role in securing $20K in seed funding by articulating the value proposition of the sleep aid.

**Hardware Design Engineer,** Neurava LLC, *West Lafayette, IN* *May 2021 – July 2022*

- Led a team of five in creating a **seizure sensor array (SSA)** for SUDEP-risk patients from concept through initial clinical trials overseeing: biomarker&sensor selection; data pipeline; PCB design, layout, fabrication, &testing.
- ❖ Conducted the initial patent search and cowrote the **patent** application for the multi-modal SSA. The SSA, which has undergone clinical testing since 2022, achieved the **lowest-known false positive rate** in the industry while maintaining state-of-the-art sensitivity, directly contributing towards securing **$3M** in seed funding for Neurava LLC.
- Developed embedded SSA firmware (DSP &controls) for real-time, low-power **mixed-signal edge computing**.
- Proposed, developed, &implemented **automated characterization protocols** to ensure SSA *reliability*.

## PATENTS / JOURNALS / CONFERENCES / POSTERS (Google Scholar: https://tinyurl.com/yc66j52v)

| | | |
|---|---|---|
| **Patents** | 1 | Irazoqui P, Shah J, Meyer T, Ganesh V, **Bhattacharyya S**, & Hsiung Y, "Multimodal Seizure Sensing," Published Nov 2023 |
| **Journals** | 1 | Mathews P, Ayyappan PR, Ige A, ***Bhattacharyya S***, Yang L, &Hasler J, "A 65 nm CMOS Analog Programmable Standard Cell Library for Mixed-Signal Computing," IEEE Transactions on VLSI Syst., vol 32, no 10, Oct 2024 |
| | 2 | ***Bhattacharyya S*** & Hasler J, "Extrema-Triggered Conversion for Non-Stationary Signal Acquisition in Wireless Sensor Nodes," JLPEA, vol 14, no 1, Feb 2024 |
| | 3 | ***Bhattacharyya S***, Ayyappan PR, & Hasler J, "Towards Scalable Digital Modeling of Networks of Biorealistic Silicon Neurons," IEEE Journal on Emerging and Selected Topics in CAS, vol 13, no 4, pp 927-939, Dec 2023 |
| | 4 | ***Bhattacharyya S*** & Graham DW, "Amplitude-Regulated Quadrature Sine-VCO Employing an OTA-C Topology," IEEE Transactions on CAS II: Express Briefs, vol 70, no 6, pp 1886-1890, June 2023 |
| | 5 | ***Bhattacharyya S***, Andryzcik S, & Graham DW, "An Acoustic Vehicle Detector & Classifier Using a Reconfigurable Analog/Mixed-Signal Platform," JLPEA, vol 10, no 1, Article 6, March-April, 2020 |
| **Confer-ences** (Oral Talks) | 1 | Mathews P, Ayyappan PR, Ige A, ***Bhattacharyya S***, Yang L, & Hasler J, "A 65nm and 130nm CMOS program-mable analog standard cell library for scalable system synthesis," IEEE CICC, Denver, CO, Apr 21-24, 2024 |
| | 2 | ***Bhattacharyya S***, Yang L, & Hasler J, "BuzzSort: A Linear-Time, Event-Driven Data Conversion and Sorting Framework for Approximate Computing Architectures," IEEE ICRC, San Diego, CA, Dec 5-6, 2023 |
| | 3 | ***Bhattacharyya S*** & Hasler J, "Extrema-Triggered Analog-Digital Conversion for Low-Power Wireless Sensor Nodes," IEEE MWSCAS, Tempe, AZ, Aug 6-9, 2023 |
| | 4 | ***Bhattacharyya S***, Mathews P, Ayyappan PR, & Hasler J, "Toward Biorealistic Silicon Neural Circuits on Reconfigurable Platforms," IEEE MWSCAS, Tempe, AZ, Aug 6-9, 2023 |
| **Posters** | 1 | Hasler J, **Bhattacharya S**, Baer S, "Dynamical Analysis of Transistor-Based Hodgkin-Huxley Neuron Circuit Models," Society for Neuroscience Conference, Chicago, IL, Oct 5-9, 2024 |
| | 2 | Meyer T, **Bhattacharya S**, Lehman P, Ganesh V, Ta J, Lowen K, Dragon D, Sainju R, Gehlbach B, Shah J, Nobis W, & Richerson G, "A Novel Multi-Modal Arm Wearable for Seizure Detection," AES Conf., Orlando, FL, Dec 1-5, 2023 |
| | 3 | **Bhattacharya S**, Graham D, and Hasler J, "Amplitude Regulation of an OTA-C Sine VCO," IEEE MWSCAS, Tempe, AZ, Aug 6-9, 2023 |
| | 4 | Rumple M, **Bhattacharyya S**, Hagedorn I, and Ghera Z, "RevEx: Low-Power, Nonoptical VR Limb Tracking with Eddy-Current Haptics," Purdue Spark Challenge, West Lafayette, IN, Dec 10, 2020 |
| | 5 | Prakash M, Szadowski H, Thompson M, Dextre A, Chan M, Lee J, **Bhattacharyya S**, Ravichandran K, Saylor D, &Howard B, "Microfluidic Argonaute Mediated COVID-19 Diagnostic Device," Fall Research Expo, West Lafayette, IN, Nov 16-20, 2020 |
| | 6 | **Bhattacharyya S**, Andryzcik S, Dilello A, Baker J, and Graham DW, "Low-Power Gait Analyzer to Aid Parkinson's Disease Diagnosis," SURE Symposium, Morgantown, WV, July 25, 2019 |
| | 7 | **Bhattacharyya S**, "DIMOS: A Low-Power, Fast Response Logic Gate Architecture," Intel ISEF 2018, Pittsburgh, PA, May 13-18, 2018 |

## HONORS & AWARDS (Selected)

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|---|---|
| IEEE International Conference on Rebooting Computing (ICRC) Best Short Paper Award | 2023 |
| **National Science Foundation Graduate Research Fellowship** (nationwide acceptance rate: 16%) | 2022 |
| Georgia Institute of Technology Presidential Fellowship (Georgia Tech's most prestigious graduate fellowship) | 2022 |
| Purdue Mathematics Department Gordon L. Walker Scholarship | 2021 |
| Purdue Physics and Astronomy Department Scholarship | 2021 |
| 2nd place in the Purdue School of ECE Spark Challenge (senior design showcase) | 2021 |
| 1st place in the Purdue Japanese Student Association Japanese Speech and Skit Competition (1st year) | 2019 |
| Purdue Trustees Scholarship | 2018 |
| 2nd place in Embedded Systems and 1st place NSA Research Directorate Award in Computing at Intel ISEF – honored with a minor planet in my name: 34619 Swagat | 2018 |
| Selected as one of two WV delegates to the 2018 National Youth Science Camp | 2018 |

## LEADERSHIP EXPERIENCE

*President*, Purdue IEEE Student Branch — 2020-21

- Oversaw operations and bylaw compliance of 11 committees with ~200 members in total.
- Spearheaded outreach events & initiated several intra- and inter-student branch collabs.

*Vice President*, Purdue IEEE Student Branch — 2019-20

- Oversaw operations of six technical committees, managed shared resources, improved workspace safety and compliance with protocol, & resolved inter-committee conflicts.

*Electrical Design & Fabrication Lead*, Purdue IEEE Engineering in Medicine & Biology Society — 2019-20, 21-22

- Taught 20 team members skills to design, prototype, and fabricate circuits during my tenure.
- Designed and constructed a navigational aid for the visually impaired.
- Designed and constructed the electronic controls systems for an exoskeletal assistive arm.

## OTHER SERVICE (Selected)

*I. Peer Review*

| Journal Name | Number of Reviews |
|---|---|
| IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS) | 1 |
| IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) | 2 |
| IEEE Midwest Symposium on Circuits and Systems (MWSCAS) | 2 |

*II. Volunteer Tutoring*

StudentU | Durham, NC — Sep-Dec, 2024

- Tutored highschoolers from marginalized minority communities in Durham, NC for 2 hours per week in math and chemistry, fostering a supportive environment for learning.

*III. Community Outreach (Selected)*

Electrical Engineering Outreach Seminar — Apr. 13, 2021

- Organized & hosted a seminar with NSBE where IEEE gave an overview of an education and career in electrical engineering to Black high schoolers; Created an interactive demo.

Halloween Toy Workshop — Oct. 20, 2020

- Proposed, coordinated, & executed a workshop where Purdue IEEE built toys proposed by elementary school children from rural Boswell, IN to demonstrate the engineering process.

## HARDWARE SKILLS

- Mixed-Signal Design & Layout (28 nm, 180 nm, 350 nm)
- EEPROM (FG) Design, Programming, & Characterization
- Automated Test &Measurement (Analog Post-Si Verification)
- PCB Schematic Design and Layout (IPC Class II)
- FPGA | Signal Proc. | Semiconductors | Circuit Macromodels

## SOFTWARE SKILLS

- Cadence Virtuoso
- Cadence Spectre & Spice
- Matlab, Python, &C (Console&Ebed)
- Altium Designer & KiCad
- Linux Environments

## MISCELLANEOUS

**Languages:** English (Native), Bengali (Native), Hindi (Advanced), Japanese (Basic), German (Basic)
**Music:** Hindustani Classical Vocal Music, Violin, Bamboo Flute
**Sports:** Taekwondo (2nd degree Black Belt), Running, Tennis, Soccer