Lab 10: Electronic Photo Album

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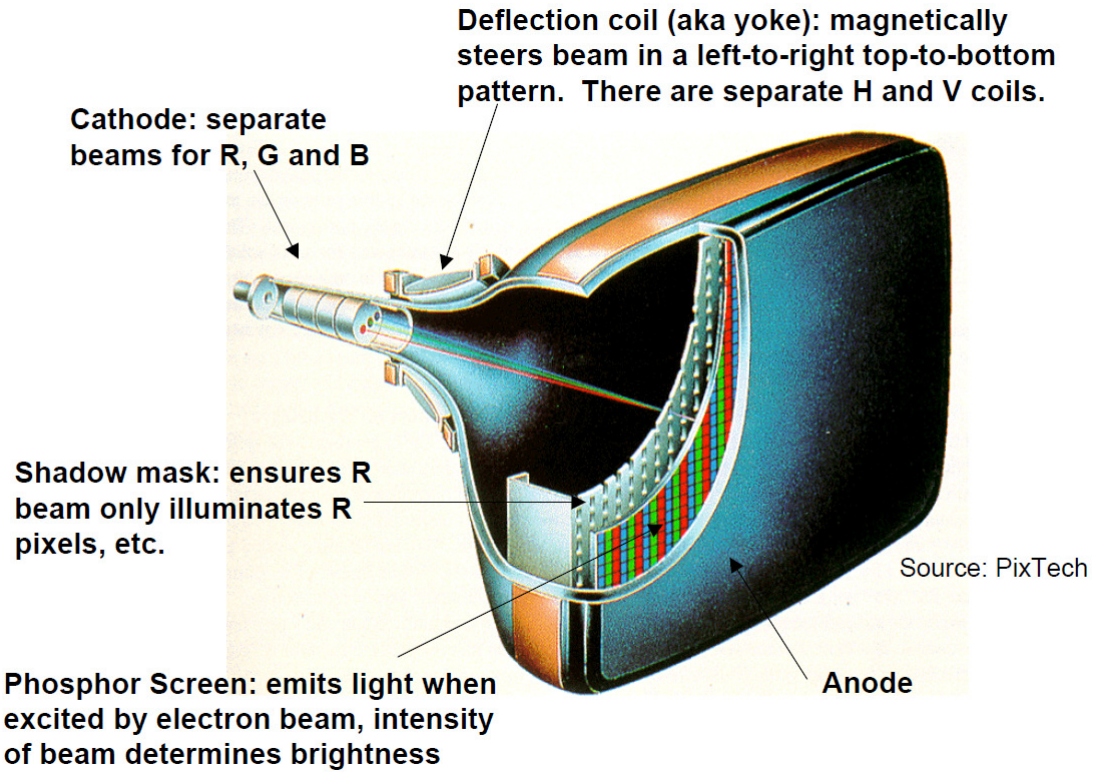
Lab 10: Electronic Photo Album

- In this lab, you will implement an electronic photo album that reads pictures from the SD card and display the photo on LCD screen through the VGA interface
  - User use the WEST/EAST buttons to browse through all the photos on the SD card
  - WEST button select the previous photo, EAST select the next photo
  - If the user reaches the last photo, the system goes back to show the first photo
- You will demo the design to your TA during the lab hours on 12/28

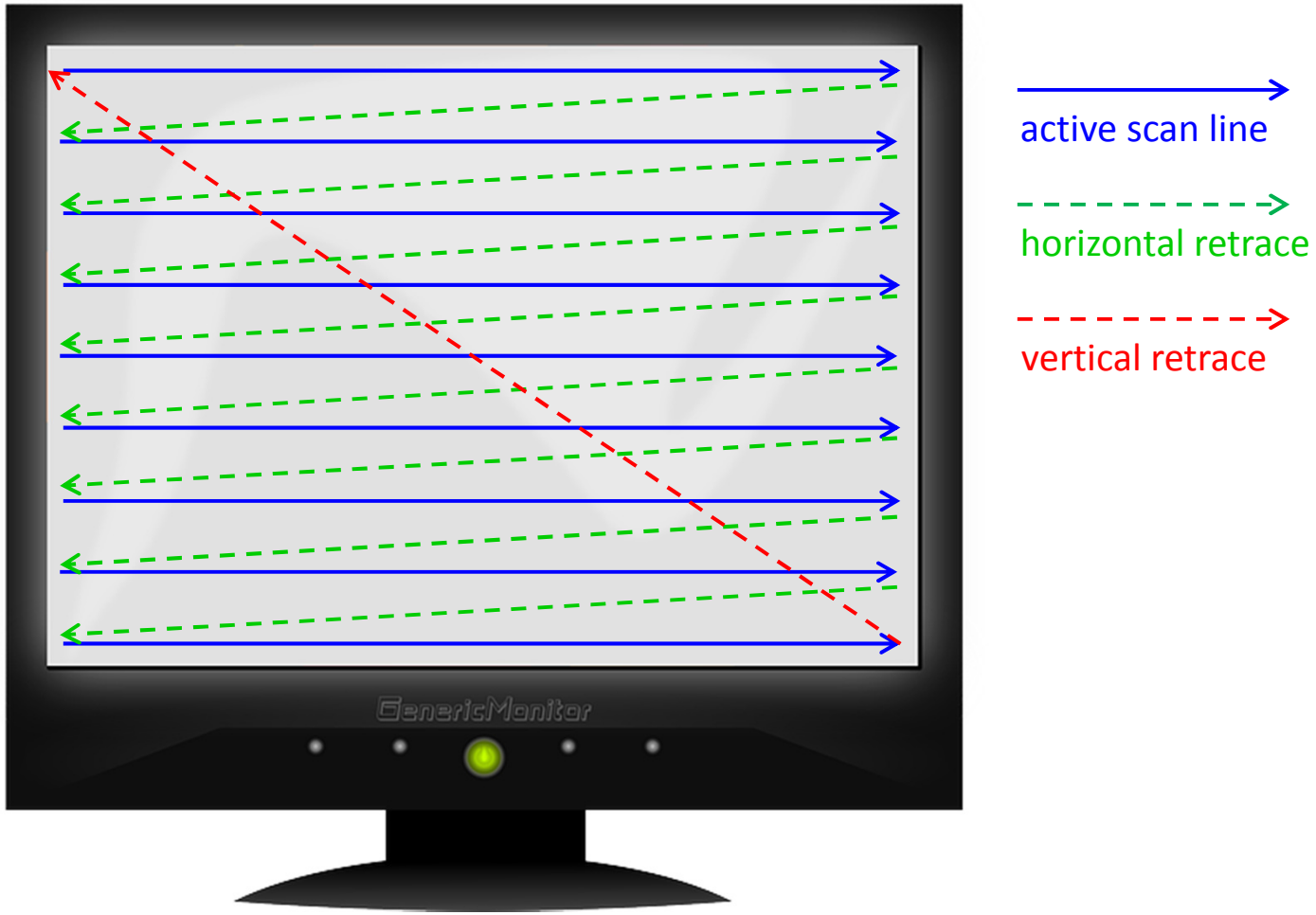
VGA – Old Soldiers Never Die

- VGA stands for Video Graphics Array; it's a video interface originally designed for CRT display:



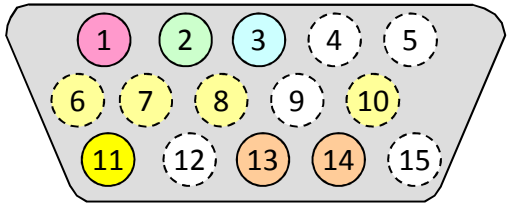
VGA Scanning Pattern

- A VGA display scans the entire screen pixel-by-pixel:



VGA Interface Pin Assignment

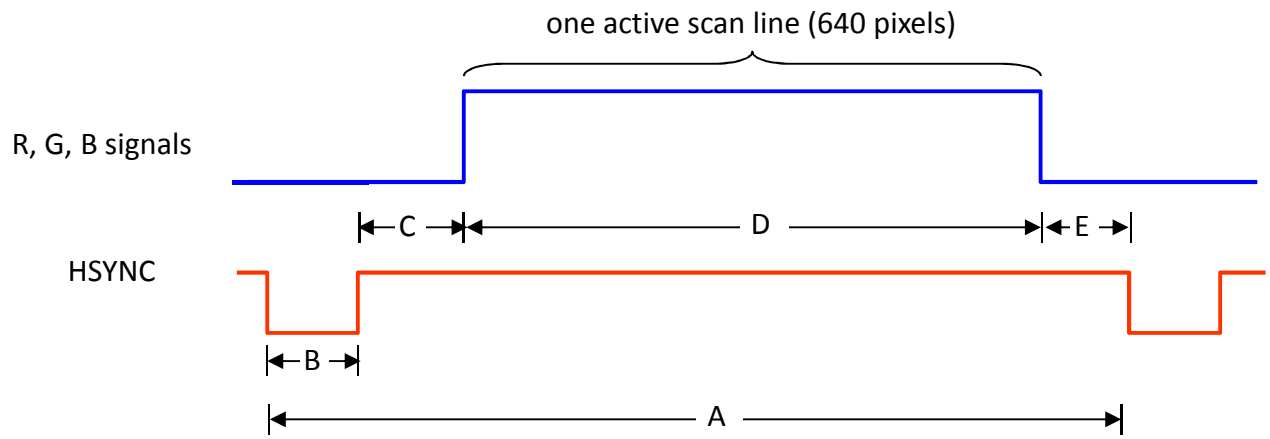
- VGA uses HD15 (a.k.a. D-sub) connectors
  - Pin #1 Red (0 ~ 0.7V)
  - Pin #2 Green (0 ~ 0.7V)
  - Pin #3 Blue (0 ~ 0.7V)
  - Pin #6, 7, 8, 10, 11 Ground
  - Pin #13 Horizontal Sync (2.5V)
  - Pin #14 Vertical Sync (2.5V)



HD-15 male

VGA Signal Timing (1/2)

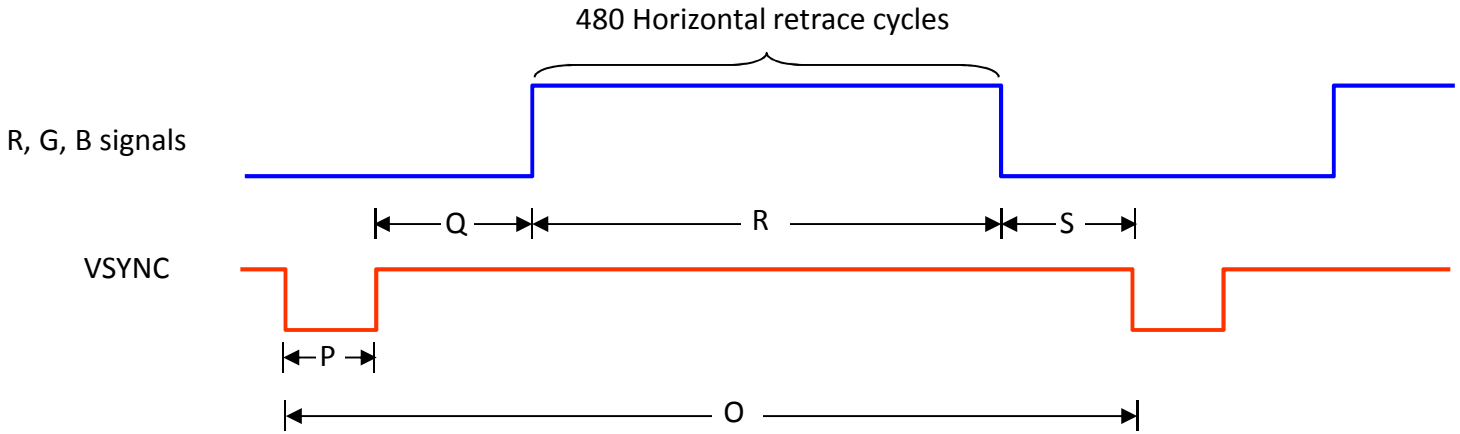
- Horizontal Retrace Cycles (for 640x480@60Hz):
  - 1/31.77μs = 31476 Hz
  - 31476/60 = 525 lines/frame



Parameters	A	B	C	D	E
Time	31.77μs	3.77μs	1.89μs	25.17μs	0.94μs

VGA Signal Timing (2/2)

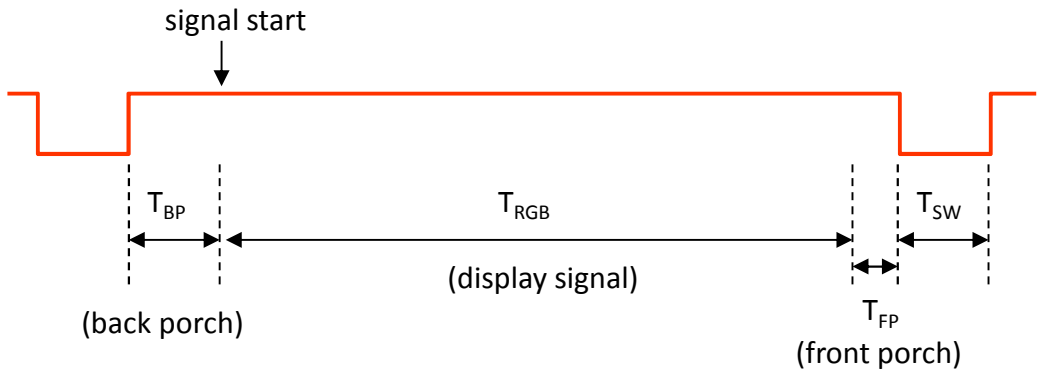
- Vertical Retrace Cycles (for 640x480@60Hz):
  - 1/16.66ms = 60 Hz (frames/second)



Parameters	O	P	Q	R	S
Time	16.66ms	64μs	1.02ms	15.25ms	0.35ms

Sync Timing in Pixel Clocks

- The Horizontal Sync (HS) and Vertical Sync (VS) signal in pixel clock ticks are as follows:



Format	Sync Type	Clock	Total	T_{RGB}	T_{FP}	T_{SW}	T_{BP}
VGA 640x480@60Hz	HS (pixels)	25.175MHz	794	640	13	95	46
	VS (lines)		528	480	13	2	33
XGA 1024x768@60Hz	HS (pixels)	65MHz	1344	1024	24	136	160
	VS (lines)		806	768	9	6	23

Vertical Timing of VGA Modes

VGA Mode	Lines Total	Line Width	Sync Pulse (μs)	Sync Pulse (line)	T_{BP} (μs)	T_{BP} (line)	T_{ACTIVE} (μs)	T_{ACTIVE} (line)	T_{FP} (μs)	T_{FP} (line)	Whole frame period (μs)	Whole frame period (line)
640x480@60Hz	525	31.78μs	63	2	953	30	15328	484	285	9	16683	525
640x480@72Hz	520	26.41μs	79	3	686	26	12782	484	184	7	13735	520
800x600@56Hz	625	28.44μs	56	1	568	20	17177	604		–1*	17775	625
800x600@60Hz	628	26.40μs	106	4	554	21	15945	604		–1*	16579	628
800x600@72Hz	666	20.80μs	125	6	436	21	12563	604	728	35	13853	666

Notes:

- Active area is actually an active area added with 4 overscan border lines (in some other VGA timing tables those border lines are included in back and front porch)
- Note that when the active part of VGA page is widened, it passes by the rising edge of the vertical sync signal in some modes (marked with *)

Horizontal Timing of VGA Modes

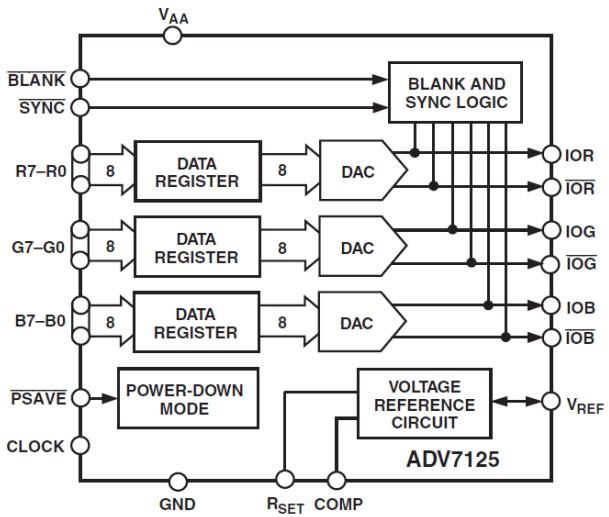
VGA Mode	Pixel Clock	Sync Pulse		T_{BP} (pix)	T_{ACTIVE} (pix)	T_{FP} (pix)	Whole line period (pix)
640x480@60Hz	25.175MHz	3.81μs	96 pix	45	646	13	800
640x480@72Hz	31.5MHz	1.27μs	40 pix	125	646	21	832
800x600@56Hz	36MHz	2μs	72 pix	125	806	21	1024
800x600@60Hz	40MHz	3.2μs	128 pix	85	806	37	1056
800x600@72Hz	50MHz	2.4μs	120 pix	61	806	53	1040

Notes:

- Active area is actually an active area added with 6 overscan border pixels (in some other VGA timing tables those border pixels are included in back and front porch)

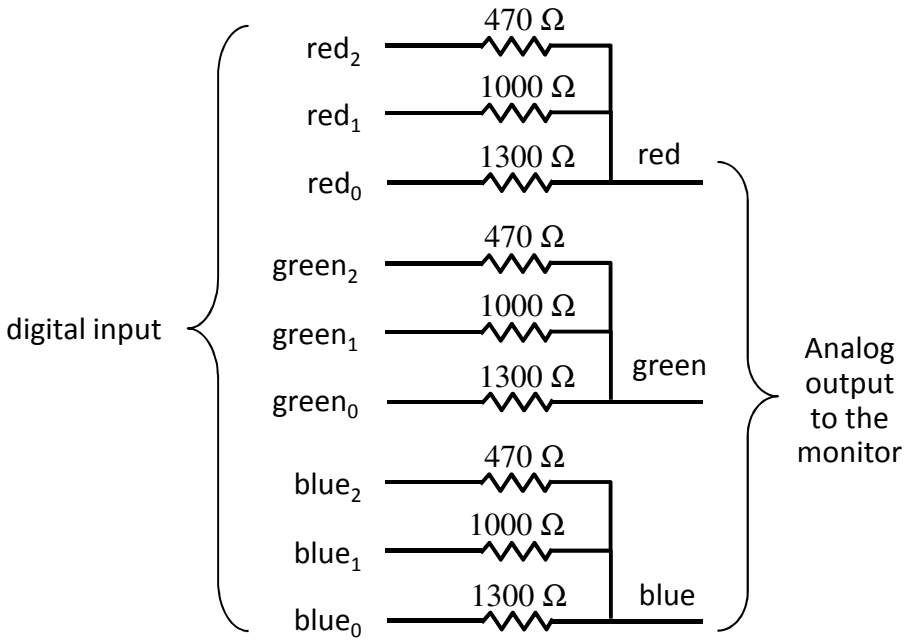
Digital-to-Analog Conversion

- VGA is an analog interface
  - 0v stands for the darkest pixel, 0.7v stands for the brightest
  - The transition from darkest pixel to brightest pixel is not linear
- A video DAC IC is usually used for converting digital picture to analog VGA signals
  - The most popular DAC is the ADV 7125 IC by Analog Devices

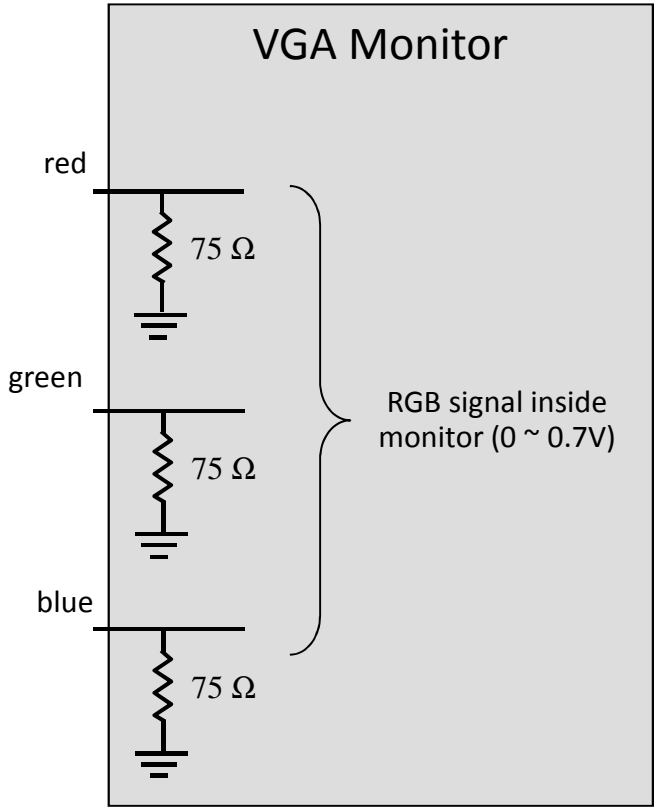


Simple VGA Interface Circuit

- A resister network can be used as a 3×3-bit VGA DAC:

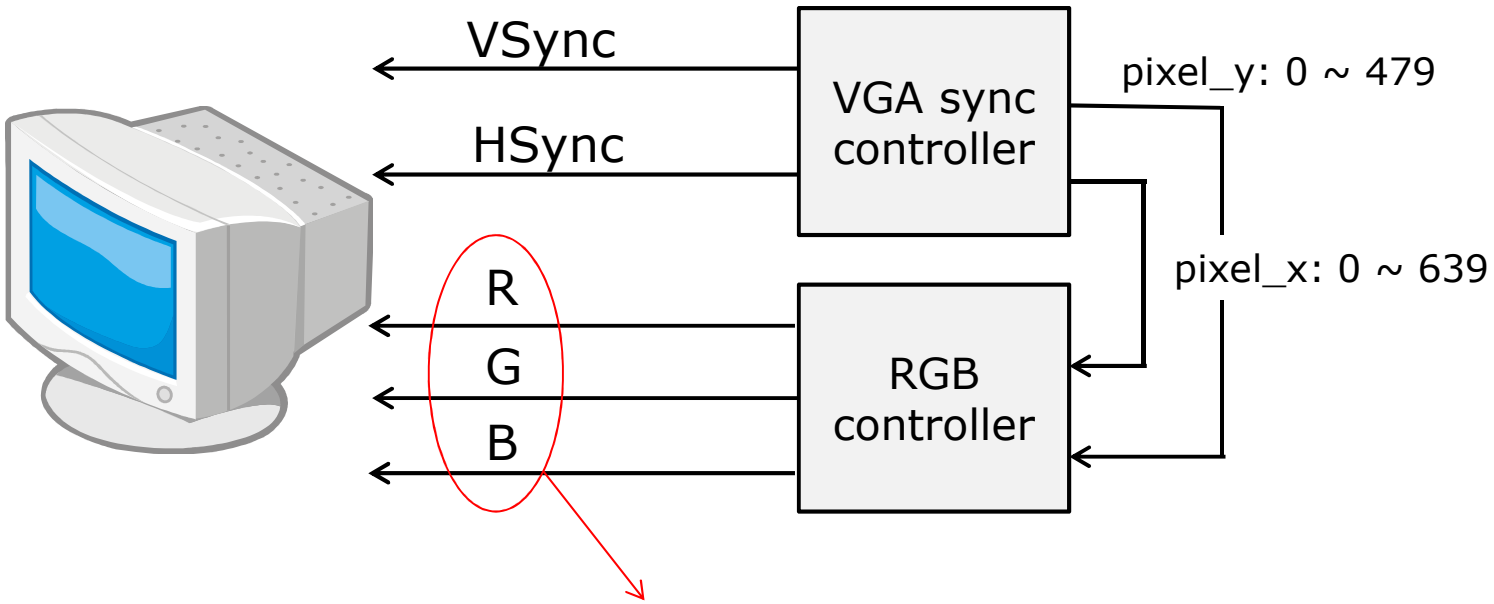


digital-to-analog conversion



VGA Controller for Lab 10

- The Verilog code of a VGA synchronization controller will be provided for this lab:



VGA Sync Controller Interfaces

- The I/O port of the VGA controller module:

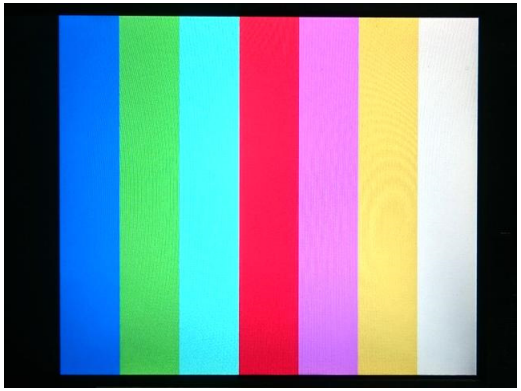
```
module vga_sync
(
  input clk,
  input reset,
  output wire oHS,
  output wire oVS,
  output wire visible,
  output wire p_tick,
  output wire [9:0] pixel_x,
  output wire [9:0] pixel_y
);
```

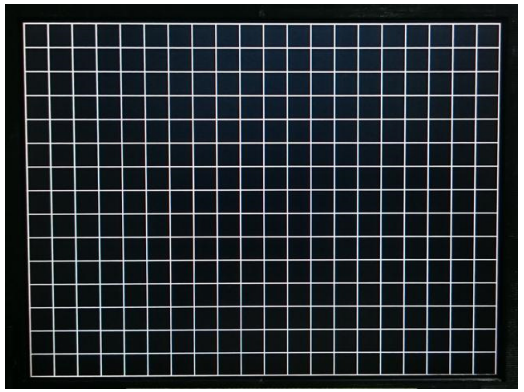
active scan line period?

update pixel?

What's in Lab 10 Sample Code

- In Lab 10, a sample circuit that shows eight video test screens will be provided
  - Users use WEST and EAST button to select different screens

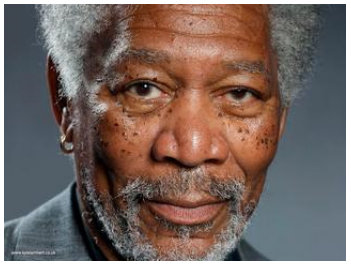





What Are the Photos for Lab10?

- Eight true color (8-bit per channel) photos in PPM format will be stored on the SD card for lab 10:

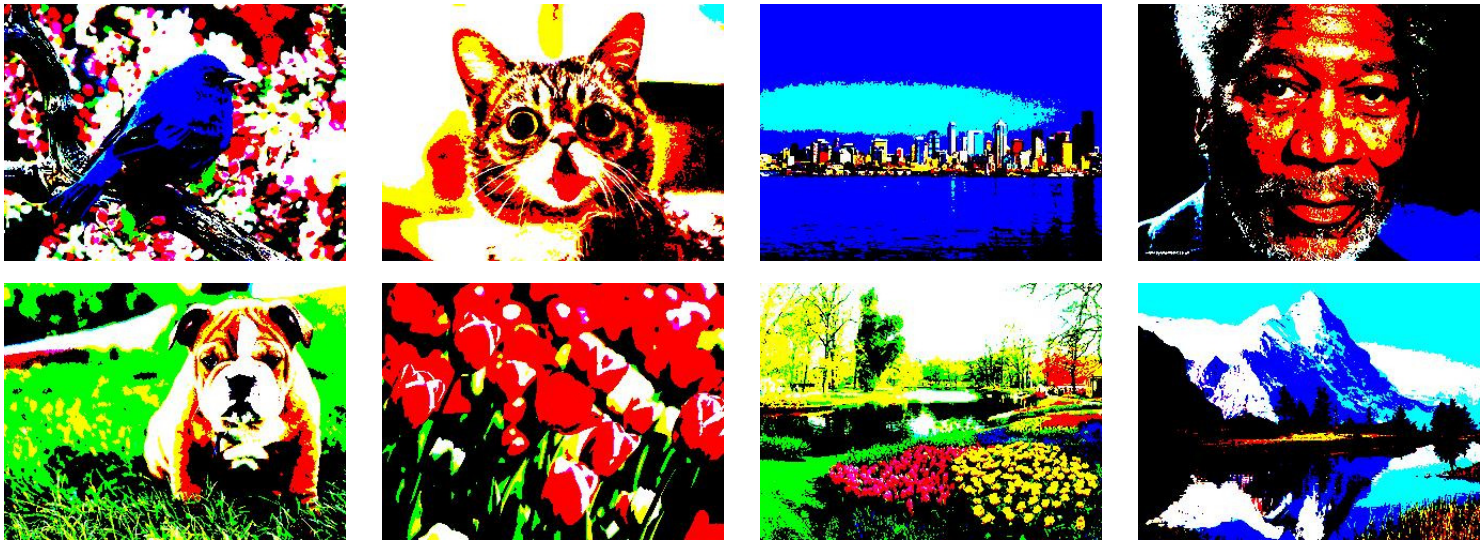




Color Reduction

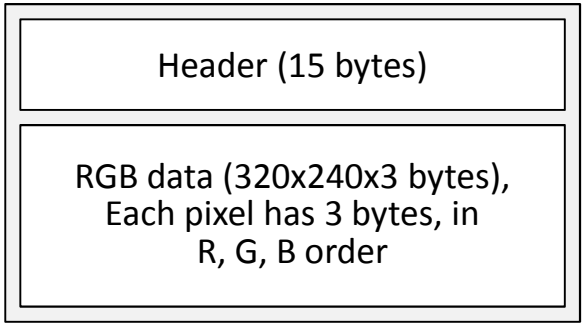
- In your circuit, after reading each photo, you must convert the color depth to 1-bit per channel



```
R <= (R_8_bit > 128)? 1 : 0;
G <= (G_8_bit > 128)? 1 : 0;
B <= (B_8_bit > 128)? 1 : 0;
```

Reading the Photos From SD Card

- All the photos stored on the SD card are in PPM format



- The 15-byte header is in ASCII format:
  - "P6↵320 240↵255↵", where ↵ stands for 0x0A
- Thus, you can search for the following hex codes to locate a photo:
  - 50 36 0A 33 32 30 20 32 34 30 0A 32 35 35 0A

Video Frame Buffer Structure

- The video frame buffer is a 3-bit memory declared as:

```
reg [2:0] vbuf[320*240-1:0];
```

- The buffer will be synthesized as a single-port Block RAM (BRAM) if its read/write follow the following rules
  - If the write operations only happen at clock edges
  - If there is only one read or write operation at each clock edge
  - If the read/write data width is less than or equal to 64 (well, this actually depends on the FPGA model, but 64 should be safe for all Xilinx FPGAs)
- BRAM is a single-cycle memory, which means it can output different data items at every clock cycles!

Sending Frame Buffer Content to VGA

- The frame buffer can be connected to the VGA controller as follows:

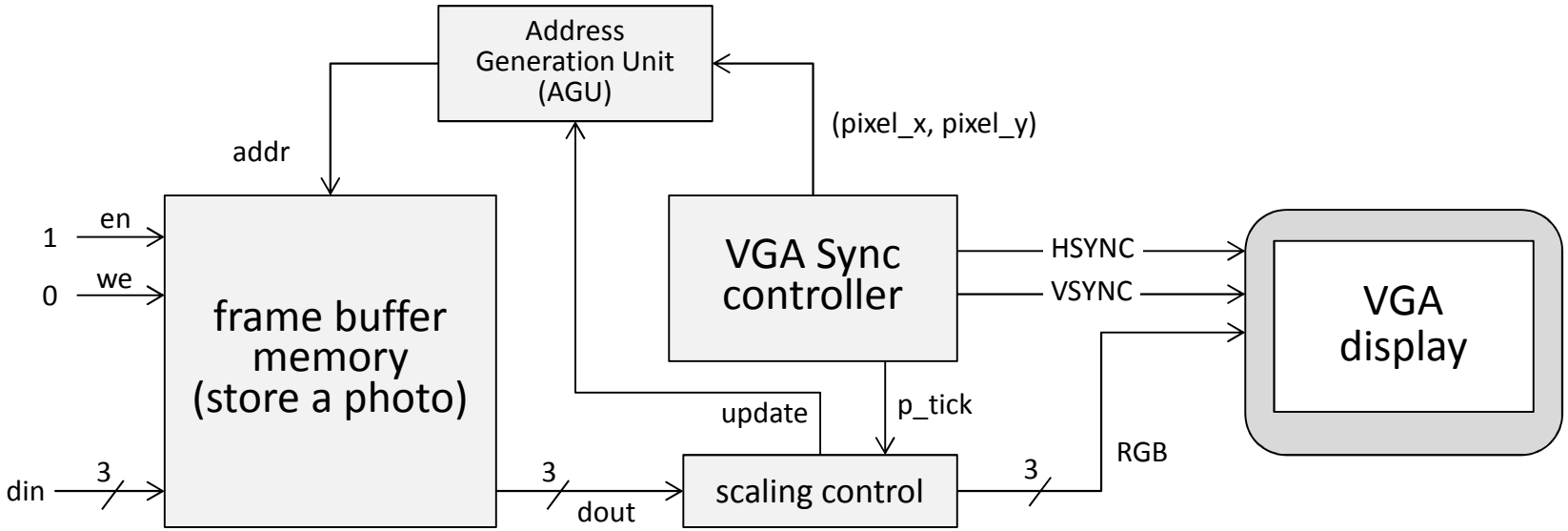
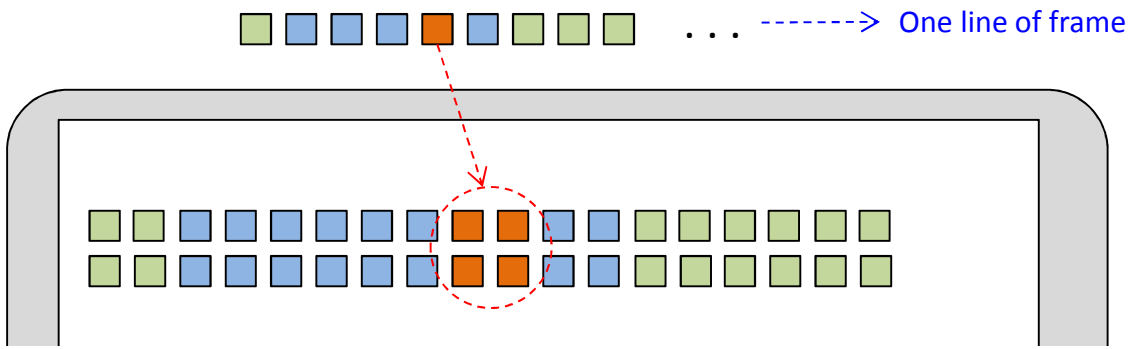


Image Scaling

- The size of our frame buffer is of 320×240 pixels, but the VGA resolution is of 640×480 pixels → we must blow up the photo by 2× in each dimension
- A simple scaling algorithm can be used:
  - Each scanline in the frame buffer is used repeatedly for two horizontal scanlines
  - Each pixel in a scanline is repeated for two pixel-clock cycles



References

- Chapter 6 of *Spartan-3E Starter Kit Board User Guide, UG230 (v1.0)*.