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Subject :- RMAE

Q1) a) What do you mean by Status register in ATmega 328P? Explain the role of each bit.

→ The status register contains information about the result of the most recently executed arithmetic instruction. This information can be used for altering program flow in order to perform conditional operations. The Status register is updated after all ALU operations, as specified in the instruction set reference.

Bit 0 :- Carry Flag

The Carry flag C indicates a carry in an arithmeti or logic operation.

Bit 1 - Z : Zero Flag

The Zero flag Z indicates a zero result in an arithmetic or logic operation.

Bit - 2 - N : Negative flag :

The negative flag N indicates a negative result in an arithmetic or logic operation.

Bit 3 - V : Two's Complement overflow flag

The Two's complement overflow flag V supports two Complement arithmetic

Bit 4 - S :- Sign flag

The S bit is always an exclusive or between th

Negative flag N and the two's complement overflow flag V.

Bit 5 - H : Half Carry Flag

The half carry flag H indicates a Half Carry in some arithmetic operations.

Bit 6 - T : Copy Storage

The Bit copy instructions (BLD) (Bit Load) and BST (Bit STore) use the T-bit as source or destination for the operated bit.

Bit 7 - I : Global Interrupt Enable

The Global Interrupt enable bit must be set for the interrupts to be enabled. If the Global Interrupt enable register is cleared, none of the interrupts enabled independent of the individual interrupt enable settings.

b) Explain Stack pointer and program Counter in case of ATmega 328P.

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Stack Pointer :-

The stack is mainly used for storing temporary data, for storing local variables and for storing return addresses after interrupts and subroutine calls. The stack pointer points to the data SRAM stack area where the subroutine and interrupt stacks are located. A stack PUSH command will decrease the stack pointer. The stack in the data sram must be defined by the program before any subroutine calls are executed or interrupts are enabled.

Program Counter :-

A program counter is a register that holds the address of the next instruction to be executed. Instruction pointer, instruction address register and the instruction counter are some of its alternative names.

Each time when the CPU fetches an instruction, the program counter increases by one. After fetching an instruction, it points to the next instruction in the sequence. Resetting the computer will make the program counter value to zero.

Q2. What do you mean by Timer/Counter in ATmega? Explain the registers used for controlling them in detail.

→ The ATmega 328P is equipped with two 8-bit timers and one 16 bit timer. A timer is a simple counter. The input clock of microcontroller and operation of the timer is independent of the program execution. All the AVR microcontrollers have timers as an inbuilt peripherals.

① OCR0A - Output compare register A

The output compare register A contains an 8 bit value that is continously compared with the counter value. A match can be used to generate an output compare interrupt, or to generate a waveform output on the OC0A pin

② OCR0B - Output Compare Register B

The output compare register B contains an

8 bit value that is continously compared with the counter value. A match can be used to generate an output compare interrupt or to generate a waveform output on the OC0B pin.

Q3) a) What do you mean by Polling, interrupt and interrupt Vector address?

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Polling :- Repeatedly reading a dataport and testing the input data value. The processor takes a measurement from a port/sensor at regular time intervals. This happens even if there is no change in the connected device. Guaranteed or predictible time slices are allocated to each device that is being polled.

Interrupt :- Interrupt is a signal generated by hardware or software that triggers the ISR to run. It only occurs when needed. Interrupts are more efficient than polling but the timing is less predictable. More difficult to code than polling.

Interrupt vector address :-

When the interrupt is triggered, the main code is paused and control jumps to the interrupt vector. The code for that ISR is executed. The ISR is located at vector address in ROM. Each of the 3 groups of pins has a ISR at three possible vectors. The interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address the higher the priority.

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Q3) b) Explain the PCINT in ATmega in detail.

→ Reading the state of an input is necessary in microcontroller programs. A specific input pin changing state can be notified. This is done by Pin change interrupts. Each of the digital I/O pins can be configured as PCINT by writing into interrupt registers in software. Group of pins share the same PCINT vector address. There are 3 PCINT groups. Programmer needs to determine which pin change causes the interrupt within the ISR before acting on it. Special registers associated with PCINT are :-

1) PCICR :- Pin change interrupt control Register

2) PCIFR - Pin change interrupt flag register

3) PCMSKx - Pin change mask register

X - Indicates 0, 1, 2. These are PCINT groups 0, 1, 2.