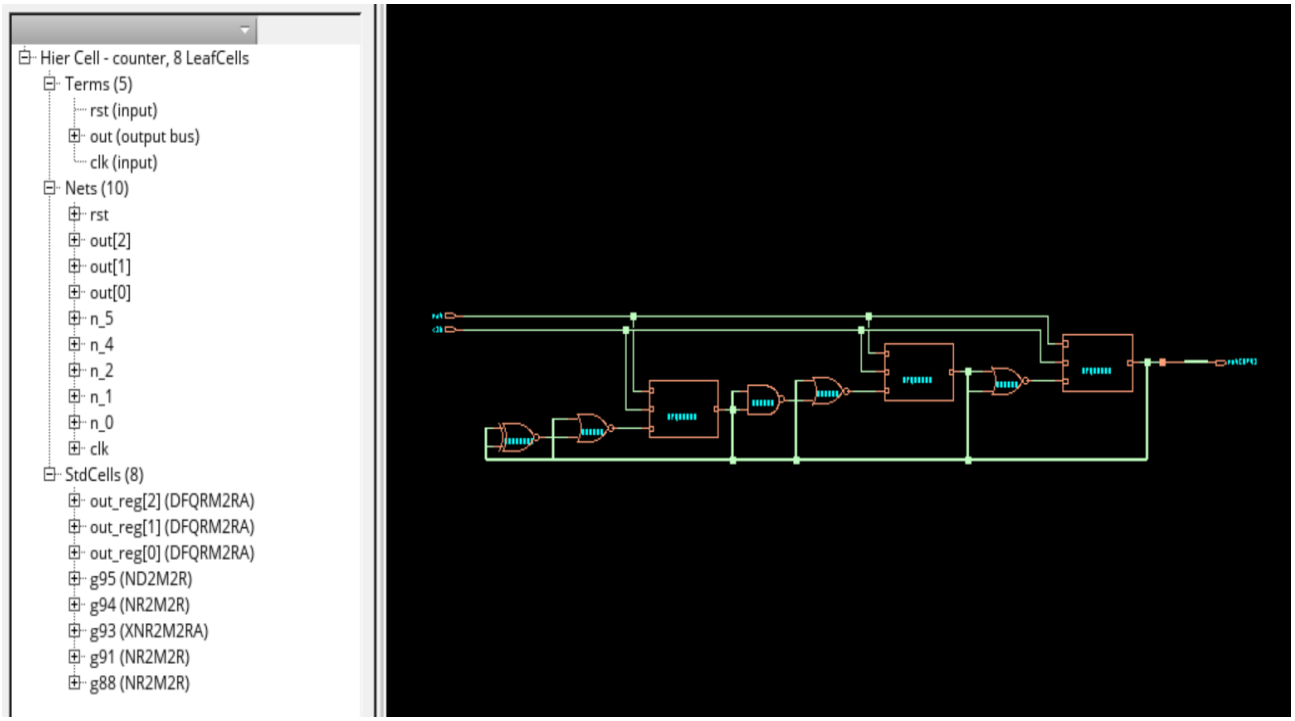
ELP831 – ASSIGNMENT

RTL to GDSII flow of mod5 counter

S.V. Swapna manjiri

Een212025

Gate level schematic:



Power analysis just after synthesis:

Power Details Report — dirac1

Generated by: Genus(TM) Synthesis Solution 19.12-s121_1 (Dec 3 2019 15:07:17)
Generated on: Oct 17 2021 16:35:35
Module: design:counter
Technology library: uk65lscllmvbbr_100c25_tc
Operating conditions: uk65lscllmvbbr_100c25_tc (balanced_tree)
Wireload mode: top

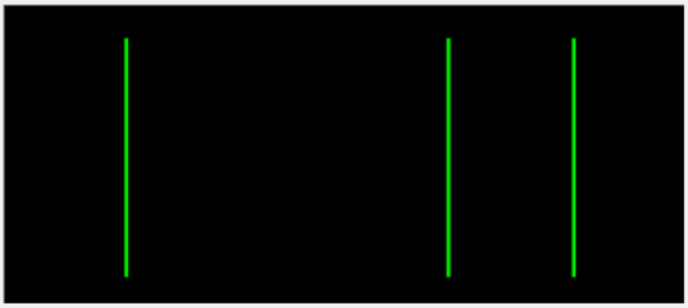
Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
counter	8	1.484	2050.434	376.866	2427.299

Timing analysis just after synthesis:

Report File(s) top.mtarpt

File Analysis Category

Path Histogram



Category Summary

Name:	all
Total Path:	3
Passing Path:	3
Failing Path:	0
WNS:	0.0000
TNS:	0.0000

Path Category

Cate	H	Category Name	Correction	WNS	TNS	#Failing Path
1		all		0.000	0.000	0

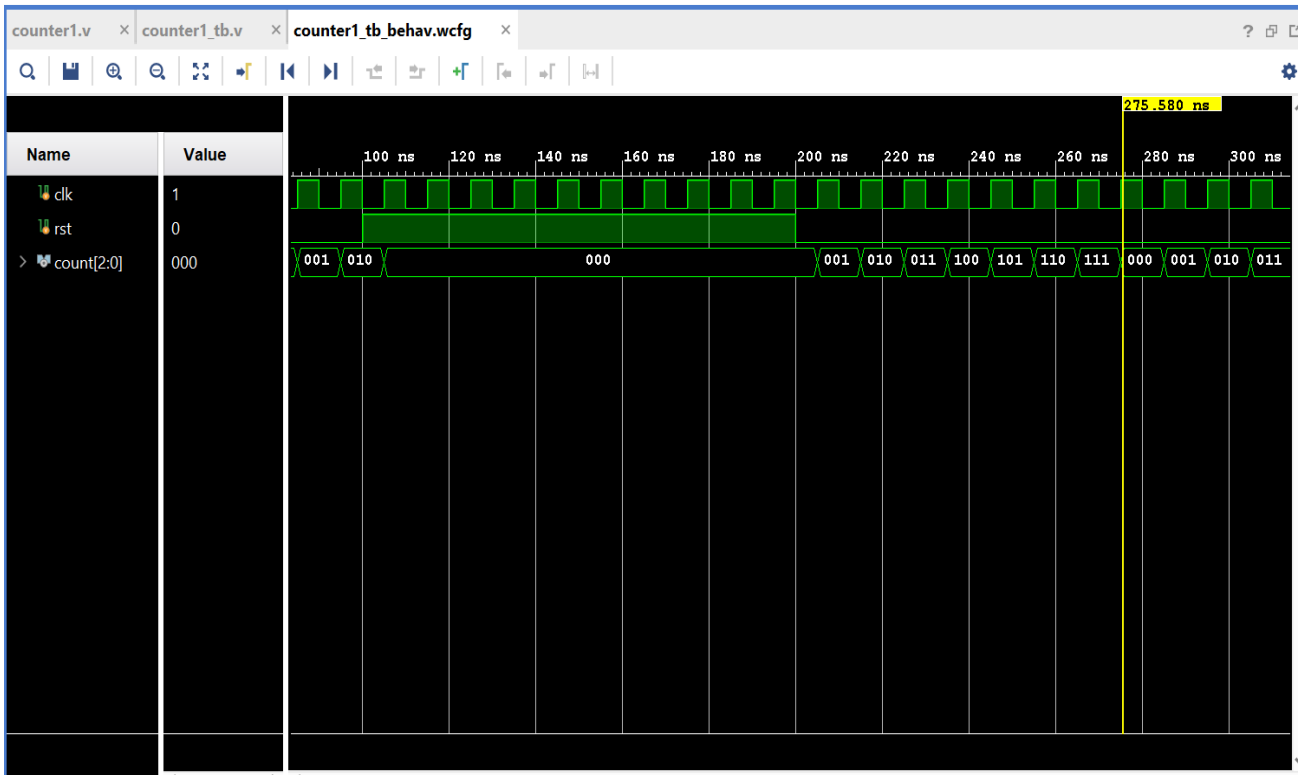
Path List

Category: all, Slack Range: all

Page: 1

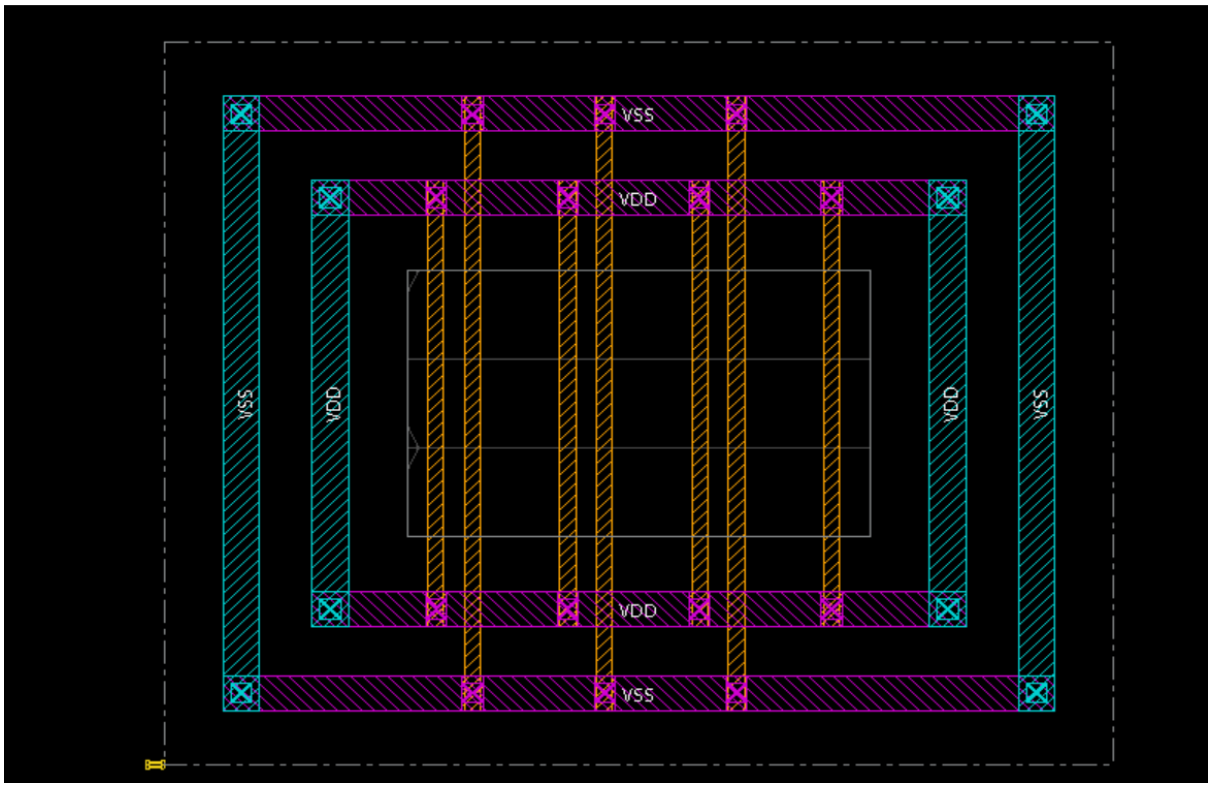
H	Path	Clock	ReqTime	Slack	Startpoint Pin	Endpoint Pin
	1	clk(leading)->clk(lead...	9.990	9.623	out_reg[1]/Q	out_reg[1]/D
	2	clk(leading)->clk(lead...	9.990	9.694	out_reg[0]/Q	out_reg[2]/D
	3	clk(leading)->clk(lead...	9.990	9.722	out_reg[2]/Q	out_reg[0]/D

Counter simulation:



Physical design:

Floor planning and power plannig



Ring generation

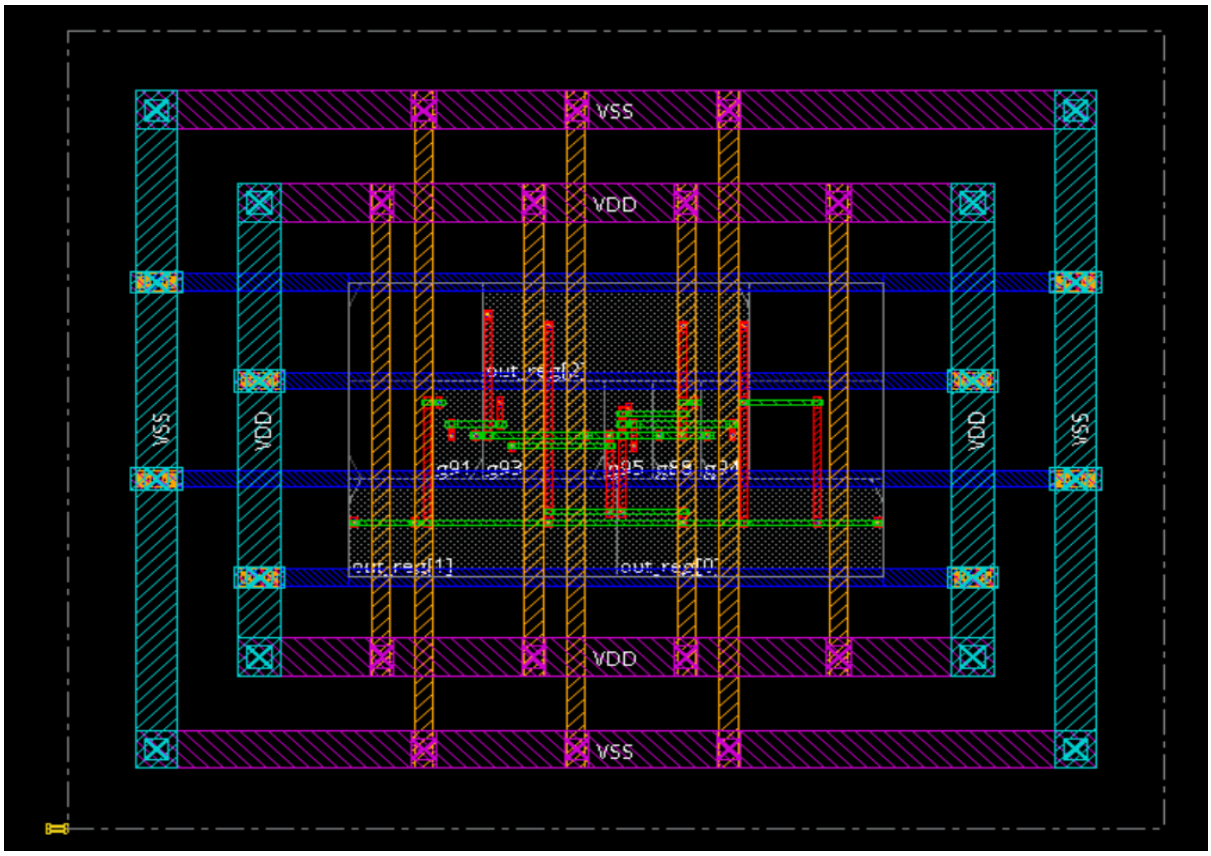
```
innovus 1> Adjusting core size to PlacementGrid : width :8.8 height
innovus 1> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

Ring generation is complete.
vias are now being generated.
addRing created 8 wires.
ViaGen created 8 vias, deleted 0 via to avoid violation.
+--------+----------------+----------------+
|  Layer |     Created    |     Deleted    |
+--------+----------------+----------------+
|   ME7  |        4       |       NA       |
|   VI7  |        8       |        0       |
|   ME8  |        4       |       NA       |
+--------+----------------+----------------+
```

Stripe generation

```
Stripe generation is complete.
vias are now being generated.
addStripe created 7 wires.
ViaGen created 14 vias, deleted 0 via to avoid violation.
+--------+----------------+----------------+
|  Layer |     Created    |     Deleted    |
+--------+----------------+----------------+
|   ME6  |        7       |       NA       |
|   VI6  |       14       |        0       |
+--------+----------------+----------------+
```

Routing and placement:




```
sroute created 12 wires.
ViaGen created 56 vias, deleted 0 via to avoid violation.
+--------+----------------+----------------+
|  Layer |     Created    |     Deleted    |
+--------+----------------+----------------+
|   ME1  |       12       |       NA       |
|   VI1  |        8       |        0       |
|   VI2  |        8       |        0       |
|   VI3  |        8       |        0       |
|   VI4  |        8       |        0       |
|   VI5  |        8       |        0       |
|   VI6  |        8       |        0       |
|   VI7  |        8       |        0       |
+--------+----------------+----------------+
*** Starting placeDesign default flow ***
*** Start deleteBufferTree ***
```

Timing summary: PRE- CTS

1) Setup mode – worst case
2) Hold mode – best case

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  9.267  |  9.267  |  9.285  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    6    |    3    |    3    |
+--------------------+---------+---------+---------+

+----------------+-----------------------------------+------------------+
|                |              Real                 |       Total      |
|    DRVs        +------------------+----------------+------------------|
|                |  Nr nets(terms)  | Worst Vio      |  Nr nets(terms)  |
+----------------+------------------+----------------+------------------+
|   max_cap      |      0 (0)       |   0.000        |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000        |      0 (0)       |
|   max_fanout   |      0 (0)       |     0          |      0 (0)       |
|   max_length   |      0 (0)       |     0          |      0 (0)       |
+----------------+------------------+----------------+------------------+

Density: 69.697%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.33 sec
Total Real time: 0.0 sec
Total Memory Usage: 2079.851562 Mbytes
```

```
          timeDesign Summary
------------------------------------------------------

Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.096  |  0.096  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    3    |    3    |    0    |
+--------------------+---------+---------+---------+

Density: 69.697%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------
Reported timing to dir timingReports
Total CPU time: 0.33 sec
Total Real time: 0.0 sec
Total Memory Usage: 2058.429688 Mbytes
```

Design final summary: Clock tree synthesis

```
     optDesign Final Summary
---------------------------------------------------------

Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  9.238  |  9.277  |  9.238  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    6    |    3    |    3    |
+--------------------+---------+---------+---------+

+-----------------+--------------------------------+------------------+
|                 |              Real              |       Total      |
|    DRVs         +------------------+-------------+------------------|
|                 |  Nr nets(terms)  | Worst Vio   |  Nr nets(terms)  |
+-----------------+------------------+-------------+------------------+
|   max_cap       |      0 (0)       |   0.000     |      0 (0)       |
|   max_tran      |      0 (0)       |   0.000     |      0 (0)       |
|   max_fanout    |      0 (0)       |     0       |      0 (0)       |
|   max_length    |      0 (0)       |     0       |      0 (0)       |
+-----------------+------------------+-------------+------------------+

Density: 69.697%
Routing Overflow: 0.00% H and 0.00% V
```

Post CTS:

```
Setup views included:
 worst_case

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  9.238  |  9.277  |  9.238  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    6    |    3    |    3    |
+--------------------+---------+---------+---------+
```

Hold mode

```
Hold  views included:
 best_case

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):|  0.094  |  0.094  |  0.000  |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |
|    Violating Paths:|    0    |    0    |    0    |
|          All Paths:|    3    |    3    |    0    |
+--------------------+---------+---------+---------+
```

Geometry verification:

```
VG: elapsed time: 0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
```

DRC verification:

```
*** Starting Verify DRC (MEM: 2126.7) ***

 VERIFY DRC ..... Starting Verification
 VERIFY DRC ..... Initializing
 VERIFY DRC ..... Deleting Existing Violations
 VERIFY DRC ..... Creating Sub-Areas
 VERIFY DRC ..... Using new threading
 VERIFY DRC ..... Sub-Area: {0.000 0.000 18.000 14.600} 1 of 1
 VERIFY DRC ..... Sub-Area : 1 complete 0 Viols.

 Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.0  ELAPSED TIME: 0.00  MEM: 0.0M) ***
```

Connectivity verification:

```
Design Name: counter
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (18.0000, 14.6000)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
   Found no problems or warnings.
End Summary

End Time: Mon Oct 18 17:19:39 2021
Time Elapsed: 0:00:00.0

********* End: VERIFY CONNECTIVITY *********
   Verification Complete : 0 Viols.   0 Wrngs.
   (CPU Time: 0:00:00.0   MEM: 0.000M)
```

Final layout: