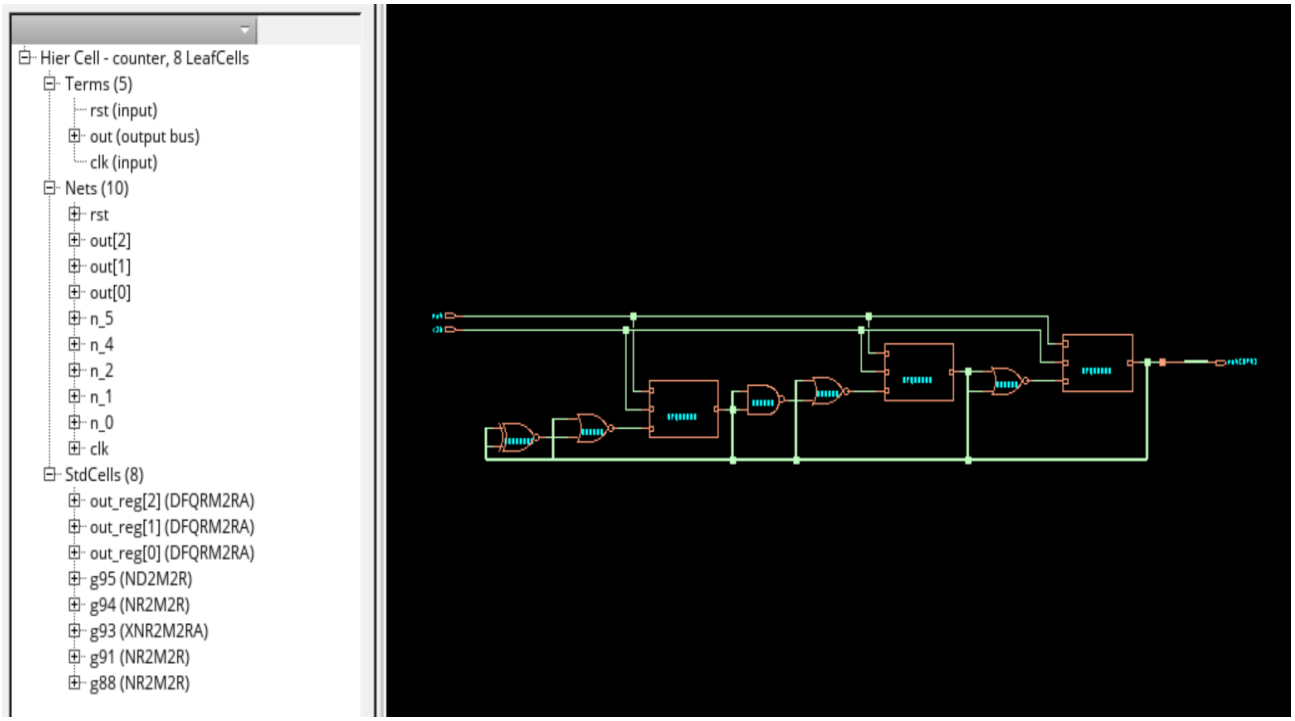
ELP831 – ASSIGNMENT

RTL to GDSII flow of mod5 counter

Gate level schematic:



Power analysis just after synthesis:

Power Details Report — dirac1

Generated by: Genus(TM) Synthesis Solution 19.12-s121_1 (Dec 3 2019 15:07:17)
Generated on: Oct 17 2021 16:35:35
Module: design:counter
Technology library: uk65lscllmvbbr_100c25_tc
Operating conditions: uk65lscllmvbbr_100c25_tc (balanced_tree)
Wireload mode: top

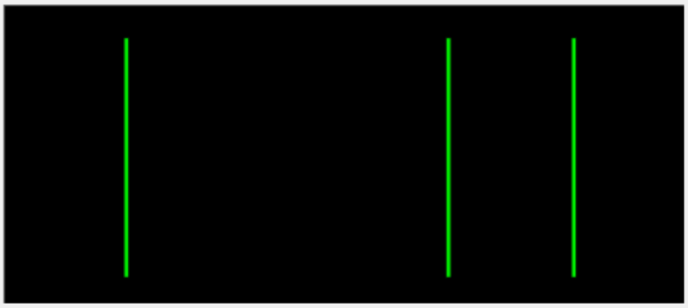
Instance	Cells	Leakage (nW)	Internal (nW)	Net (nW)	Switching (nW)
counter	8	1.484	2050.434	376.866	2427.299

Timing analysis just after synthesis:

Report File(s) top.mtarpt

File Analysis Category

Path Histogram



Category Summary

Name:	all
Total Path:	3
Passing Path:	3
Failing Path:	0
WNS:	0.0000
TNS:	0.0000

Path Category

Cate	H	Category Name	Correction	WNS	TNS	#Failing Path
1		all		0.000	0.000	0

Path List

Category: all, Slack Range: all

Page: 1

H	Path	Clock	ReqTime	Slack	Startpoint Pin	Endpoint Pin
	1	clk(leading)->clk(lead...	9.990	9.623	out_reg[1]/Q	out_reg[1]/D
	2	clk(leading)->clk(lead...	9.990	9.694	out_reg[0]/Q	out_reg[2]/D
	3	clk(leading)->clk(lead...	9.990	9.722	out_reg[2]/Q	out_reg[0]/D

Counter simulation: