

Academic Qualifications

Year	Degree/Certificate	Institute	CPI/%
2022 - Present	B.Tech	Indian Institute of Technology Kanpur	9.3/10
2022	CBSE(XII)	Bhavan Vidyalaya, Panchkula	96.6%
2020	CISCE(X)	Yadavindra Public School, Patiala	92.4%

Scholastic Achievements

- Secured **All India Rank 109** in **JEE Advanced 2022**, conducted by **IIT Bombay** amongst the 250,000 shortlisted candidates
- Secured **All India Rank 76** amongst the approximately 1 million applicants in **JEE Mains 2022**, conducted by the NTA
- Selected for a **Semester Exchange Program** to **EPFL, Switzerland** having a **World QS University Ranking of 36**
- Recipient of the **Class of 1990 Scholarship, IITK** by SSPC for the year **2022** for having **exceptional JEE Advanced Rank**
- Awarded the **Academic Excellence Award** for exceptional academic performance for the years **2022-2023** and **2023-2024**
- Qualified **Kishore Vaigyanik Protsahan Yojna (KVPY) 2022**, conducted by **IISc Bangalore**, with **All India Rank 96**
- Amongst the **35** students, throughout the country, to qualify the **Indian National Mathematics Olympiad (INMO) 2022**
- Amongst the **53** students, throughout the country, to qualify the **Indian National Chemistry Olympiad (INChO) 2022**
- Amongst the **32** students, throughout the country, to qualify the **Indian National Astronomy Olympiad (INAO) 2022**
- Among the **300** students, in the country, to qualify the **Indian Olympiad Qualifier in Physics (IOQP), Part-I 2022**

Work Experience

Speech Technologies in Indian Languages | MADHAV Lab | Mentor: Prof. Vipul Arora (Dec' 23)

Objective	Created a Speech-to-Text system for use by Prasar Bharti (Doordarshan) in regional language channels
Execution	Experimented with VAD models, PANNs , SileroVAD , FSMN-VAD and WebRTC using Hindi news audio Implemented streaming ASR using ESPnet from the microphone of the local device without loading audio Implemented a streaming ASR model for Hindi using offline ESPnet model , to reduce training effort
Result	Created a process that successfully allowed any ESPnet style offline model to be used for streaming

Competitive Programming

- Experienced competitive programmer with a peak rating of **1733 (Expert)** on **Codeforces** and **1669** on **Codechef**
- Secured **Global Rank 863** in **Codeforces Round 955**(Division 2) and **Global Rank 266** in **Codechef Starters 141C**

Key Projects

Elysium | CS253 course project | Mentor: Prof. Indranil Saha (Jan'24 - Apr'24)

- Collaborated with a team of **10** to develop a **Full Stack Web Application** using **MERN Stack** for **Sports and Wellness**
- Implemented a **priority based booking system** that utilizes user history to calculate **dynamic scores** optimizing efficiency
- Implemented a matchmaking system **Matching Players** using a **ladder based rating system** during the **booking step**
- Maintained **comprehensive documentation** of the entire project and extensively both **alpha** and **beta** tested the application

Algebraic Circuit Complexity | Under-Graduate Project | Mentor: Prof. Nitin Saxena (Jan'24 - Apr'24)

- Learnt about models of **computational complexity** like **Arithmetic Circuits** and **Algebraic Branching Programs**
- Read research papers that used **Valiant's Criterion** and **Border Complexity** to prove lower bounds for **special circuits**
- Presented a **30 min talk** on a few research papers that showed **super-polynomial lower bounds** for these special circuits

Hack Companion Arbiter PUF | CS771 course project | Mentor: Prof. Purushottam Kar (Jan'24 - Apr'24)

- Designed a **mapping** for data based on transforming the **CAR-PUF** from a **non-linear** to a **linear model** using **matrices**
- Experimented with **Linear Models**, like **Logistic Regression**, **Linear Regression**, **Ridge Regression** for hacking the PUF
- Tuned the **hyper parameters** like **tolerance** and **loss function** to find the best ones for each model, using **Grid Search**

Verilog FPGA | CS220 lab project | Mentor: Prof. Mainak Chauduri (Jan'24 - Apr'24)

- Designed a **32-bits MIPS processor** using **Verilog HDL**, and Implemented it on a **Xilinx Spartan 3e FPGA** board
- Designed a **7-state FSM** handling **fetch**, **decode** and **execute** cycles, ensuring accurate instruction processing and control flow
- Worked with **MIPS Assembly** using **SPIM** to implement and simulate algorithms for **Binary Search** and **Array Addition**

Technical Skills

- Programming Languages:** C, C++, Python, JavaScript, Verilog, MIPS Assembly
- Softwares & Libraries:** Jupyter, Bash, Git-Github, LaTeX, Pandas, NumPy, Matplotlib

Relevant Courses

Data Structures and Algorithms (A)	Fundamentals of Computing - I, II (A,A*)	Discrete Maths (A)
Software Development and Operations	Introduction to Electronics (A)	Introduction to Machine Learning (A)
Probability for Computer Science	Mathematical Logic	Computer Organization