

PROJECT REPORT
ON
Emergency Vehicle Priority System



Submitted in Partial fulfilment for the award of
Post Graduate Diploma in
EMBEDDED SYSTEM AND DESIGN
From C-DAC, ACTS (Pune)

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CERTIFICATE
TO WHOMSOEVER IT MAY CONCERN

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Emergency Vehicle Priority System

Under the guidance of
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Project Guide

Project Supervisor

Acknowledgment

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Abstract

High density of vehicles on roads poses a challenge for emergency vehicle along with them. Therefore problem of traffic management is increasing for emergency vehicles. The idea behind this project is to implement a system which would alert traffic signal and let emergency vehicles navigate on precedence. Goal is to reduce latency for vehicle causing less disruption to traffic.

An emergency vehicle priority system (EVprio) is a technology that enables emergency vehicles such as ambulances, Fire Engines, Police cars to communicate with traffic control devices and prioritize their passage through intersections. The system's objective is to reduce response times and improve the efficiency of emergency services by providing a clear and safe path for emergency vehicles to travel.

The system works by using transceiver and GPS technology to detect the location of the emergency vehicle and communicate this information to traffic control devices. These devices then give the emergency vehicle priority at intersections, either by holding green lights or turning red lights green, allowing the vehicle to pass through safely and quickly.

Implementation of an emergency vehicle priority system requires coordination between emergency services, local authorities, and transportation agencies. While at traffic junctions, bypass of traffic isn't that smooth and navigation hampered. To overcome this we have to come up with new methods.

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Chapter 1

INTRODUCTION

In this project we develop on experimental setup of STM32f407VG microcontroller based approaching a Vehicle to send an alert message to traffic signal with the help of nrf24l01 Transceiver for passing emergency Vehicle by set high priority task.

1.1 Overview

Traffic lights are used to monitor on-going vehicular movements on roads and safe passage of pedestrians to cross the road. Occurrence of emergency is inevitable and it requires prompt action. One of the critical consequences of traffic problem is delay of vehicles such as Ambulances, Fire Trucks, VIPs, Ministers, and Govt. Officials.

Traffic congestion occurs during peak hours, special occasions etc. which results waiting in long queues which traps emergency vehicles too. Even if there is no rush in the traffic but due to certain limit on traffic signal, Vehicles are at standby until normalcy is restored. In order to solve this problem, traffic system needs to be controlled thus giving way to emergency vehicles which can be ambulance or say envoy. Easy control of traffic and passage of emergency vehicle through it and making them reach destination. The system works by detecting the approach of an emergency vehicle and automatically changing the traffic signals to give it a clear path through intersections. The system also provides information to the emergency vehicle about the status of upcoming signals and adjusts the timing of those signals to help the vehicle move more quickly and safely through the intersection.

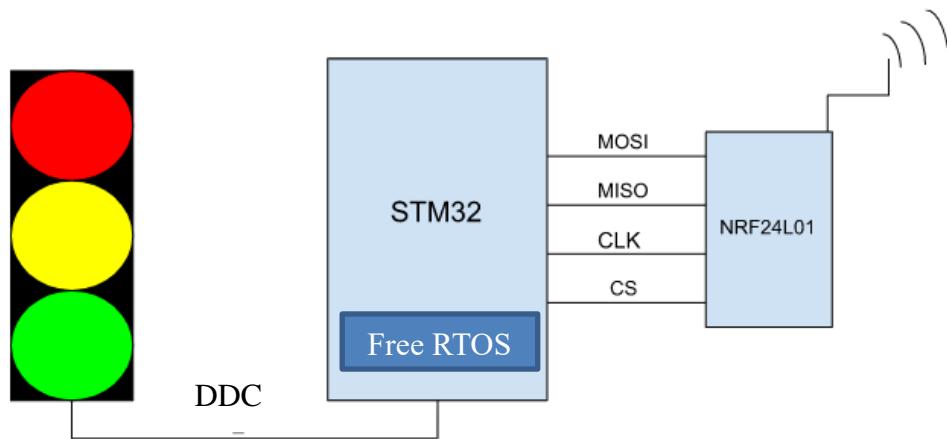
Emergency vehicle priority systems are designed to improve emergency response times, reduce the risk of accidents, and ensure the safety of both emergency personnel and the public. They are becoming increasingly common in cities and urban areas around the world, and are an important tool for emergency responders in ensuring timely and effective emergency services.

On certain route, traffic is normal but passage of emergency vehicle is given precedence in this scenario approaching emergency vehicle sends out prior details of emergency vehicles like live location, distance and time to reach etc. traffic is cleared for incoming vehicle. While at junction, a certain minimum distance away

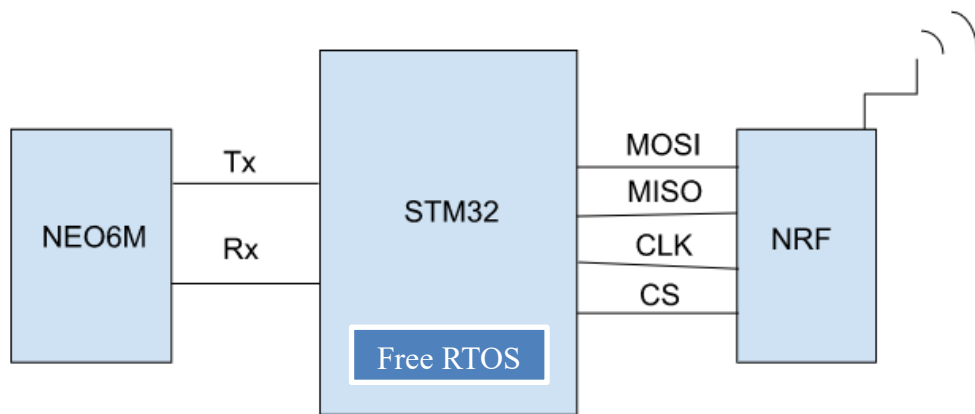
1.2 Block Diagram

Block diagram of the system is as shown below figure. The system consist of following hardware's

- STM32F07VG Board
- GPS Neo6M
- Transceiver NRF24l01



Block diagram of receiving module (RxM)



Block diagram of transmitting module (TxM)

1.3 Hardware Setup

The system is based on Cortex-M3/M4 based STM32f407VG Microcontroller board. The system is interfaced with GPS, Esp32, and Transceivers. The System is divided into two nodes.

1st node is transmitter and which is mounted in vehicle. 2nd node is called receiver which will fixed on traffic signal. They will communicate with the help of radio frequency.

Whenever transmitter comes in the range of receiver they will communicate each other and send a priority task signal to receiver. Some conditions are specified in the program.

1.3.1 STM32f407VG6

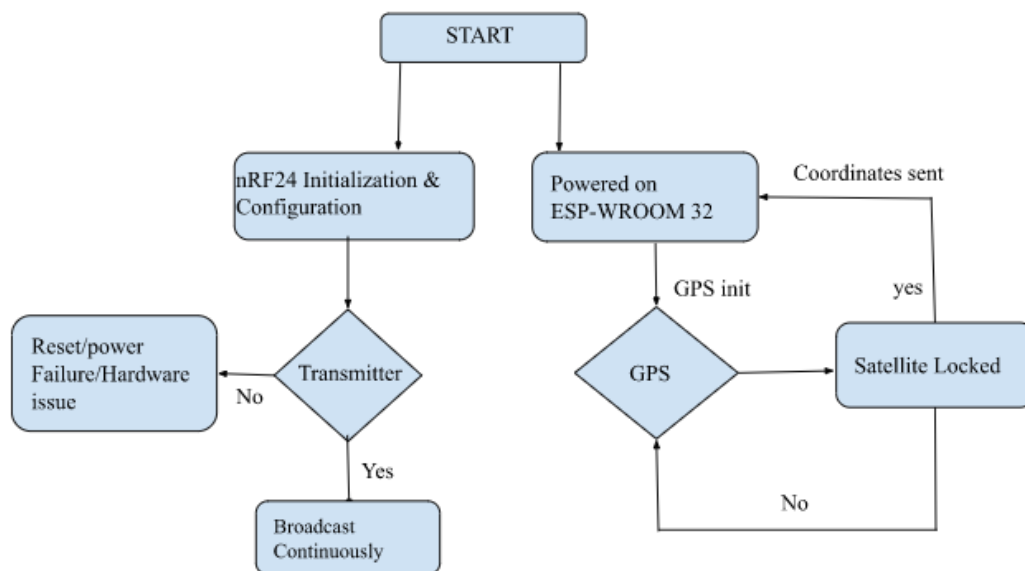
The arm Cortex-M4 processor is a high performance embedded processor with DSP instructions developed to address digital signal control markets that demand an efficient, easy to use blend of control and signal processing capabilities. The process is highly configurable enabling a wide range of implementations from those requires floating point operation, memory protection and powerful trace technology to cost sensitive device require minimal area.

In build feature and support

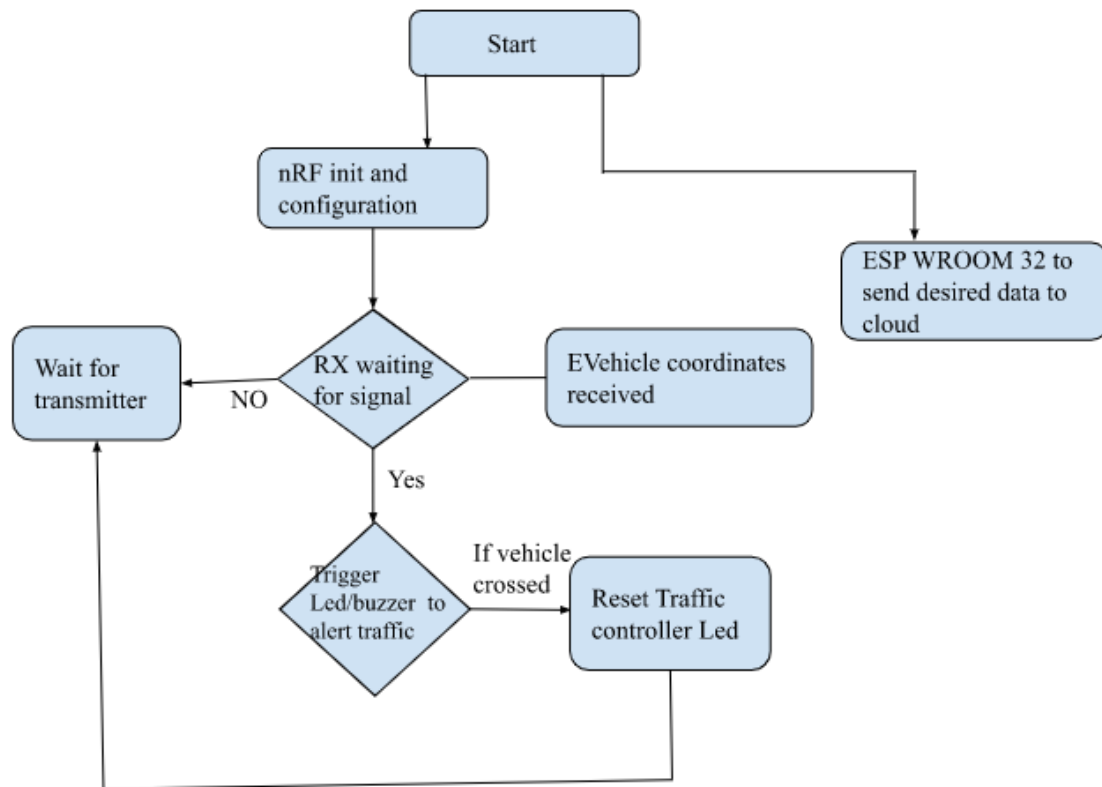
- Protocol (SPI, I2C, UART)
- Debug (JTAG)
- RTOS
- Accelerometer
- GPIO

1.4 Working Principal

Our emergency vehicle is equipped with GPS and transmitter modules which are publishing signals constantly. While at the traffic signal a receiver is mounted this is in polling mode waiting for signals. When EV arrives within the range, received signal generates an interrupt and traffic lights are manipulated i.e. concerned lane is made green while other traffic lights are forced to red until passage of vehicle is achieved. If there happens any sort of delay, extra timer can be added to rest of red signals. Live location of the EV is informed prior to arrival hence management should be done in such a way that no long queues of waiting vehicles in certain lane is increased as it will take some to clear the traffic.



Transmitter node



Receiver Node

CHAPTER 2

Literature review

2.1 General

Emergency vehicle priority system is an idea to give higher preference to vehicle which is in dire need. This vehicle is loaded with transceiver along with GPS so that advance knowledge of approaching vehicle is conveyed without any confusion about lanes or route taken.

Vehicle is equipped with transmitter which is transmitting signals and GPS to show current location and when it arrives within the proximity, it communicates with receiver mounted at traffic lights system. Receiver at the traffic light system checks the mode of current light and overrides with green with some timer so that during that allotted time rest of the traffic freezes.

2.2 Emergency Vehicle Priority System

Transmitter in EV i.e. nRF24L101 which communicates through one of the available 126 RF channels with the receiver when once it comes within range. Receiver on getting the signal generates an interrupt to make passage smooth by overturning the traffic lights.

At the junction, pre-emption and controlling the lights can be difficult, in order to deal with situation prior notice of urgency can be moderated and live location can be monitored in such a way that lanes don't stack up with huge traffic and additional delays. Overriding of traffic lights can be tricky and such scenario and would need more convenience. Prompt inspection and continuous monitoring of the junction can be reviewed.

2.2 Criticality

These systems give emergency response services to vehicles to safely navigate through traffic during peak travel duration. Time-sensitive emergencies which demand faster response times to medical emergencies resulting in faster arrival times. Rescue vehicles in terms of disaster emergencies, protect and evacuate people and save lives ,require cleared traffic for a while and so the non-hindrance vehicles.

Chapter 3

System Design

This chapter explain in details about hardware used, their features and application

3.1 STM32F407VG Microcontroller

The STM32F4 Discovery board is small devices based on STM32F407 ARM microcontroller, Which is a high-performance microcontroller. This board allows users to Develop and design applications. It has multiple modules within itself which allows the User to communicate and design the interface of different kinds without relying on any Third device.

The board has all the modern system modules peripherals like DAC, ADC, Audio port, UART, SPI, etc. which makes it one of the best-developing devices. The device May be for developing modern applications but some protocols will need to be Followed to use the device, like the compiler, voltage potential, etc.

The STM32F407xx family is based on the high-performance ARM Cortex-M432-bit RISC core with FPU operating at a frequency of upto72MHz, and embedding floating Point unit (FPU),a memory protection unit(MPU) and an embedded trace microcell (ETM). The family in corporates high-speed embedded memories (upto1Mbytes of Flash memory,upto 192Kbytes of RAM) and an extensive range of enhanced I/O's And peripherals connected to two APB buses.

They also feature standard and Advanced communication interfaces: up to two I2Cs, up to three SPIs(two SPIs are with Multiplexed full-duplex I2Ss), three USARTs, up to two UARTs, CAN and USB. To achieve audio class accuracy, the I2S peripherals can be clocked via an external PLL. The STM32F303xB/STM32F303xC family operates in the -40 to + 85。 C and -40 to +105。 C

Temperature ranges from a 2.0to3.6V power supply. A comprehensive set of power saving mode allows the design flow-Power application.



STM32F407VG DISCOVERY BOARD

3.1.1 Features

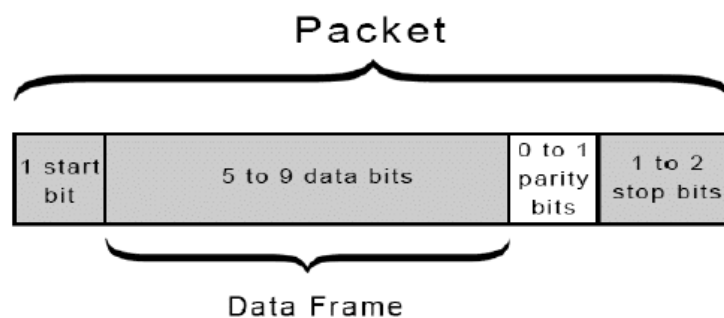
- STM32 Microcontroller with LQFP64 package.
- Two type of extension resources.
- 4LEDS.
- Two push buttons: USER and RESET.
- USB Re-enumeration capability: three different supported on USB, etc.

3.2 UART

This application note described how to implement an emulated universal asynchronous receiver transmitter (UART) on microcontroller of STM32F4 series. Such as emulation is needed in application that required more UARTs that's available on STM32F4 microcontrollers.

The UART is a full duplex asynchronous transmitter. It Supports up to 9 data bits and baud rates up to 115200 bps. It also can be used as Tx or Rx line. In addition, this UART emulator uses DMA to minimize CPU Usage.

The below given diagram describes the UART communication frame :-



The main features of the UART emulator are the following

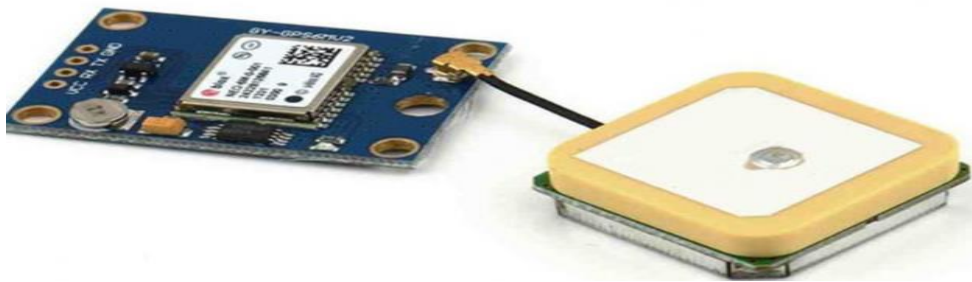
- Full- duplex asynchronous communication up to 11500 bps
- Programmable data word length: from 5 to 9 bits
- Flexible GPIO usage: all GPIOs can be configurable as UART_Tx/Rx
- Configurable number of stop bits: 1 or 2 stop bits
- Parity control
 - Transmission of parity bit
 - Parity check of received data frame
- Transfer detection flags
 - Receive complete
 - Transmit complete
- Error detection flags
 - Frame error
 - Parity error

3.3 GPS-neo6M

3.3.1 Description

GPS module (neo-6) which works on 2.4 GHz ISM band has 4 pins with following connections:

- VCC ----> 5V
- RX ----->TX (PA2 of STM32)
- TX ----->RX(PA3 of STM 32)
- GND-----> GND



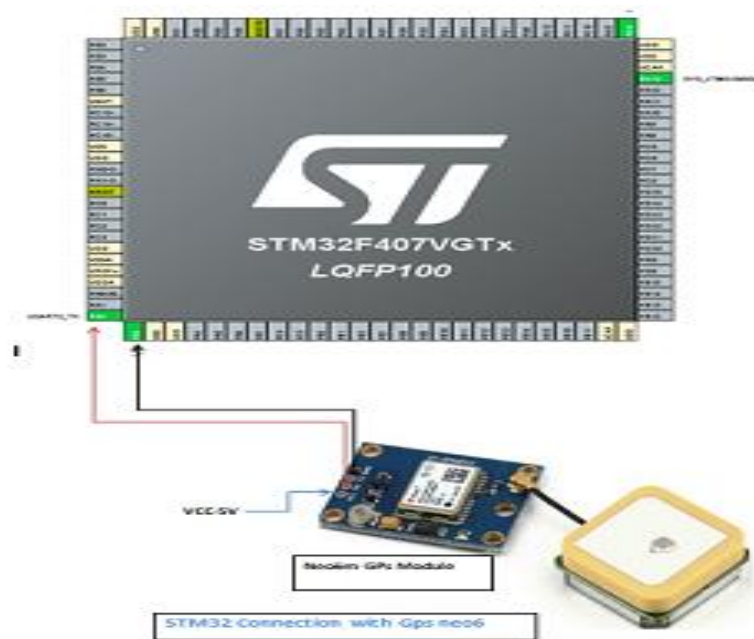
GPS-neo6M- Module Image

3.3.2 Communication

- NEO-6 modules include one configurable UART interface for serial communication.
- It provides a USB version 2.0 FS (Full Speed, 12Mbit/s) interface as an alternative to the UART. The pull-up resistor on USB_DP is integrated to signal a full-speed device to the host.
- SPI interface allows for the connection of external devices with a serial interface, e.g. serial flash to save configuration and Assist Now Offline A-GPS data or to interface to a host CPU. The interface can be operated in master or slave mode. In master mode, one chip select signal is available to select external slaves.
- In slave mode a single chip select signal enables communication with the host. Maximum bandwidth 100 kbits/s.

3.3.3 Antenna

- Antenna Type Passive and active antenna
- Active Antenna Recommendations
- Minimum gain 15 dB
- Maximum gain 50db
- Maximum noise figure 1.5dB



3.4 nRF24L01

About

The nRF24L01 is a single chip 2.4GHz transceiver with an embedded baseband protocol engine (Enhanced ShockBurst™), designed for ultra-low power wireless applications. The nRF24L01 is designed for operation in the world wide ISM frequency band at 2.400 - 2.4835GHz. An MCU (microcontroller) and very few external passive components are needed to design a radio system with the nRF24L01.

The nRF24L01 is configured and operated through a Serial Peripheral Interface (SPI.) Through this inter-face the register map is available. The register map contains all configuration registers in the nRF24L01 and is accessible in all operation modes of the chip.

The radio front end uses GFSK modulation. It has user configurable parameters like frequency channel, output power and air data rate.

The air data rate supported by the nRF24L01 is configurable to 2Mbps. The high air data rate combined with two power saving modes makes the nRF24L01 very suitable for ultra-low power designs.

Specifications

Radio

- Worldwide 2.4GHz ISM band operation
- 126 RF channels
- Common RX and TX pins
- GFSK modulation
- 1 and 2 Mbps air data rate
- 1MHz non-overlapping channel spacing at 1Mbps
- 2MHz non-overlapping channel spacing at 2Mbps

Transmitter

- Programmable output power: 0, -6, -12 or -18dBm
- 11.3mA at 0dBm output power

Receiver

- Integrated channel filters
- 12.3mA at 2Mbps
- -82dBm sensitivity at 2Mbps
- -85dBm sensitivity at 1Mbps
- Programmable LNA gain

Operating voltage: 3.3 volts (up to 5 volts)

Crystal Oscillator (MHz): 16

Range: up to 1000m

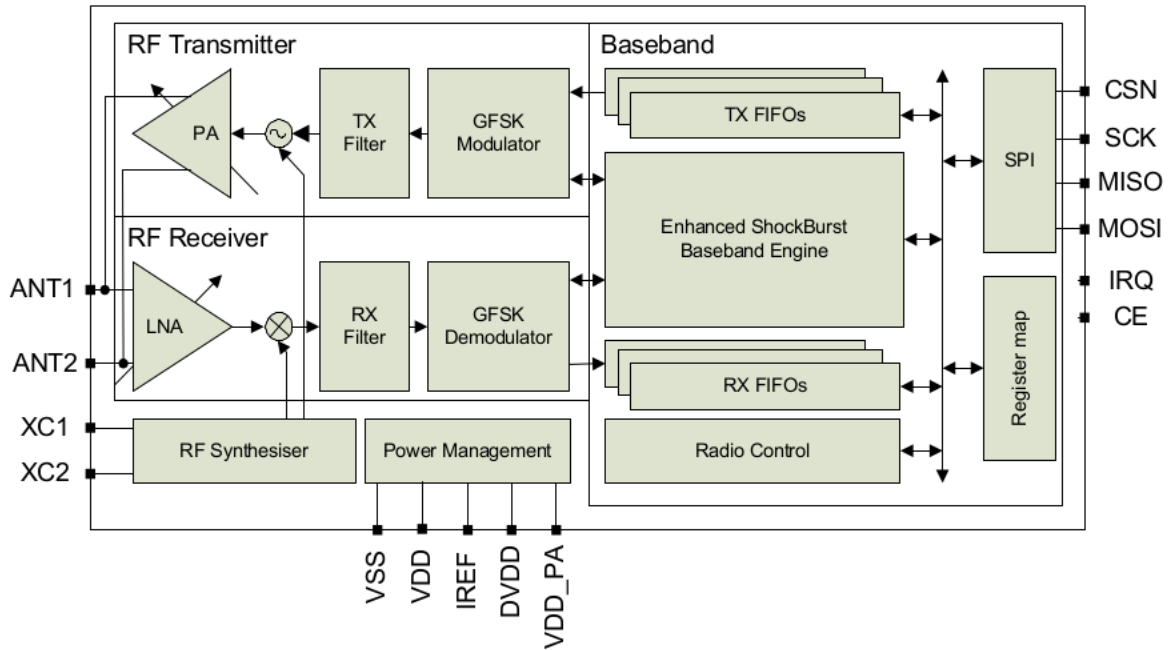


Figure 1. NRF24L01 block diagram

Operational Modes

RX mode: The RX mode is an active mode where the nRF24L01 radio is a receiver. To enter this mode, the nRF24L01 must have the PWR_UP bit set high, PRIM_RX bit set high and the CE pin set high.

TX Mode: The TX mode is an active mode where the nRF24L01 transmits a packet. To enter this mode, the nRF24L01 must have the PWR_UP bit set high, PRIM_RX bit set low, a payload in the TX FIFO and, a high pulse on the CE for more than 10µs.

Mode	PWR_UP register	PRIM_RX register	CE	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFO. Will empty all levels in TX FIFO ^a .
TX mode	1	0	minimum 10µs high pulse	Data in TX FIFO. Will empty one level in TX FIFO ^b .
Standby-II	1	0	1	TX FIFO empty
Standby-I	1	-	0	No ongoing packet transmission
Power Down	0	-	-	-

Figure 2. Mode operation selection

RF channel frequency

The RF channel frequency determines the centre of the channel used by the nRF24L01. The channel occupies a bandwidth of 1MHz at 1Mbps and 2MHz at 2Mbps. nRF24L01 can operate on frequencies from 2.400GHz to 2.525GHz. The resolution of the RF channel frequency setting is 1MHz.

At 2Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2Mbps mode, the channel spacing must be 2MHz or more. At 1Mbps the channel bandwidth is the same as the resolution of the RF frequency setting.

The RF channel frequency is set by the RF_CH register according to the following formula:

$$F0 = 2400 + \text{RF_CH [MHz]}$$

A transmitter and a receiver must be programmed with the same RF channel frequency to be able to communicate with each other.

RX/TX control

The RX/TX control is set by PRIM_RX bit in the CONFIG register and sets the nRF24L01 in transmit/receive.

Data Frame

Preamble 1 byte	Address 3-5 byte	Packet Control Field 9 bit	Payload 0 - 32 byte	CRC 1-2 byte
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Figure 3. Data Frame

Multiceiver

Multiceiver is a feature used in RX mode that contains a set of 6 parallel data pipes with unique addresses. A data pipe is a logical channel in the physical RF channel. Each data pipe has its own physical address decoding in the nRF24L01.

The data pipes are enabled with the bits in the EN_RXADDR register. By default only data pipe 0 and 1 are enabled. Each data pipe address is configured in the RX_ADDR_PX registers.

Each pipe can have up to 5 byte configurable addresses Figure 2. Data pipe 0 has a unique 5 byte address. Data pipes 1-5 share the 4 most significant address bytes. The LSByte must be unique for all 6 pipes. Below mentioned is an example of how data pipes 0-5 are addressed.

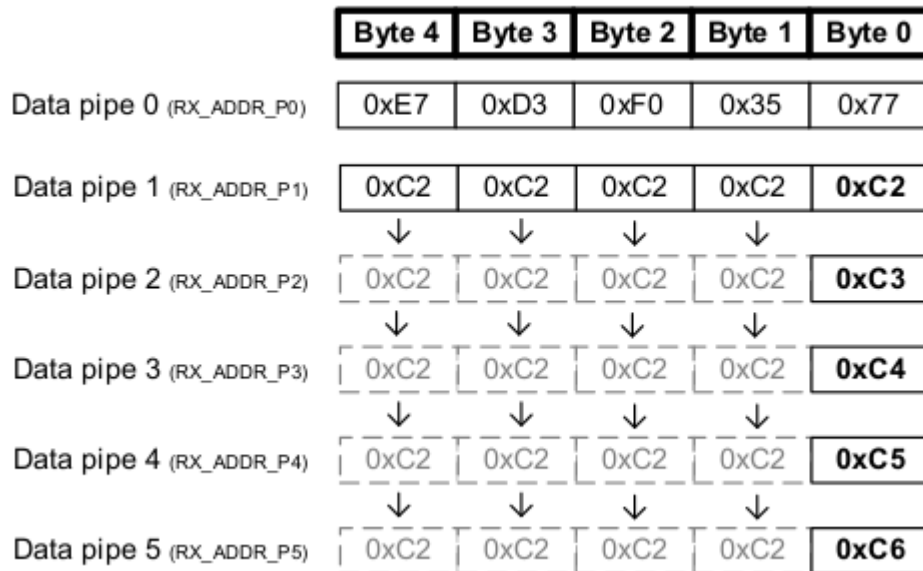


Figure 4. Addressing data pipes 0-5

Data and Control Interface

The data and control interface gives you access to all the features in the nRF24L01. The data and control interface consists of the following six 5 Volts tolerant digital signals:

- IRQ (this signal is active low and is controlled by three maskable interrupt sources)
- CE (this signal is active high and is used to activate the chip in RX or TX mode)
- CSN (SPI signal)
- SCK (SPI signal)
- MOSI (SPI signal)
- MISO (SPI signal)

You can use the SPI to activate the nRF24L01 data FIFOs or the register map by 1 byte SPI commands during all modes of operation.

Functional description

The SPI is a standard SPI with a maximum data rate of 8Mbps.

SPI Read Operation

Abbreviation	Description
Cn	SPI command bit
Sn	STATUS register bit
Dn	Data Bit (Note: LSByte to MSByte, MSBit in each byte first)



Figure 5: SPI Read operation

SPI Write Operation

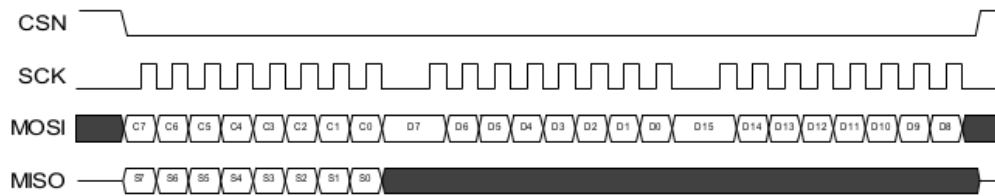
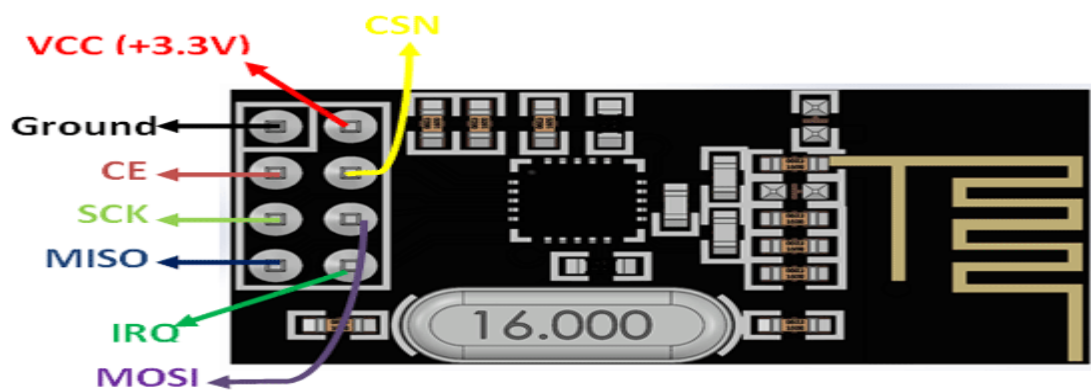


Figure 6: SPI Write operation



NRF24L01 Device pin configuration

SPI Commands

Command name	Command word (binary)	# Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSByte first	Read command and status registers. AAAA = 5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5 LSByte first	Write command and status registers. AAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32 LSByte first	Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed.
REUSE_TX_PL	1110 0011	0	Used for a PTX device Reuse last transmitted payload. Packets are repeatedly retransmitted as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission
ACTIVATE	0101 0000	1	This write command followed by data 0x73 activates the following features: <ul style="list-style-type: none"> • R_RX_PL_WID • W_ACK_PAYLOAD • W_TX_PAYLOAD_NOACK A new ACTIVATE command with the same data deactivates them again. <i>This is executable in power down or stand by mode s only.</i> The R_RX_PL_WID, W_ACK_PAYLOAD, and W_TX_PAYLOAD_NOACK features registers are initially in a deactivated state; a write has no effect, a read only results in zeros on MISO. To activate these registers, use the ACTIVATE command followed by data 0x73. Then they can be accessed as any other register in nRF24L01. Use the same command and data to deactivate the registers again.
R_RX_PL_WID ⁴	0110 0000		Read RX-payload width for the top R_RX_PAYLOAD in the RX FIFO.
W_ACK_PAYLOAD ⁴	1010 1PPP	1 to 32 LSByte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0.

Figure 7: SPI commands with operations

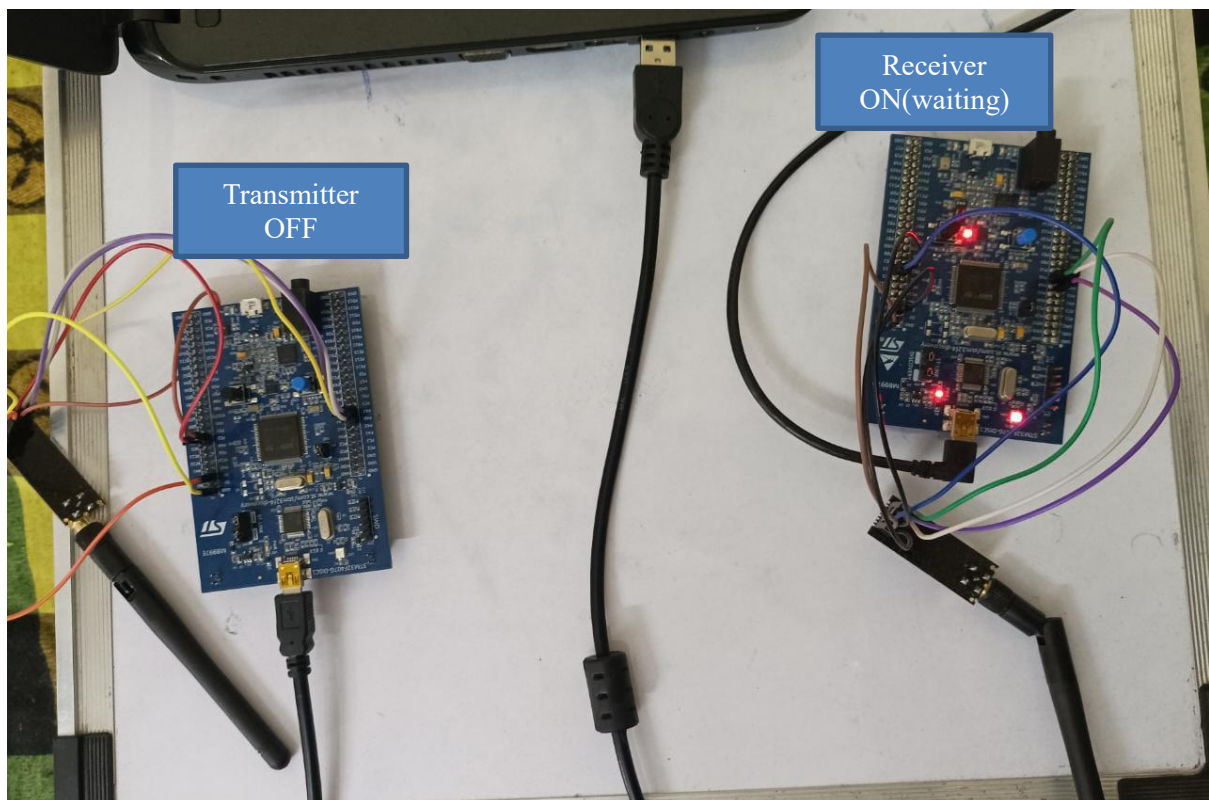
Chapter 4

Results and Analysis

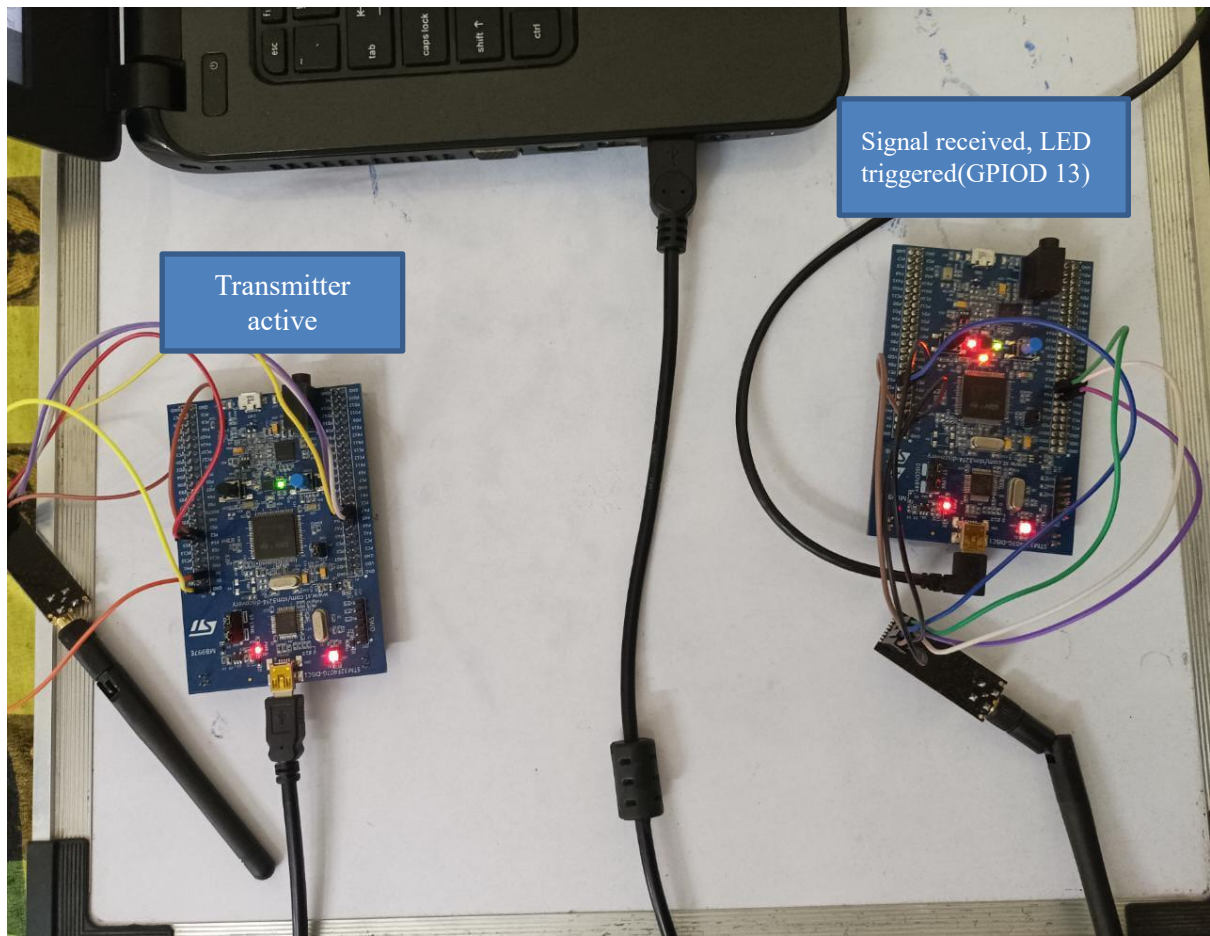
EV had the smooth passage through the traffic on roads which had straight traffic but on the junction, a delay can be observed if our EV is in 1st lane and a moment before arrival, opposite side traffic is waived green. In order to combat this, prior alert and live location is shared every time after reaching within calculated and proximity is maintained so that before waving the green signal, timer to wait will be flashed.

Junction traffic to be monitored and effort to be taken to mitigate in any abnormal vehicular motion. Intelligent traffic light system to be made equally stable. RF at traffic system needs to be sensitive to receive signal, generates an interrupt, alert the traffic and over write the current light with green thus pre-empting traffic light paving passage for EV.

Case 1: Transmitter is OFF and Receiver is waiting for signal



Case 2: Transmitter is active and within range, receiver alert traffic signal



Chapter 5

Challenges faced during project

- Through reference of datasheets was crucial so was the circuitry nevertheless we did it patiently.
- Receiving data via GPS was challenging too.
- Interfacing between ESP32 and STM32 was challenging.
- Creating, linking libraries files of respective sensors on STM cube ide .

Chapter6

Future Scope

Future work on EV may have potential developments like connected vehicle technology EV vehicles can directly communicate with other vehicles, notify of their presence thus reducing risk of accidents and make it easier to navigate through traffic.

With the ascent of technology, IoT sensors, cloud system, LoRa etc. can be incorporated where less manual involvement is perceived. Distributed edge computing based energy vehicle pre-emption system using IoT sensors.

Machine Learning and Artificial Intelligence integration will use real –time data to predict fastest and safest route thus avoiding major part of the traffic.

Local processing and control zone integration in smart cities. Under this, fast status updates, visualization on dashboard, event management optimization logic and further updating n cloud server. GPS based IoT use it as Dash Board Unit (DBU). DBU will send local data to nearby edge server every second. Technologies might be developed to find nearby edge server and send data which is needed. On receiving the data packets, edge server finds the direction, entry route and activates the green light on traffic signal controller which is connected to centralized cloud based traffic management system.

Another such can be dividing the cities in different zones based on the edge serves location.

Clustering techniques can be used to differentiate between zones and smooth handoff to be done without losing away the data. Once data received is done, established connection be continuously pinged to get latest data to nearest edge server.

Satellite view of networks of roads to studied, implementing camera and thermal sensors to get the actual intensity of traffic and which vehicle is causing ruckus to be identified. Street view of such roads to be noted and count of EV during day time, peak time can be recorded.

Chapter 7

Conclusion

We successfully implemented precedence passage of Emergency Vehicle through congestion and controlling traffic light to green of respective lane of emergency vehicle until it to navigate out. Those was done with the help of free RTOS for better CPU utilization and time bond and also for set different priority of task for different variety of vehicle depends on priority.

REFERENCES

- [1] Data sheets of nRF24L01
- [2] Neo6m GPS module
- [3] STM32f07 Reference Manual
- [4] ESP32 (Wi-Fi) Reference Manual
- [5] Communication Protocol (SPI, UART)
Link of TEXAS instrument reference of communication protocol
https://www.ti.com/lit/ug/sprugp1/sprugp1.pdf?ts=1678598923600&ref_url=https%253A%252F%252Fwww.google.com%252F
- [6] Hashim, Norlezah, Fakrulradzi Idris, Ahmad Fauzan Kadmin, and Siti Suhaila Jaapar Sidek. "Automatic traffic light controller for emergency vehicle using peripheral interface controller." *International Journal of Electrical and Computer Engineering* 9, no. 3 (2019): 1788.
- [7] Vani, R., Thendral, N., Kavitha, J.C. and Bhavani, N.P.G., 2018, December. Intelligent traffic control system with priority to emergency vehicles. In *IOP Conference Series: Materials Science and Engineering* (Vol. 455, No. 1, p. 012023). IOP Publishing.