SRK/KW/14/6959

Faculty of Engineering & Technology

Third Semester B.E. (Computer Science & Engineering) (CBS) Examination

COMPUTER ARCHITECTURE & ORGANIZATION

Paper—V

Time—Three Hours] [Maximum Marks 80

INSTRUCTIONS TO CANDIDATES

(1) All questions carry marks as indicated.

(2) Due credit will be given to neatness and adequate dimensions.

(3) Assume suitable data wherever necessary.

(4) Illustrate your answers wherever necessary with the help of neat sketches.

1. (a) Explain subroutine linkage and parameter passing methods with suitable example. 6

(b) Explain the following assembler commands :

(i) EQU

(ii) ORIGIN

(iii) DATA

(iv) START

(v) END. 5

(c) Define effective address and base address. 2

OR

2. (a) Explain the operation of Hardwired control unit with the help of suitable block diagram. 5

(b) Compare Hardwired control unit with Microprogrammed control unit. 3

(c) Define :

(i) Microprogram

(ii) Microinstruction

(iii) Microroutine

(iv) Control Word

(v) Control Store 5

3. (a) Using Booth's Algorithm solve :

(–18) * (9) 5

(b) Using Bit-pair recording of multipliers solve (+13) * (–6). 5

(c) Explain IEEE standard floating point format. 3

OR

4. (a) Solve the following using Restoring Division method :

23 ÷ 9 7

(b) Perform the following division using Non-restoring algorithm :

11101 DIV 0111 6

5. (a) Explain cache memories in detail and also explain different mapping techniques with diagram. 7

(b) Explain ROM, PROM, EPROM & EEPROM. 7

OR

6. (a) A block set associative cache consists of a total of 64 blocks divided in 4 blocks per set. The main memory contains 4096 blocks each of 128 words

(i) How many bits are there in main memory address ?

(ii) How many bits are there in each of the WORD, TAG and SET field ? 5

(b) Differentiate between static RAM vs Dynamic RAM. 4

(c) Design 8K × 8 bits RAM system using a 1K × 4 bits RAM IC's and appropriate decoders. 5

7. (a) Why handshaking signals are required in asynchronous data transfer ? Explain with a suitable example. 6

(b) Why are interrupts preferred over programmed IO ? Explain with an example. 7

OR

8. (a) What will be the total capacity of a hard disk having 8 sectors per pack, 32 tracks per surface, and

20 surfaces where each sector can store maximum 2 KB of data 5

(b) Describe various secondary storage devices used in computer systems 8

9. (a) What is a stall in a pipeline ? Why does it occur ? 5

(b) What is branch prediction ? Why it is used ? Give an example 9

OR

10. (a) Why sometimes in pipelined architecture, we delay branch ? Explain with a suitable example. 8

(b) What is pipelining ? What are interstage buffers ? Why are they required ? 6

11. (a) Why there is a need of multicore architecture ? With a suitable diagram explain how two cores coordinate in two-core architecture. 8

(b) What are multiprocessors ? 5

OR

12 Write short notes on

(a) Vector processors

(b) Array processors

(c) Flynn's classification of parallel structures 15