B.E. (Computer Science & Engineering) (New) Semester Third (C.B.S.)

Computer Architecture & Organization

Paper - V

P. Pages : 2 **KNT/KW/16/7241**

Time : Three Hours * 0 9 1 2 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) State and explain the various addressing modes. Give one example for each of the addressing modes. **7**

b) Explain how a shift register can be used as a control unit? Discuss it's limitations. **7**

OR

2. a) Convert below given arithmetic expression into a assembly language code segment using zero address, one address and two address instructions **7**

$$X = A * B + C * D$$

b) State the attributes of vertical and horizontal microinstructions formats. **4**

c) Discuss the advantages and disadvantages of single bus structure. **3**

3. a) Give the non - restoring integer division algorithm. Also draw the necessary circuit arrangement. **7**

b) Design a thirty two bit adder using four eight bit carry look ahead adders. State the advantage of this adder over thirty two bit ripple adder. **6**

OR

4. a) Perform the multiplication of $(+13)$ and (-6) using Booth multiplication method and bit pair recorded multiplier method. **7**

b) Explain, why bit pair recorded multiplier method of multiplication is better than Booth's multiplication method. **3**

c) Give single precision IEEE floating point format. **3**

5. a) Draw and explain the internal organisation of a static random access memory chip. **7**

b) Find the page hit and page fault ratio for the given page address stream using (i) Least recently used (ii) optimal page replacement policy. Assume four page buffers page address stream → 2, 3, 2, 1, 5, 2, 4, 5, 3, 2, 5, 2. **6**

OR

6. a) Consider a Cache consisting of 128 blocks of 16 words each and main memory of 64 K words. Explain the various mapping functions with reference to the above stated Cache. **7**

b) Explain the given below page replacement algorithm **6**
i) First In First Out
ii) Optimal
iii) Least recently used.

7. a) Explain I/O mapped I/O and memory mapped I/O. State the advantage of I/O mapped I/O over memory mapped I/O. **7**

b) Explain in detail the working principal of magnetic disk and it's physical structure. **6**

OR

8. a) Explain in detail the sequence of action taken by the microprocessor when it is interrupted. **7**

b) Draw and explain the organisation of data on magnetic tape. **6**

9. a) Draw a typical hardware for a four stage instruction pipelining and explain it. **7**

b) Write a short note on delayed branching. **7**

OR

10. a) Write a short note on branch prediction. **7**

b) Explain instruction queueing and prefetching with the help of necessary hardware organisation. **7**

11. a) Explain the loosely and tightly coupled multicomputer system. **7**

b) Draw and explain cross bar inter connection network. **6**

OR

12. a) Write a short note on array processors. **7**

b) Draw and explain single bus inter connection network. **6**

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