B.E. (Computer Science & Engineering (New)) Third Semester (C.B.S.)

Computer Architecture & Organization

P. Pages : 2 **NJR/KS/18/4381**

Time : Three Hours * 0 1 3 5 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) State & explain the various addressing modes. Give one example for each of the addressing modes. **7**

b) Write the set of instructions for solving the expression: **7**
$(A+B)*(C-D)$ using
a) Zero-address instruction
b) One-address instruction
c) Two-address instruction

OR

2. a) Differentiate between Hardwired control unit & microprogrammed control unit. **7**

b) Explain single bus structure & generate the control signal with the help of suitable example & diagram. **7**

3. a) Give the non-restoring integer division algorithm. Also draw the necessary circuit arrangement for the same & solve 10/3. **7**

b) Solve using Booth's algorithm. **7**
i) $13*6$.

OR

4. a) Represent the following number in single precision & double precision floating point format. **7**
a) 0.000125 b) 309.1875

b) Explain hardware for integer division. Divide 17 by 3 using restoring method. **7**

5. a) Consider a cache consisting of 128 blocks of 16 words each & main memory of 64k words. Explain the various mapping functions with reference to the above stated cache. **7**

b) Explain the concept of memory hierarchy & characteristics of memory systems. **6**

OR

6. a) Design the static RAM $128K \times 8$ RAM using $16K \times 2$ RAM chips/IC or static memory. **7**

b) Find the page hit & page fault ratio for the given page address stream using. **6**
i) Least recently used (LRU)
ii) Optimal
iii) First in first out page (FIFO) replacement algorithm. Assume three page buffers.
Page address stream:
2, 3, 2, 1, 5, 2, 4, 5, 3, 2, 5

7. a) Differentiate between IO mapped I/O & memory mapped I/O devices. **7**

b) Explain magnetic disk in detail. **6**

OR

8. a) Differentiate between synchronous & Asynchronous data transfer. **6**

b) Explain the concept of Interrupt with all its types. **7**

9. a) What is data hazards? Explain in detail with example. **7**

b) What is the concept of operand forwarding. **6**

OR

10. a) Explain the concept of delayed branch with 2-stage pipeline. **7**

b) Explain the concept of branch prediction with the help of neat diagram. **6**

11. a) What is the need of parallel processing? Explain the classification of parallel architecture. **7**

b) What is multicore architecture why there is a need of multicore architecture? **6**

OR

12. a) Write short note on following **any two.** **13**
i) Array Processor ii) Vector processor
iii) Multiprocessor

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