B.E. (Computer Science & Engineering (New)) Third Semester (C.B.S.)

Computer Architecture & Organization

P. Pages : 2 **NRJ/KW/17/4381**

Time : Three Hours * 0 5 1 1 * Max. Marks : 80

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Solve Question 11 OR Questions No. 12.
8. Due credit will be given to neatness and adequate dimensions.
9. Assume suitable data whenever necessary.
10. Illustrate your answers whenever necessary with the help of neat sketches.

1. a) Explain multiple bus architecture with the help of diagram. **7**

b) Explain how nested subroutine call is implemented using processor stack. **7**

OR

2. a) Explain different instruction format and write the following instruction into zero, one and two address instruction (A x B) + (A + D). **7**

b) Explain various addressing modes with examples which are used in instruction set design. **7**

3. a) Represent :- **6**

i) $(-450.725)_{10}$. ii) – 0.000125
iii) 3.295×10^2.
in double precision IEEE format.

b) Design a carry look ahead adder. **7**

OR

4. a) Solve the following by using Booth's algorithm. **6**
47 x – 3

b) Using restoring division method solve the following. **7**
11011 DIV 00111

5. a) A block set associative cache consist of a total of 64 blocks sets. The main memory contains 4096 blocks each consisting of 128 words. **7**

i) How many bits are there in a main memory address.

ii) How many bits are there in each of TAG, SET and WORD fields.

b) Write a short notes on multiple module memory system. **6**

OR

6. a) Write a note on paging and page table. **7**

b) Draw the block diagram to implement 8m x 32 memory using 512K x 8 memory chips. **6**

7. a) Explain interrupts with their types in detail. **7**

b) Differentiate between hard disk and floppy disk. **6**

OR

8. a) Explain direct memory access in detail. **7**

b) What is bus arbitration? Explain their type in detail with diagram. **6**

9. a) Explain instruction queue and prefetching with the help of necessary Hardware organization. **7**

b) What is super scalar operation? Explain with an example. **7**

OR

10. a) Explain data dependency in detail with an example. **7**

b) What is mean by Hazard? Explain all types of Hazard in detail. **7**

11. a) Draw and explain single bus inter connection network. **6**

b) Draw and explain the uniform and non uniform memory access multiprocessor system. **7**

OR

12. Write short notes on **any two.**

i) Array processor. **7**

ii) Vector processor. **6**

iii) Multi processor.

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