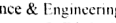
B.Tech. Third Semester (Computer Science & Engineering) (C.B.C.S.) Winter 2022

Computer Architecture & Digital System

P. Pages : 2

Time : Three Hours



SPM/KW/22/2532

Max. Marks : 70

Notes :
1. All questions carry marks as indicated.
2. Solve Question 1 OR Questions No. 2.
3. Solve Question 3 OR Questions No. 4.
4. Solve Question 5 OR Questions No. 6.
5. Solve Question 7 OR Questions No. 8.
6. Solve Question 9 OR Questions No. 10.
7. Due credit will be given to neatness and adequate dimensions.
8. Assume suitable data whenever necessary.

1. a) Define and draw NAND Gate, NOR Gate with their Truth table and Logic symbol. Why they are known as Universal Logic Gate. **7**

b) Reduce the expression using k - map $f = \sum m(0,1,3,5,7,8,9,10,12,13)$ and implement the real minimal expression in universal logic. **7**

OR

2. a) Implement the following logic function using an 8×1 MUX. $F(A,B,C,D) = \sum m(1,3,4,11,12,13,14,15)$. **7**

b) Obtain 4 – to – 16 decoder using 3 - to - 8 decoders with suitable logic diagram and function table. **7**

3. a) Explain Von Neuman Architecture in detail. **7**

b) What are the Instruction formats. Explain Two - Address and Three - Address Instruction. **7**

OR

4. a) What is addressing mode? Explain any six addressing modes. **8**

b) What are subroutines? Explain the execution sequence of nested subroutines. **6**

5. a) Define and explain the control sequence of execution of complete instruction. **7**

b) Write down the control sequence for fetching a word from memory using single bus organization. **7**

OR

6. a) Explain the difference between hardwired control unit and microprogrammed control unit with neat diagram. Illustrate the concept hardwired control associated with a control memory. **8**

b) Illustrate microinstruction format with example. **6**

7. a) Multiply $(-13) \times (+27)$ using Bit - pair coding (fast multiplication) method. **7**

b) Divide 31 by 8 using Restoring Division method. **7**

OR

8. a) Represent $-\frac{1}{16}$ and $\frac{1}{32}$ in IEEE single and Double Precision format. **8**

b) Multiply $(+13) \times (+6)$ using Booth's algorithm. **6**

9. a) What is virtual memory/ Describe address translation scheme in virtual memory. **7**

b) Design $4m \times 32$ memory using $512K \times 8$ static memory chip. **7**

OR

10. Explain **any four**. **14**

i) Page table.

ii) Associative memory.

iii) Synchronous data transfer.

iv) Interrupts handling mechanism.

v) Memory Interleaving.

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