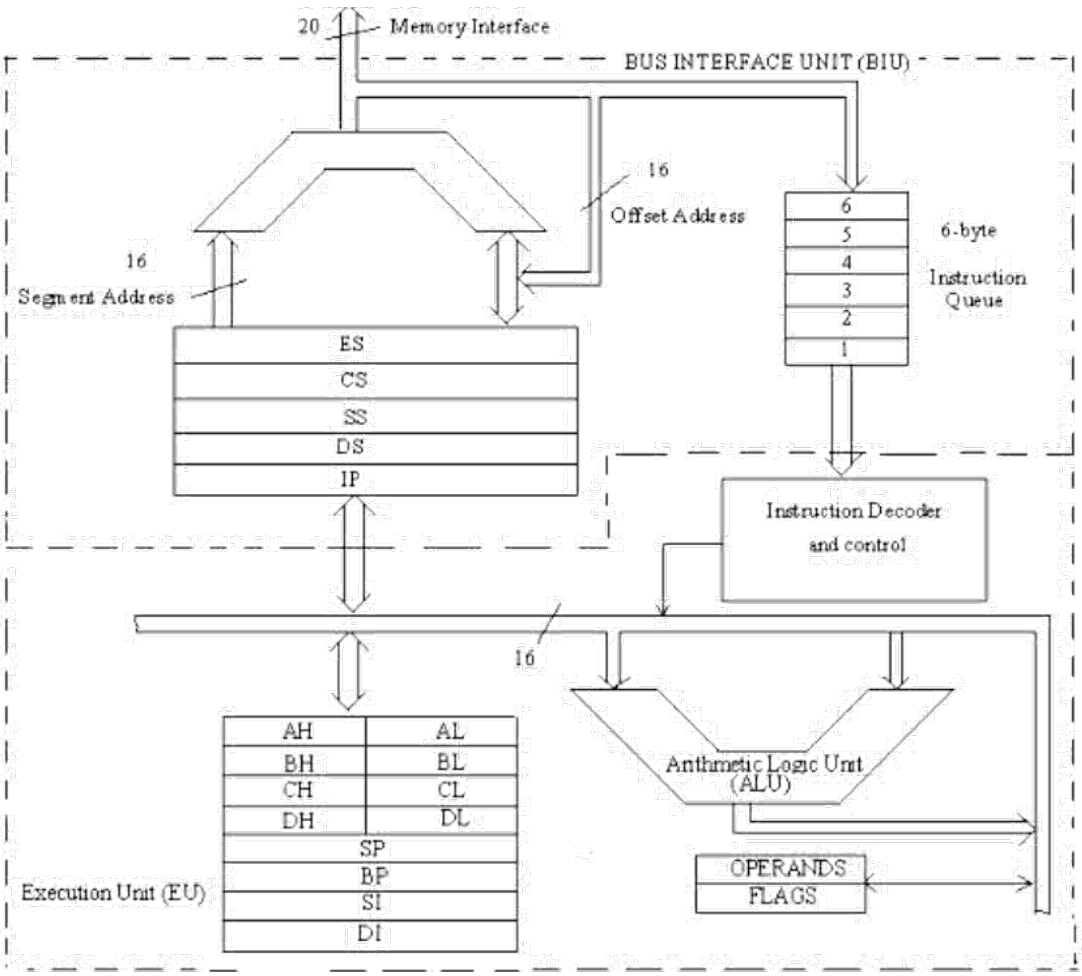
Unit III

Syllabus: 8086 Architecture: 8086 Architecture-Functional diagram, Register Organization, Memory Segmentation, Programming Model, Memory addresses, Physical Memory Organization, Architecture of 8086, Signal descriptions of 8086-Common Function Signals, Timing diagrams, Interrupts of 8086.

8086 Architecture :

Intel 8086 is a 16 bit integer processor. It has 16-bit data bus and 20-bit address bus. The lower 16-bit address lines and 16-bit data lines are multiplexed (AD0-AD15). Since 20-bit address lines are available, 8086 can access up to 2 20 or 1 Giga byte of physical memory.

The internal architecture of Intel 8086 is divided into two units, viz., Bus Interface Unit (BIU) and Execution Unit (EU).



Bus Interface Unit (BIU)

The Bus Interface Unit (BIU) generates the 20-bit physical memory address and

provides the interface with external memory (ROM/RAM). As mentioned earlier, 8086 has a single memory interface. To speed up the execution, 6-bytes of instruction are fetched in advance and kept in a 6-byte Instruction Queue while other instructions are being executed in the Execution Unit (EU). Hence after the execution of an instruction, the next instruction is directly fetched from the instruction queue without having to wait for the external memory to send the instruction. This is called pipe-lining and is helpful for speeding up the overall execution process.

8086's BIU produces the 20-bit physical memory address by combining a 16-bit segment address with a 16-bit offset address. There are four 16-bit segment registers, viz., the code segment (CS), the stack segment (SS), the extra segment (ES), and the data segment (DS). These segment registers hold the corresponding 16 -bit segment addresses. A segment address is the upper 16-bits of the starting address of that segment. The lower 4-bits of the starting address of a segment is always zero. The offset address is held by another 16-bit register. The physical 20-bit address is calculated by shifting the segment address 4-bit left and then adding that to the offset address.

For Example:

Code segment Register CS holds the segment address which is 4569 H Instruction pointer IP holds the offset address which is 10A0 H The physical 20-bit address is calculated as follows.

Segment address : 45690 H
Offset address : + 10A0 H
Physical address : 46730 H

Register Organization

The registers AX, BX, CX, and DX are the general 16-bit registers.

AX Register: Accumulator register consists of two 8-bit registers AL and AH, which can be combined together and used as a 16- bit register AX. AL in this case contains the low-order byte of the word, and AH contains the high-order byte. Accumulator can be used for I/O operations, rotate and string manipulation.

BX Register: This register is mainly used as a base register. It holds the starting base location of a memory region within a data segment. It is used as offset storage for forming physical address in case of certain addressing mode.

CX Register: It is used as default counter or count register in case of string and loop instructions.

DX Register: Data register can be used as a port number in I/O operations and

implicit operand or destination in case of few instructions. In integer 32-bit multiply and divide instruction the DX register contains high-order word of the initial or resulting number.

Segment registers:

To complete 1Mbyte memory is divided into 16 logical segments. The complete 1Mbyte memory segmentation is as shown in fig 1.5. Each segment contains 64Kbyte of memory. There are four segment registers.

Code segment (CS) is a 16-bit register containing address of 64 KB segment with processor instructions. The processor uses CS segment for all accesses to instructions referenced by instruction pointer (IP) register. CS register cannot be changed directly. The CS register is automatically updated during far jump, far call and far return instructions. It is used for addressing a memory location in the code segment of the memory, where the executable program is stored.

Stack segment (SS) is a 16-bit register containing address of 64KB segment with program stack. By default, the processor assumes that all data referenced by the stack pointer (SP) and base pointer (BP) registers is located in the stack segment. SS register can be changed directly using POP instruction. It is used for addressing stack segment of memory. The stack segment is that segment of memory, which is used to store stack data.

Data segment (DS) is a 16-bit register containing address of 64KB segment with program data. By default, the processor assumes that all data referenced by general registers (AX, BX, CX, DX) and index register (SI, DI) is located in the data segment. DS register can be changed directly using POP and LDS instructions. It points to the data segment memory where the data is resided.

Extra segment (ES) is a 16-bit register containing address of 64KB segment, usually with program data. By default, the processor assumes that the DI register references the ES segment in string manipulation instructions. ES register can be changed directly using POP and LES instructions. It also refers to segment which essentially is another data segment of the memory. It also contains data.

Pointers and index registers.

The pointers contain within the particular segments. The pointers IP, BP, SP usually contain offsets within the code, data and stack segments respectively

Stack Pointer (SP) is a 16-bit register pointing to program stack in stack segment.

Base Pointer (BP) is a 16-bit register pointing to data in stack segment. BP register is usually used for based, based indexed or register indirect addressing.

Source Index (SI) is a 16-bit register. SI is used for indexed, based indexed and register indirect addressing, as well as a source data addresses in string

manipulation instructions.

Destination Index (DI) is a 16-bit register. DI is used for indexed, based indexed and register indirect addressing, as well as a destination data address in string manipulation instructions.

Conditional Flags

Conditional flags are as follows:

Carry Flag (CY): This flag indicates an overflow condition for unsigned integer arithmetic. It is also used in multiple-precision arithmetic.

Auxiliary Flag (AC): If an operation performed in ALU generates a carry/barrow from lower nibble (i.e. D0 – D3) to upper nibble (i.e. D4 – D7), the AC flag is set i.e. carry given by D3 bit to D4 is AC flag. This is not a general-purpose flag, it is used internally by the Processor to perform Binary to BCD conversion.

Parity Flag (PF): This flag is used to indicate the parity of result. If lower order 8-bits of the result contains even number of 1's, the Parity Flag is set and for odd number of 1's, the Parity flag is reset.

Zero Flag (ZF): It is set; if the result of arithmetic or logical operation is zero else it is reset.

Sign Flag (SF): In sign magnitude format the sign of number is indicated by MSB bit. If the result of operation is negative, sign flag is set.

Control Flags

Control flags are set or reset deliberately to control the operations of the execution unit.

Control flags are as follows:

Trap Flag (TF): It is used for single step control. It allows user to execute one instruction of a program at a time for debugging. When trap flag is set, program can be run in single step mode.

Interrupt Flag (IF): It is an interrupt enable/disable flag. If it is set, the maskable interrupt of 8086 is enabled and if it is reset, the interrupt is disabled. It can be set by executing instruction sit and can be cleared by executing CLI instruction.

Direction Flag (DF): It is used in string operation. If it is set, string bytes are accessed from higher memory address to lower memory address. When it is reset, the string bytes are accessed from lower memory address to higher memory address.

8086 Programmer's Model

ES
CS
SS
DS
IP

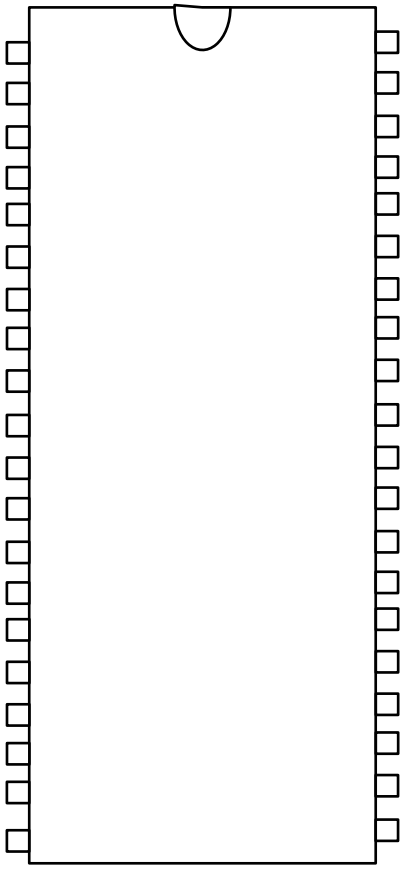
AH	AL
BH	BL
CH	CL
DH	DL
SP	
BP	
SI	
DI	
FLAGS	

Memory Segmentation

In memory the data is stored as bytes. Each byte considered as memory location. (Here study about segment registers which is discussed above)

Signal Descriptions of 8086

Important 8086 Pin Diagram/Description



The 8086 Microprocessor is a 16-bit CPU available in 3 clock rates, i.e. 5, 8 and 10MHz, packaged in a 40 pin CERDIP or plastic package. The 8086 Microprocessor operates in single processor or multiprocessor configurations to achieve high performance. The pin configuration is as shown in fig1. Some of the pins serve a particular function in minimum mode (single processor mode) and others function in maximum mode (multiprocessor mode) configuration.

The 8086 signals can be categorized in three groups. The first are the signals having common functions in minimum as well as maximum mode, the second are the signals which have special functions in minimum mode and third are the signals having special functions for maximum mode

The following signal descriptions are **common** for both the **minimum and maximum modes**.

AD15-AD0: These are the time multiplexed memory I/O address and data lines. Address remains on the lines during T1 state, while the data is available on the data bus during T2, T3, TW and T4. Here T1, T2, T3, T4 and TW are the clock states of a machine cycle. TW is a wait state. These lines are active high and float to a tristate during interrupt acknowledge and local bus hold acknowledge cycles.

A19/S6, A18/S5, A17/S4, A16/S3: These are the time multiplexed address and status lines. During T1, these are the most significant address lines or memory operations. During I/O operations, these lines are low. During memory or I/O operations, status information is available on those lines for T2, T3, TW and T4 .The status of the interrupt enable flag bit(displayed on S5) is updated at the beginning of each clock cycle. The S4 and S3 combinedly indicate which segment register is presently being used for memory accesses as shown in Table below.

S4	S3	Indication
0	0	Alternate Data
0	1	Stack
1	0	Code or none
1	1	Data

These lines float to tri-state off (tristated) during the local bus hold acknowledge. The status line S6 is always low (logical). The address bits are separated from the status bits using latches controlled by the ALE signal.

BHE/S7-Bus High Enable/Status: The bus high enable signal is used to indicate the transfer of data over the higher order (D15-D8) data bus as shown in Table below. It goes low for the data transfers over D15-D8 and is used to derive chip selects of odd address memory bank or peripherals. BHE is low during T1 for read, write and interrupt acknowledge cycles, when- ever a byte is to be transferred on the higher byte of the data bus. The status information is available during T2, T3 and T4. The signal is active low and is tri-stated during 'hold'. It is low during T1 clock pulse of the interrupt acknowledges.

BHE	A0	Indication
0	0	Whole Word
0	1	Upper Byte from or to odd address
1	0	Lower Byte from or to Even address
1	1	None

RD: Read: Read signal, when low, indicates the peripherals that the processor is performing a memory or I/O read operation. RD is active low and shows the state for

T2, T3, TW of any read cycle. The signal remains tri-stated during the 'hold acknowledge'.

READY: This is the acknowledgement from the slow devices or memory that they have completed the data transfer.

INTR: Interrupt Request: This is a level triggered input. This is sampled during the last clock cycle of each instruction to determine the availability of the request. If any interrupt request is pending, the processor enters the interrupt acknowledge cycle. This can be internally masked by resetting the interrupt enable flag. This signal is active high and internally synchronized.

TEST: This input is examined by a 'WAIT' instruction. If the TEST input goes low, execution will continue, else, the processor remains in an idle state. The input is synchronized internally during each clock cycle on leading edge of clock.

NMI: Non-maskable Interrupt: This is an edge-triggered input which causes a Type2 interrupt. The NMI is not maskable internally by software. A transition from low to high initiates the interrupt response at the end of the current instruction. This input is internally synchronized.

RESET: This input causes the processor to terminate the current activity and start execution from FFFF0H. The signal is active high and must be active for at least four clock cycles. It restarts execution when the RESET returns low. RESET is also internally synchronized.

CLK: Clock Input: The clock input provides the basic timing for processor operation and bus control activity. Its an asymmetric square wave with 33% duty cycle. The range of frequency for different 8086 versions is from 5MHz to 10MHz.

VCC: +5V power supply for the operation of the internal circuit. GND ground for the internal circuit.

MN/MX: The logic level at this pin decides whether the processor is to operate in either minimum (single processor) or maximum (multiprocessor) mode.

The following pin functions are for the minimum mode operation of 8086.

M/IO -Memory/IO: This is a status line logically equivalent to S2 in maximum mode. When it is low, it indicates the CPU is having an I/O operation, and when it is high, it indicates that the CPU is having a memory operation. This line becomes active in the previous T4 and remains active till final T4 of the current cycle. It is tri-stated during local bus "hold acknowledge".

INTA: Interrupt Acknowledge: This signal is used as a read strobe for interrupt acknowledge cycles. In other words, when it goes low, it means that the processor has accepted the interrupt. It is active low during T2, T3 and TW of each interrupt acknowledge cycle.

ALE-Address latch Enable: This output signal indicates the availability of the valid address on the address/data lines, and is connected to latch enable input of latches. This signal is active high and is never tri-stated.

DT /R -Data Transmit/Receive: This output is used to decide the direction of data flow through the transceivers (bidirectional buffers). When the processor sends out data, this signal is high and when the processor is receiving data, this signal is low. Logically, this is equivalent to S1 in maximum mode. Its timing is the same as M/I/O. This is tri-stated during 'hold acknowledge'.

DEN-Data Enable: This signal indicates the availability of valid data over the address/data lines. It is used to enable the transceivers (bidirectional buffers) to separate the data from the multiplexed address / data signal. It is active from the middle ofT2 until the middle of T4 DEN is tri-stated during 'hold acknowledge' cycle.

HOLD, HLDA-Hold/Hold Acknowledge: When the HOLD line goes high it indicates to the processor that another master is requesting the bus access. The processor, after receiving the HOLD request, issues the hold acknowledge signal on HLDA pin, in the middle of the next clock cycle after completing the current bus (instruction) cycle. At the same time, the processor floats the local bus and control lines. When the processor detects the HOLD line low, it lowers the HLDA signal. HOLD is an asynchronous input, and it should be externally synchronized. If the DMA request is made while the CPU is performing a memory or I/O cycle, it will release the local bus during T 4 provided:

1. The request occurs on or before T 2 state of the current cycle.

2. The current cycle is not operating over the lower byte of a word (or operating on an odd address).

3. The current cycle is not the first acknowledge of an interrupt acknowledge sequence.

4. A Lock instruction is not being executed.

The following pin functions are applicable for maximum mode operation of 8086.

S2, S1, S0 -Status Lines: These are the status lines which reflect the type of operation, being carried out by the processor. These become active during T4 of the previous cycle and remain active during T1 and T2 of the current bus cycle. The status lines return to passive state during T3 of the current bus cycle so that they may again become active for the next bus cycle during T4. Any change in these lines during T3 indicates the starting of a new cycle, and return to passive state indicates end of the bus cycle. These status lines are encoded in table below.

S2	S1	S0	Indication
0	0	0	Interrupt Acknowledge

0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read Memory
1	1	0	Write memory
1	1	1	Passive

LOCK: This output pin indicates that other system bus masters will be prevented from gaining the system bus, while the LOCK signal is low. The LOCK signal is activated by the 'LOCK' prefix instruction and remains active until the completion of the next instruction. This floats to tri-state off during "hold acknowledge". When the CPU is executing a critical instruction which requires the system bus, the LOCK prefix instruction ensures that other processors connected in the system will not gain the control of the bus. The 8086, while executing the prefixed instruction, asserts the bus lock signal output, which may be connected to an external bus controller.

QS1, QS0-Queue Status: These lines give information about the status of the code prefetch queue. These are active during the CLK cycle after which the queue operation is performed. These are encoded as shown in Table below.

QS1	QS0	Indication
0	0	No Operation
0	1	First byte of opcode from the queue
1	0	Empty Queue
1	1	Subsequent byte from the queue

This modification in a simple fetch and execute architecture of a conventional microprocessor offers an added advantage of pipelined processing of the instructions. The 8086 architecture has a 6-byte instruction prefetch queue. Thus even the largest (6- bytes) instruction can be prefetched from the memory and stored in the prefetch queue. This results in a faster execution of the instructions. This scheme is known as instruction pipelining. At the starting the CS:IP is loaded

with the required address from which the execution is to be started. Initially, the queue will be empty and the microprocessor starts a fetch operation to bring one byte (the first byte) of instruction code, if the CS:IP address is odd or two bytes at a time, if the CS:IP address is even. The first byte is a complete opcode in case of some instructions (one byte opcode instruction) and it is a part of opcode, in case of other instructions (two byte long opcode instructions), the remaining part of opcode may lie in the second byte. But invariably the first byte of an instruction is an opcode. These opcodes along with data are fetched and arranged in the queue. When the first byte from the queue goes for decoding and interpretation, one byte in the queue becomes empty and subsequently the queue is updated. The microprocessor does not perform the next fetch operation till at least two bytes of the instruction queue are emptied. The instruction execution cycle is never broken for fetch operation. After decoding the first byte, the decoding circuit decides whether the instruction is of single opcode byte or double opcode byte. If it is single opcode byte, the next bytes are treated as data bytes depending upon the decoded instruction length otherwise, the next byte in the queue is treated as the second byte of the instruction opcode. The second byte is then decoded in continuation with the first byte to decide the instruction length and the number of subsequent bytes to be treated as instruction data. The queue is updated after every byte is read from the queue but the fetch cycle is initiated by BIU only if at least, two bytes of the queue are empty and the EU may be concurrently executing the fetched instructions. The next byte after the instruction is completed is again the first opcode byte of the next instruction. A similar procedure is repeated till the complete execution of the program. The main point to be noted here is that the fetch operation of the next instruction is overlapped with the execution of the current instruction. As shown in the architecture, there are two separate units, namely, execution unit and bus interface unit. While the execution unit is busy in executing an instruction, after it is completely decoded, the bus interface unit may be fetching the bytes o(the next instruction from memory, depending upon the queue status.

RQ/GT0, RQ/GT1-ReQuest/Grant: These pins are used by other local bus masters, in maximum mode, to force the processor to release the local bus at the end of the processor's current bus cycle. Each of the pins is bidirectional with RQ/GT0 having higher priority than RQ/ GT1, RQ/GT pins have internal pull-up resistors and may be left unconnected. The request grant sequence is as follows:

1. A pulse one clock wide from another bus master requests the bus access to 8086.

2. During T4 (current) or T1 (next) clock cycle, a pulse one clock wide from 8086 to the requesting master, indicates that the 8086 has allowed the local bus to float and that it will enter the "hold acknowledge" state at next clock cycle. The CPU's bus interface unit is likely to be disconnected from the local bus of the system.

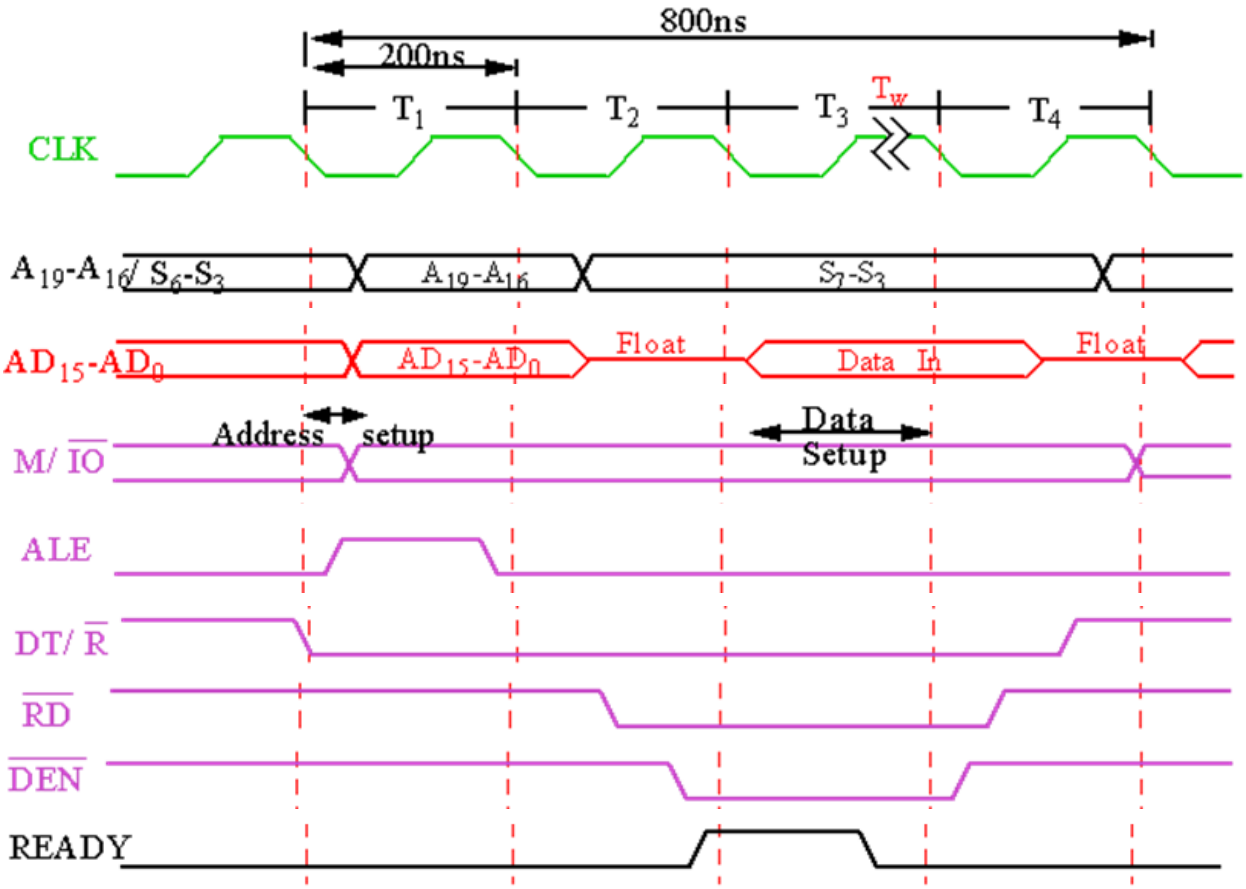
3. A one clock wide pulse from the another master indicates to 8086 that the 'hold' request is about to end and the 8086 may regain control of the local bus at the next

clock cycle.

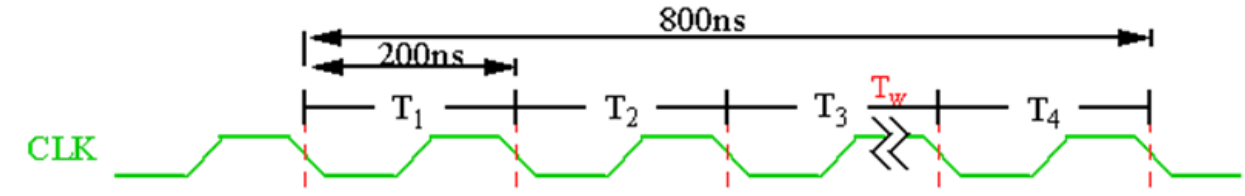
Thus each master to master exchange of the local bus is a sequence of 3 pulses. There must be at least one dead clock cycle after each bus exchange. The request and grant pulses are active low. For the bus requests those are received while 8086 is performing memory or I/O cycle, the granting of the bus is governed by the rules as discussed i~ case of HOLD, and HLDA in minimum mode.

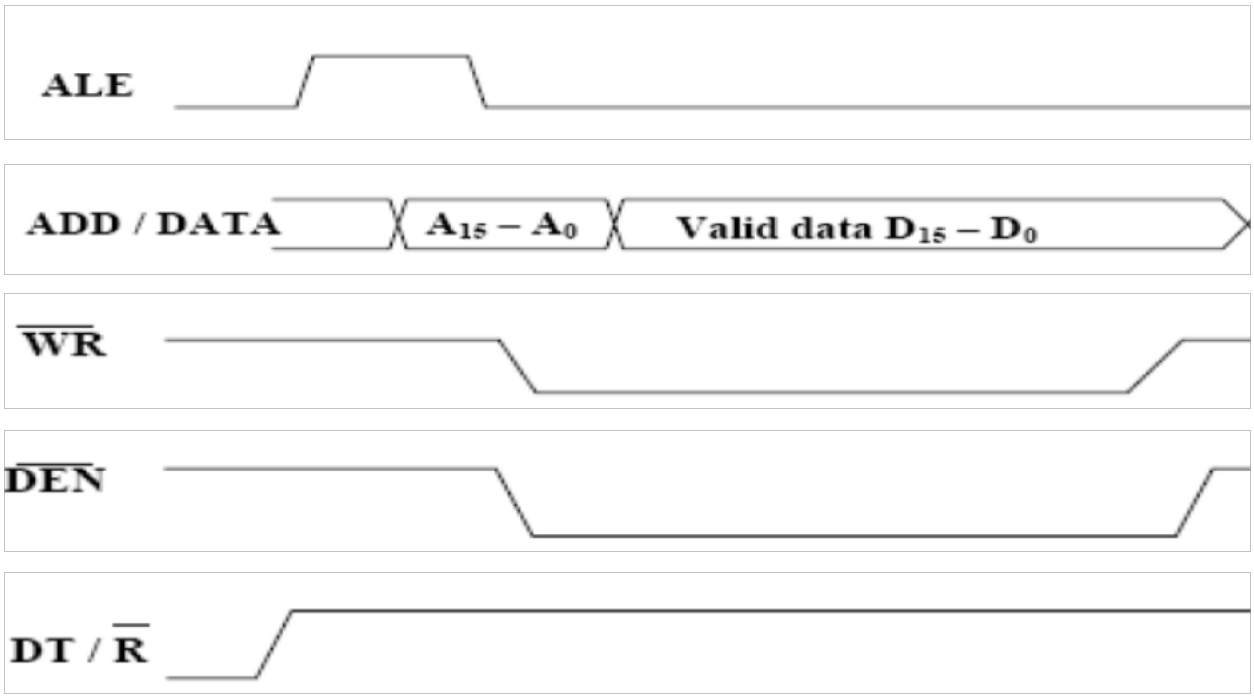
Timing Diagram:

Minimum Mode timing diagram Read operation

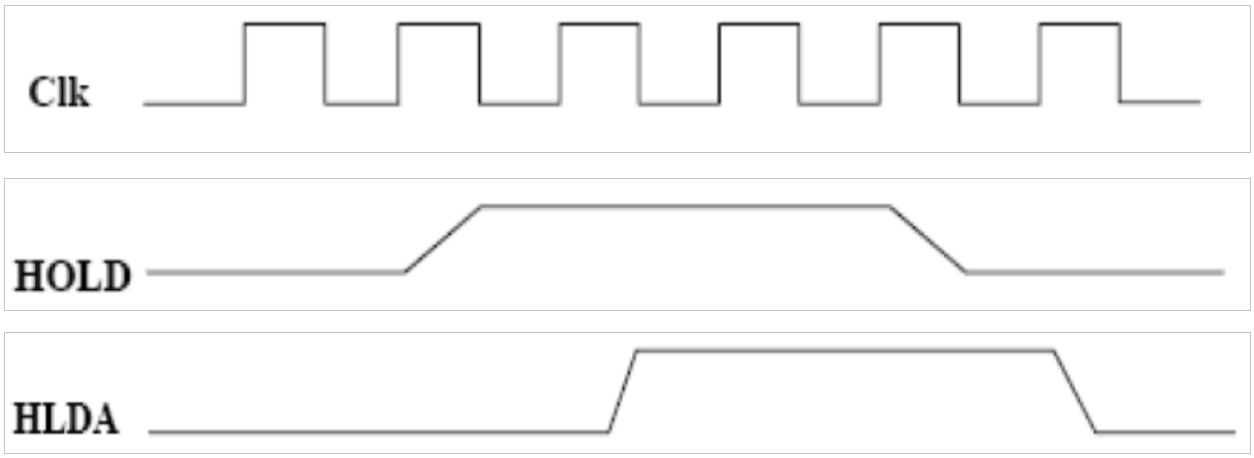


Minimum Mode timing diagram Write operation

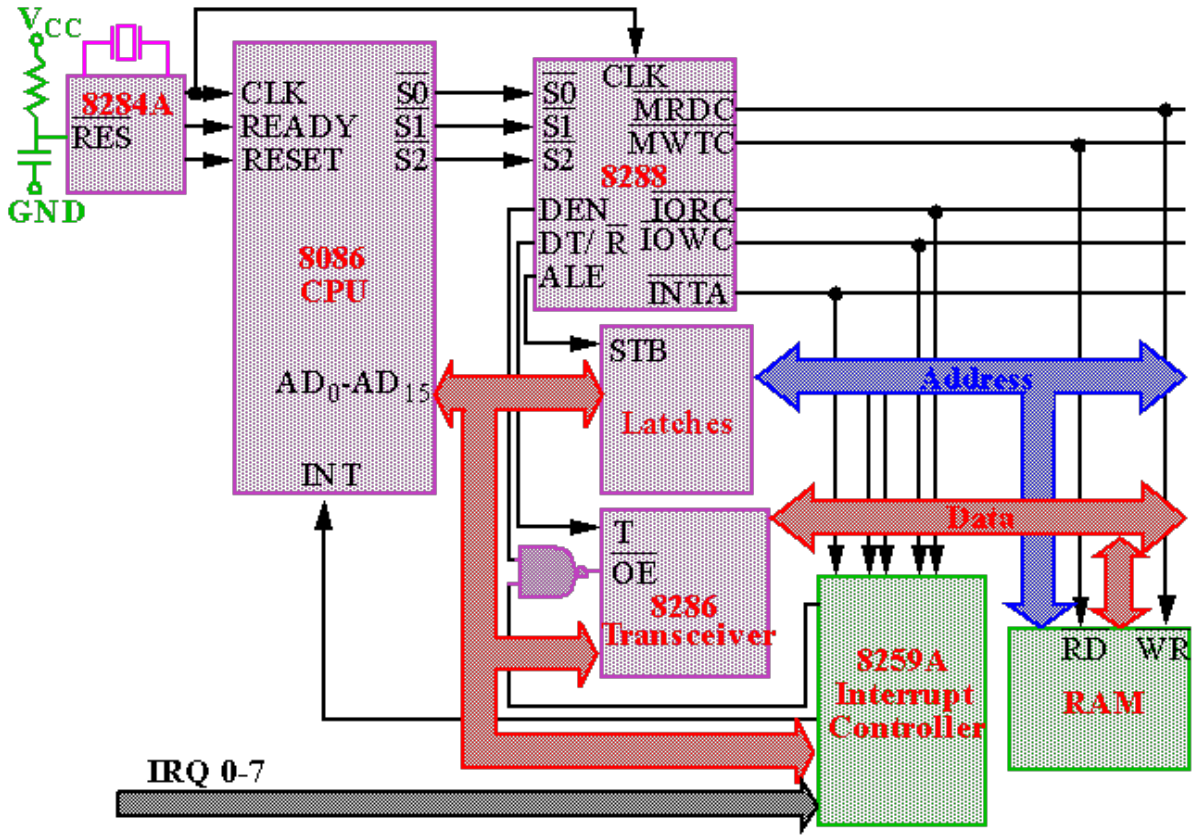




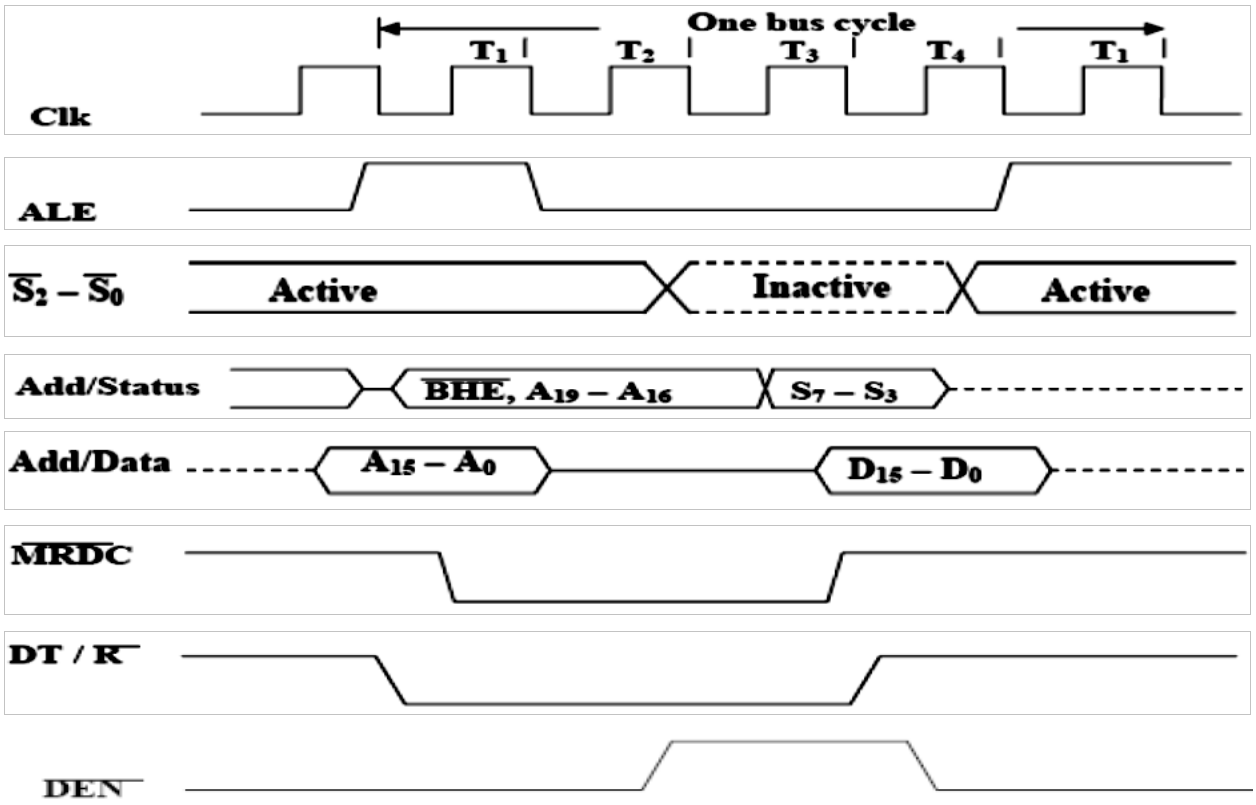
Hold response in min. mode



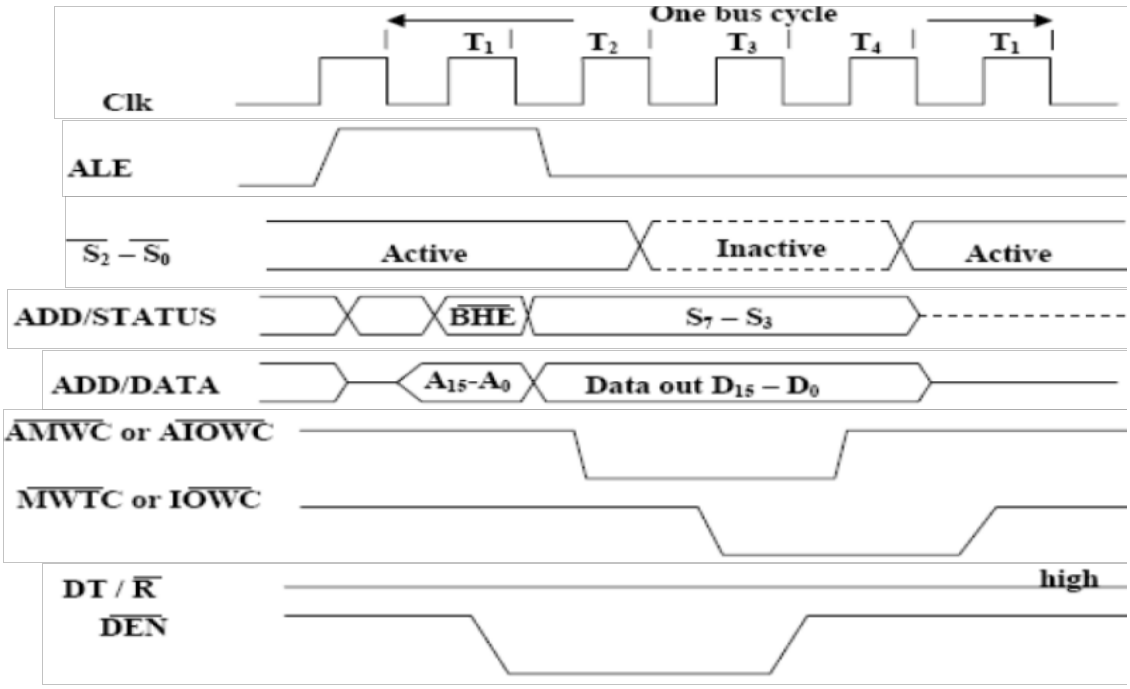
Maximum mode of 8086



Maximum mode Memory Read Operation



Maximum mode Write Operation



Interrupts of 8086

Interrupt Types

Hardware Interrupts: External event

Software Interrupts: Internal event (Software generated)

Maskable and non-maskable interrupts

Interrupt priority

Interrupt Vectors and Interrupt Handlers

Interrupt Controllers

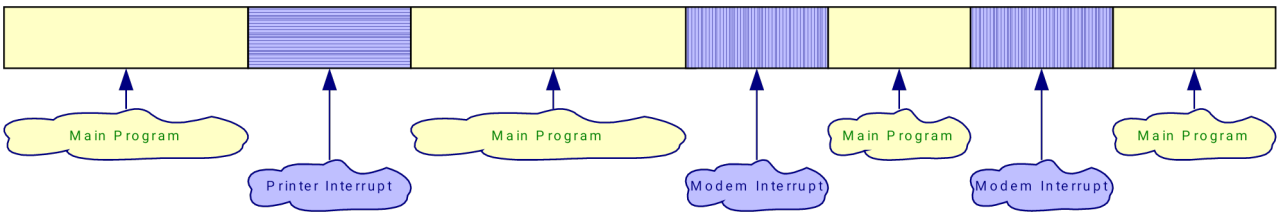
The Purpose of Interrupts

Interrupts are useful when interfacing I/O devices with low data-transfer rates, like a keyboard or a mouse, in which case polling the device wastes valuable processing time

The peripheral interrupts the normal application execution, requesting to send or receive data.

The processor jumps to a special program called *Interrupt Service Routine* to service the peripheral

After the processor services the peripheral, the execution of the interrupted program continues.



Interrupt pins: Set of pins used in hardware interrupts

Interrupt Service Routine (ISR) or Interrupt handler: code used for handling a specific interrupt

Interrupt priority: In systems with more than one interrupt inputs, some interrupts have a higher priority than other

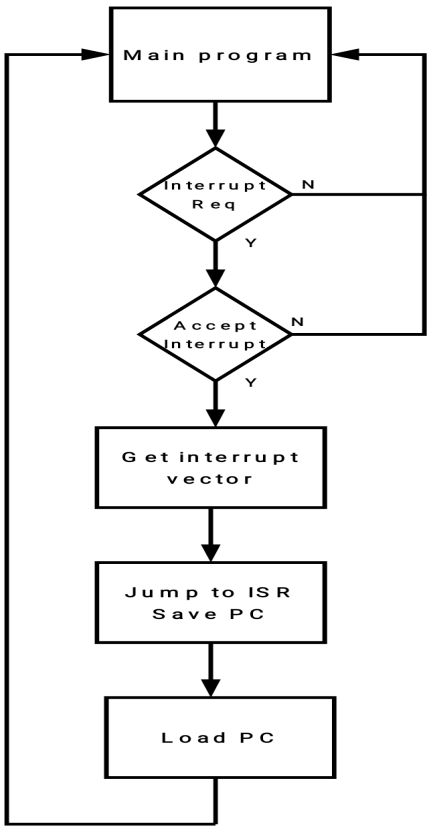
They are serviced first if multiple interrupts are triggered simultaneously

Interrupt vector: Code loaded on the bus by the interrupting device that contains the Address (segment and offset) of specific interrupt service routine

Interrupt Masking: Ignoring (disabling) an interrupt

Non-Maskable Interrupt: Interrupt that cannot be ignored (power-down)

Interrupt processing flow



Interrupt Vectors

The processor uses the interrupt vector to determine the address of the ISR of the interrupting device.

In the 8088/8086 processor as well as in the 80386/80486/Pentium processors operating in Real Mode (16-bit operation), the interrupt vector is a pointer to the Interrupt Vector Table.

The Interrupt Vector Table occupies the address range from 00000H to 003FFH (the first 1024 bytes in the memory map).

Each entry in the Interrupt Vector Table is 4 bytes long:

The first two represent the offset address and the last two the segment address of the ISR.

The first 5 vectors are reserved by Intel to be used by the processor.

The vectors 5 to 255 are free to be used by the user.

The *Interrupt Vector* contains the address of the interrupt service routine

The *Interrupt Vector Table* is located in the first 1024 bytes of memory at address 000000H-0003FFH.

It contains 256 different 4-byte interrupt vectors, grouped in 18 types

000H: Type 0 (Divide error)

004H: Type 1 (Single-step)

008H: Type 2 (NMI)

00CH: Type 3 (1-byte breakpoint)

010H: Type 4 (Overflow)

014H: Type 5 (BOUND)

018H: Type 6 (Undefined opcode)

01CH: Type 7 (Coprocessor not available)

020H: Type 8 (Double fault)

024H: Type 9 (Coprocessor segment overrun)

028H: Type 10 (Invlid task state segment)

02CH: Type 11 (Segment not present)

030H: Type 12 (Stack segment overrun)

034H: Type 13 (General protection)

038H: Type 14 (Page fault)

03CH: Type 15 (Unassigned)

040H: Type 16 (Coprocessor error)

044H-07CH: Type 14-31 (Reserved)

080H: Type 32-255 (User)

1. Type 0: Divide error – Division overflow or division by zero
2. Type 1: Single step or Trap – After the execution of each instruction when trap flag set
3. Type 2: NMI Hardware Interrupt – '1' in the NMI pin
4. Type 3: One-byte Interrupt – INT3 instruction (used for breakpoints)
5. Type 4: Overflow – INTO instruction with an overflow flag
6. Type 5: BOUND – Register contents out-of-bounds
7. Type 6: Invalid Opcode – Undefined opcode occurred in program
8. Type 7: Coprocessor not available – MSW indicates a coprocessor
9. Type 8: Double Fault – Two separate interrupts occur during the same instruction
10. Type 9: Coprocessor Segment Overrun – Coprocessor call operand exceeds FFFFH
11. Type 10: Invalid Task State Segment – TSS invalid (probably not initialized)
12. Type 11: Segment not present – Descriptor P bit indicates segment not present or invalid
13. Type 12: Stack Segment Overrun – Stack segment not present or exceeded
14. Type 13: General Protection – Protection violation in 286 (general protection fault)
15. Type 14: Page Fault – 80386 and above

16. Type 16: Coprocessor Error – ERROR' = '0' (80386 and above)
17. Type 17: Alignment Check – Word / Double word data addressed at odd location (486 and above)
18. Type 18: Machine Check – Memory Management interrupt (Pentium and above)

UNIT -II:

Instruction Set and Assembly Language Programming of 8086:

8086 INSTRUCTIONS

An instruction given to the computer it performs a specified operation on given data. The instruction set of a microprocessor is the collection of the instructions that the microprocessor is designed to execute.

The instructions of Intel 8086 have been classified into the following groups.

1. Data transfer instructions.
2. Arithmetic instructions.
3. Bit manipulation (logical) instructions.
4. String instructions.
5. Program execution transfer instructions.
6. Processor control instructions.

DATA TRANSFER INSTRUCTIONS

General purpose byte or word transfer instructions:

MOV	Copy byte or word from specified source to specified destination.
PUSH	Copy specified word to top of stack

POP Copy word from top of stack to specified location.

XCHG Exchange bytes or exchange words.

XLAT Translate a byte in AL using a table in memory.

Simple input and output port transfer instructions:

IN Copy a byte or word from specified port to accumulator.

OUT Copy a byte or word from accumulator to specified port.

Special address transfer instructions:

LEA Load effective address of operand into specified register.

LDS Load DS register and other specified registers from memory.

LES Load ES register and other specified register from memory.

Flag transfer instructions:

LAHF Load (copy to) AH with the low byte of the flag register.

SAHF Store (copy) AH Register to low byte of flag register.

PUSHF Copy flag register to top of stack.

POPF Copy word at top of stack to flag register.

ARITHMETIC INSTRUCTIONS

Addition instructions:

ADD Add specified byte to byte or specified word to word.

ADC Add byte + byte + carry flag or word + word + carry flag

INC Increment specified byte or specified word by 1.

AAA ASCII adjust after addition.

DAA Decimal (BCD) adjust after addition.

Subtraction instructions

SUB Subtract byte from byte or word from word.

SBB Subtract byte and carry flag from byte or word and carry flag from word

DEC Decrement specified byte or specified word by 1

NEG Negate – invert each bit of a specified byte or word and add 1 (form 2’s

compliment).

CMP Compare two specified bytes or two specified words.

AAS ASCII adjust after subtraction.

DAS Decimal (BCD) adjust after subtraction.

Multiplication instructions :

MUL Multiply unsigned byte by byte or unsigned word by word.

IMUL Multiply signed byte by byte or signed word by word.

AAM ASCII adjust after multiplication.

Division instructions:

DIV Divide unsigned word by byte or unsigned double word by word.

IDIV Divide signed word by byte or signed double word by word.

AAD ASCII adjust before division.

CBW Fill upper byte or word with copies of sign bit of lower byte.

CWD Fill upper word of double word with sign bit of lower word.

BIT MANIPULATION INSTRUCTIONS

Logical instructions:

NOT Invert each bit of a byte or word

AND AND each bit in a byte or word with the corresponding bit in another byte or word.

OR OR each bit in a byte or word with the corresponding bit in another byte or word.

XOR Exclusive OR each bit in a byte or word with the corresponding bit in another byte or word.

TEST AND operands to update flags, but don’t change operands.

Shift instructions:

SHL/SAL Shift bits of word or byte left, put zero(s) in LSB(s).

SHR Shift bits of word or byte right, put zero(s) in MSB(s).

SAR Shift bits of word or byte right, copy old MSB into new MSB.

Rotate instructions:

ROL Rotate bits of byte or word left, MSB to LSB and to CF.

ROR Rotate bits of byte or word right, LSB to MSB and to CF.

RCL Rotate bits of byte or word left, MSB to CF and CF to LSB.

RCR Rotate bits of byte or word right LSB to CF and CF to MSB.

STRING INSTRUCTIONS

A string is a series of byte or a series of words in sequential memory locations. A string often consists of ASCII character codes. In the list, a "/" is used to separate different mnemonics for the same instructions. Use the mnemonic which most clearly describe the function of the instruction in a specific application. A "B" in a mnemonic is used to specifically indicate that a string of bytes is to be acted upon. A "W" in the mnemonic is used to indicate that a string of words is to be acted upon.

REP An instruction prefix. Repeat following instruction until CX=0.

REPE/REPZ An instruction prefix. Repeat instruction until CX = 0 or zero flag ZF 1.

REPNE/REPNZ An instruction prefix. Repeat until CX = 0 or ZF = 1.

MOVS/MOVSB/MOVSW Move byte or word from one string to another

COMPS/COMPSB/COMPSW Compare two string bytes or two string words

SCAS/SCASB/SCASW Scan a string. Compare a string byte with a byte in AL or a string word with a word in AX

LODS/LODSB/LODSW Load string byte into AL or string word into AX

STOS/STOSB/STOSW Store byte from AL or word from AX into string

PROGRAM EXECUTION TRANSFER INSTRUCTIONS

These instructions are used to tell the 8086 to start fetching instruction from some new address, rather than continuing in sequence.

Unconditional transfer instructions:

CALL Call a procedure (subprogram) save return address on stack.

RET Return from procedure to calling program.

JMP Go to specified address to get next instruction.

A “/” is used to separate two mnemonics which represent the same instruction. Use the mnemonic which most clearly describes the decision condition in a specific program. These instructions are often used after a compare instruction. The term below and above refers to unsigned binary numbers. Above means larger in magnitude. The terms greater than or less than refer to signed binary numbers. Greater than means more positive.

JA/JNBE Jump if above/Jump if not below or equal

JAE/JNB Jump if above or equal / Jump if not below

JB/JNE Jump if below / Jump if not above or equal

JBE/JNA Jump if below or equal / Jump if not above

JC Jump if carry flag CF = 1

JE/JZ Jump if equal / Jump if zero flag ZF = 1

JG/JNLE Jump if greater / Jump if not less than or equal

JGE/JNL Jump if greater than or equal / jump if not less than

JL/JNGE Jump if less than / Jump if not greater than or equal

JLE/JNG Jump if less than or equal / Jump if not greater than

JNC Jump if no carry (CF = 0)

JNE/JNZ Jump if not equal / Jump if not zero (ZF = 0)

JNO Jump if no overflow (overflow flag OF = 0)

JNP/JPO Jump if not parity / Jump if parity odd (PF = 0)

JNS Jump if not sign (sign flag SF = 0)

JO Jump if over flow flag OF = 1

JP/JPE Jump if parity / Jump if parity even (PF = 1)

JS Jump if sign (SF = 1)

ITERATION CONTROL STATEMENTS

These instructions can be used to execute a series of instructions some number of times. Here mnemonics separated by a “/” represent the same instruction. Use the one that best fits the specific application.

LOOP Loop through a sequence of instructions until CX = 0.

LOOPE/LOOPZ	Loop through a sequence of instructions while ZF = 1 and CX	0
LOOPNE/LOOPNZ	Loop through a sequence of instructions while ZF = 0 and CX	0.
JCXZ	Jump to specified address if CX = 0.	

Interrupt instructions:

INT	Interrupt program execution, call service procedure
INTO	Interrupt program execution if OF = 1
IRET	Return from interrupt service procedure to main program

PROCESSOR CONTROL INSTRUCTIONS

Flag set/clear instructions:

STC	Set carry flag CF to 1
CLC	Clear carry flag CF to 0
CMC	Compliment the state of the carry flag CF
STD	Set direction flag DF to 1 (decrement string pointer)
CLD	Clear direction flag DF to 0
STI	Set interrupt enable flag to 1 (enable INTR input)
CLI	Clear interrupt enable flag to 0 (disable INTR input)

External hardware synchronization instructions:

HLT	Halt (do nothing) until interrupt or reset
WAIT	Wait (do nothing) until signal on the TEST pin is low
ESC	Escape to external co-processor such as 8087 or 8089
LOCK	An instruction prefix. Prevents another processor from taking the bus while the adjacent instruction executes

No operation instruction:

NOP	No action except fetch and decode.

Instruction formats

opcode	D	W	MOD	REG	R/M	Low byte displacement	High byte displacement	Low byte immediate	Higher byte immediate

								data	data
6	1	1	2	3	3	8	8	8	8

Different Instructions

1) One byte instructions

2) Register to register instructions

3) Register to memory with no displacement

4) Register to memory with displacement

5) Immediate operand to register

6) Immediate operand to memory with 16 bit displacement

1) One byte instruction: This format is only one byte long and may have the implied data or register operands. The least significant 3 bits are used for specifying the register operand if any. Otherwise all the 8 bits form an opcode and the operands are implied.

One byte instruction format:

opcode	D	W
6	1	1

Ex) STC, CLC, STD, CLD.,

2) Register to register instruction : This format is a 2 byte long. The first byte of the code specifies the operation code and width of the operand specified by W bit. The second byte of the code shows the register operands and R?M fields as shown.

Register to register instruction format:

opcode	D	W	MOD	REG	R/M
6	1	1	2	3	3

Ex) MOV AX,BX

MOV AL,BL

3)Register to memory with no displacement : This format also 2 bytes long and similar to register to register format except for the MOD field.

Register to memory with no displacement instruction format:

opcode	D	W	MOD	REG	R/M
6	1	1	2	3	3

Ex) MOV AL, [DX]

4) Register to memory with displacement: This type of instruction format contains one or two additional bytes for displacement along with the format of the register to/from memory without displacement.

Register to memory with displacement

opcode	D	W	MOD	REG	R/M	Low byte displacement	High byte displacement
6	1	1	2	3	3	8	8

EX) MOV AL,[4587]

5)Immediate Operand to Register : In this format, the first byte as well as the 3-bits from secod byte which are used for REG field are used for opcode.

Immediate operand to register format:

opcode	D	W	MOD	REG	R/M	Low byte displacement	High byte displacement
6	1	1	2	3	3	8	8

EX) MOV AL,45H

MOV AX,4568H

6) Immediate operand to memory with 16 bit displacement: This type of instruction format requires 5 or 6 bytes for coding. The first 2 bytes contain the information regarding OPCODE, MOD and R/M. The remaining 4 bytes contain 2 bytes of displacement and 2 bytes of data.

Opcode	D	W	MOD	REG	R/M	Low byte displacement	High byte displacement	Low byte immediate data	Higher byte immediate data
6	1	1	2	3	3	8	8	8	8

EX) MOV DEST [DI],4567H

The opcode usually appears in the first byte, but in a few instructions, in some instructions the 3-bits in the second byte also used for opcode.

The assembler instruction formats of intel 8086 are shown. The description of instruction format is as follows:

D- represents a 1 bit field identifying the direction. If D is 0 the register specified is the source, otherwise destination.

W-bit : This indicates whether the instruction is to be operate over an 8-bit data or 16 -bit data. If w bit is 0, the operand is of 8-bits and if w is 1, the operand is of 16-bits.

MOD is a 2-bit field defines addressing mode.

REG is a 3-bit field identifies a register

R/M is a 3-bit field specifies a register or memory address.

Displacement is an 8-bit or 16-bit value contained in an instruction.

The REG code of the different registers either as source or as destination operands in the opcode byte are assigned with binary codes. The segment registers are only 4. Hence 2 binary bits are sufficient to code them. The other registers are 8 in number, so at least 3 bits are required for coding them.

Addressing modes

Each instruction requires certain data on which it has to operate. There are various techniques to specify the address of the data. The different ways that a processor can access data are referred to as its addressing modes.

For example the MOV instruction has the format

MOV destination, source

When executed, this instruction copies a word or a byte from the specified source location to the specified destination location. The source can be a number written directly in the instruction, a specified register, or a memory location.

The destination can be a specified register or a memory location.

The source and destination cannot both be memory locations in an instruction.

The various addressing modes can be classified into the following groups.

1. Immediate addressing mode.

2. Register addressing mode.

3. Addressing modes for accessing data in memory.

    a. Direct Addressing mode

    b. Register indirect Addressing mode

c. Based Addressing mode

d. Indexed Addressing mode

e. Based indexed Addressing mode

f. String Addressing mode.

4. Addressing modes for accessing I/O ports.

5. Relative addressing mode.

6. Implied addressing mode.

1.Immediate Addressing Mode:-

Suppose if you want to put a number 437BH in the CX register,

MOV CX, 437BH

instruction can be used. This instruction will put the immediate hexadecimal number 437BH in the 16-bit CX register. This is referred to as immediate addressing mode, because the number to be loaded into CX register will be put in two memory locations immediately following the code for the MOV instruction.

CH ← 43H

CL ← 7BH

The instruction MOV CL, 48H can be used to load the 8-bit immediate number 48H into the 8-bit CL register.

2. Register Addressing Mode :-

Register addressing mode means that a register is the source of an operand for the instruction.

For example

MOV CX, AX

Copies the contents of the 16-bit AX register into the 16-bit CX register. The previous contents of CX are written over, but the contents of AX are not changed. If CX contains 2A84H and AX contains 4971H before MOV CX, AX instruction executes. After the instruction executes CX will contains 4971H and AX will still contains 4971H.

You can move any 16-bit register to any 16-bit register, or you can move any 8-bit register to any 8-bit register. But you cannot move an 8-bit register to a 16-bit register.

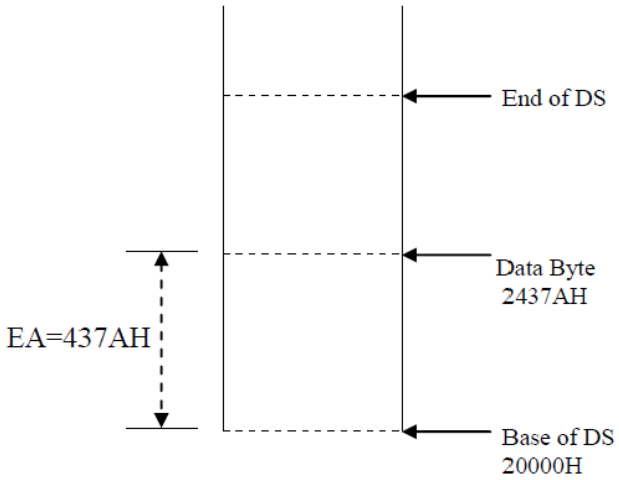
MOV AL,BL ; Content of register BL is copied to register AL.

3a) Direct Addressing Mode: -

MOV CL, [437AH]

The square brackets around the 437AH indicate that "the contents of the memory location at a displacement from the segment base". When this instruction executed the contents of the memory location, at a displacement of 437AH from the data segment base copied into CL register.

The actual 20-bit physical memory address will be produced by shifting the data segment base in DS four bit left and adding the effective address 437AH to the result.



MOV BX, [437AH]

This instruction copies a word from memory into the BX register. Since each memory address of 8086 represents a byte of storage, the word must come from two memory locations.

DS=	2	0	0	0	0	H
EA=		4	3	7	A	H
Physical Address	2	4	3	7	A	H

The byte at a displacement of 437AH from the data segment base will be copied into BL. The contents of next higher address, displacement 437BH, will be copied into the BH register.

[BL] ← [437AH]

[BH] ← [437BH]

The instruction MOV [437AH], BX will copy the contents of the BX register to two

memory locations in the data segment. The contents of BL will be copied to the memory location at a displacement of 437AH. The contents of BH will be copied to the memory location at a displacement of 437BH.

[437AH ← [BL]

[437BH ← [BH]

3b) Register Indirect Addressing Mode :-

In this mode, the effective address is specified in either a pointer register or an index register. The pointer register can be either base register BX or a base pointer register BP and index register can be either source index (SI) register or destination Index (DI) register.

The 20-bit physical address is computed using DS and EA.

Example:- MOV [DI], BX

The destination operand of the above instruction is in register indirect mode; while the source operand is in register mode. The instruction moves the 16-bit content of BX into a memory location offset by the value of EA specified in DI from the current contents in DS.

DS = 5004H 50040H

DI = 0020H 0020H

BX= 2456H 50060H

After MOV[DI], BX the content of BX (2456) is moved to memory locations 50060 and 50061.

3c) Based Addressing Mode:-

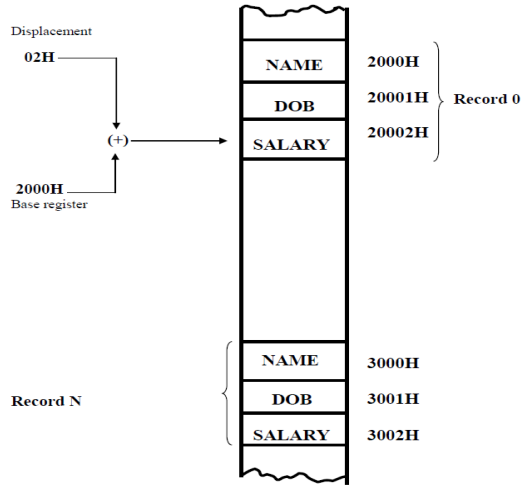
In this mode EA is obtained by adding a displacement value to the contents of BX or BP. The segment registers used are DS and SS. When memory is accessed, the 20-bit physical address is computed from BX and DS, on the other hand when the stack is accessed, the 20-bit physical address is computed from BP and SS. This allows the programmer to access the stack without changing SP contents.

MOV AL, START [BX]

The source operand in the above instruction is in based mode. EA is obtained by adding the value of start and [BX]. The 20-bit physical address is produced from DS and EA.

The 8-bit content of this memory location is moved to AL. The displacement START can be either unsigned 16-bit or signed 8-bit.

MOV AL, START [BX]



BX		2	0	0	0	H
START				0	2	H
EA		2	0	0	2	H
DS	2	0	0	0	0	H
Physical Address	2	2	0	0	2	H

Based addressing provides a convenient way to address structure which may be stored at different places in memory.

For example the element salary in record 0 of employee name 0 can be loaded into an 8086 internal register such as AL using the instruction MOV AL, ALPHA[BX], where ALPHA is the 8-bit displacement 02H and BX contains the starting address of record 0. Now in order to access the salary of record N, the programmer simply changes the contents of base register to 3000H.

Indexed Addressing Mode :-

In this mode, the effective, address is calculated by adding the unsigned 16-bit or signed 8-bit displacement and the contents of SI or DI.

MOV BH, START [SI]

Move the contents of 20-bit address computed from the displacement START, SI and DS into BH.

The 8-bit displacement is provided by the programmer using the assembler pseudo instruction such as EQU.

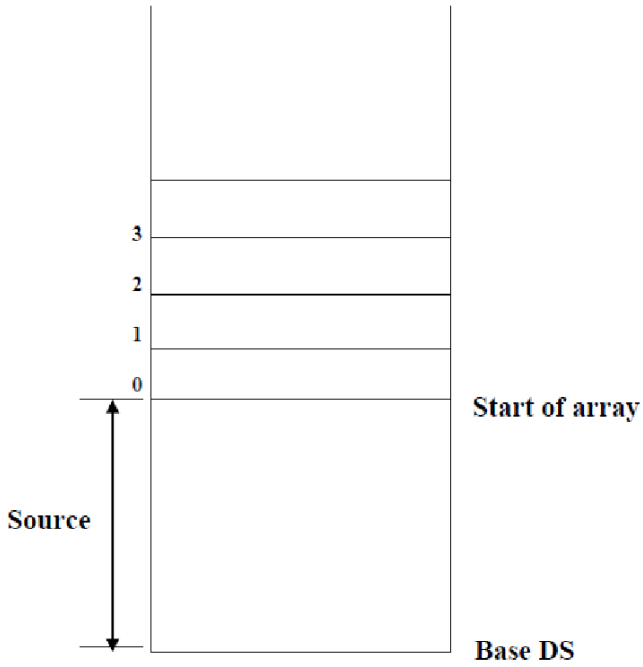
Index addressing mode can be used to access a single table(Single dimensional array). The displacement can be the starting address of the table. The contents of SI or DI can then be used as an index from the starting address to access a particular

element in the table.

The instruction

MOV AL, Source [SI]

Sends elements of array to register AL Where Source is the name of the array SI gives the position. I f SI=0, the first element will be copied into register AL, if SI=1, the second element will be copied into register AL, and so on.



Based Indexed Addressing Mode:-

In this mode EA is computed by adding a base register [BX OR BP], an index register [SI or DI] and a displacement.

MOVE ALPHA [SI][BX],CL

[BX] = 0200H

ALPHA = 08H

[SI] = 1000H

[DS] = 3000H

[DS] ---------- |3|0|0|0|0|H

[BX] ---------- | |0|2|0|0|H

ALPHA ---------- | | | |0|8|H

[SI] ---------- |3|1|2|0|8|H

Then 8-bit content of CL is moved to 20-bit physical address 31208.

Based index addressing mode provides a convenient way for a subroutine to address an array allocated on stack. Register BP can be loaded with the offset in the segment SS. The displacement can be the value which is the difference between the top of the stack and the beginning of the array. An index register can then be used to access individual array elements.

String Addressing Mode:-

This mode uses index registers. The string instructions automatically assume SI to point the first byte or word of the source operand and DI to point to the first byte or word of the destination operand. The contents of SI and DI are automatically incremented; or decremented to point to the next byte or word.

Consider MOVSB instruction

If [DF]=0 [DS]=2000H, [SI]=0500H, [ES]=4000H, [DI]=0300H,

[20500H]=38H and [40300H]=45H

LEA SI, Source

LEA DI, Destination

MOV CX, 0004H

CLD

REP MOVSB

Then after execution of MOVS BYTE instruction

[40300H]=38H and [SI]=0501H [DI]=0301H.

MOVSB instruction moves one byte from source to destination increases SI and DI, Decreases CX. REP checks whether count in CX is zero or not. If it is not zero it repeats MOVSB until CX becomes zero. The contents of other registers and memory locations are unchanged. Note that SI and DI can be used in either source or destination operand of a two operand instruction.

4. ADDRESSING MODES FOR ACCESSING I/O PORTS :-

Standard I/O uses port addressing modes. For memory mapped I/O, memory addressing modes are used. There are two types of port addressing modes.

Direct & Indirect

In direct port mode, the port number is an 8-bit immediate operand. This allows fixed access to ports numbered 0 to 255.

For example OUT 05H, AL outputs content of AL to 8-bit port 05H.

IN AL,05H ;input data from port address 05H to register AL

In indirect port mode, the port number is taken from DX allowing 64K 8-bit ports or 32K 16-bit ports.

For example if [DX] = 5040H then

IN AL, DX

Inputs the 8-bit content of port 5040H into AL.

On the other hand IN AX,DX inputs the 8-bit contents of ports 5040H and 5041H into AL and AH respectively. Note that 8-bit and 16-bit I/O transfers must take place via AL and AX respectively.

OUT DX, AL

This instruction sends the contents of register AL to the port addressed by DX.

5. Relative Addressing Mode :-

Instructions using this mode specify the operand as a signed 8-bit displacement relative to Program Counter/instruction pointer.

JNC START

This instruction means that if carry = 0 then PC/IP is loaded with current PC/IP contents + 8-bit signed value of START. Otherwise the next instruction is executed.

MOV AL, N1

MOV AH, 00H

MOV BL, N2

ADD AL, BL

JNC FORWARD

INC AH

FORWARD: MOV RES, AX

HLT

Other Examples

JC : Jump on Carry

JNC= Jump on no carry

JE/JZ: Jump if equal or jump on zero

JNE/JNZ: Jump if not equal/jump if result is not zero

JNP/JPO: Jump if no parity/jump if odd parity

JS: Jump if sign flag is set.

6) Implied Addressing Mode:-

Instructions using this mode have no operands. An example is

CLC which clears the carry Flag to zero.

STC-Set carry Flag

CMC-Complement carry Flag

STI-Set Interrupt Flag

CLI-Clear Carry Flag

STD-Set Direction Flag

CLD-Clear Direction Flag

Assembler Directives

Assembly language programs are composed of two types of statements.

1) The Instructions which can be translated to machine code by the assembler.

2) The directives that directs the assembler during the assembly process for which no machine code is generated.

Assembler Directives are instructions entered into the source code along with the assembly language. Pseudo instructions (Assembler Directives) do not get translated into object code, but are used as special instructions to the assembler to perform some special functions. The directives control the generation of machine code and organization of the program.

Ex: SEGMENT, ENDS, ASSUME, DB, DW, DD, DQ, DT, END, PROC, ENDP, MACRO, ENDM, EQU, LENGTH, SIZE, OFFSET, EVEN, ORG, LABEL, INCLUDE

The assembler directives are classified into the following categories based on the functions performed by them. They are

a) Data definition and storage allocation directives

b) Program organization directives

c) Alignment Directives

d) Program end Directive

e) Value returning attribute directives

f) Procedure definition directives

g) Macro definition directives

h) Data control directives

i) Header file inclusion directives

a) Data definition and storage allocation directives

Data definition directives are used to define the program variables and allocate a specified amount of memory to them. They are of type BYTE, WORD, Double Word, Quad Word and Ten Byte and their size in bytes are 1,2,4,8 and 10 respectively. The data definition directives are DB, DW, DD, DQ, DT.

DB – [define byte]

The DB directive is used to define a byte–type variable or to set aside one or more storage locations of type byte in memory. It can be used to define single or multiple byte variables.

Ex 1) n DB 42H

tells the assembler to reserve 1 byte of memory for a variable named n and to put the value 42H in the that memory location, when the program is loaded into memory to be run.

Ex 2) num DB ?

The above statement informs the assembler to reserve one byte of memory for a variable named num. use of ? in data definition informs the assembler that the value is unknown and hence the variable num is not initialized.

Ex 3) grade DB ‘A’ or “A”

The above statement informs the assembler to reserve one byte of memory for a variable named grade and initializes with ASCII equivalent of a letter ‘A’. The ASCII character should be enclosed within single or double quotes.

Ex 4) num DB 25,50,43,76,34

The above statement reserves 5 bytes of consecutive memory locations for the variable num and initializes them with 5 values.

Ex 5) info DB ‘welcome’

The above statement defines a variable info and reserves 7 bytes of consecutive

memory locations and initializes with the string ‘welcome’ during execution of program.

Ex 6) sname db 10 dup(‘-‘)

This statement defines a variable sname, reserves 10 bytes of consecutive memory locations and initializes with ASCII equivalent of character ‘-‘.

Ex 7) sum db 25 dup(?)

This statement defines a variable and reserves 25 bytes of consecutive memory locations and are not initialized.

DW – [define word]

The DW directive is used to declare a variable of type word, or to reserve storage locations of type word in memory.

Ex:- MULTIPLIER DW 347AH

num dw 023ah

sum dw ?

items dw 03abh, 0abc4h, 0bbah, 0543ch, 04a4bh

res dw 20 dup(0)

DD – [define double word]

The DD directive is used to declare a variable of type double word.

DQ – Define Quad word :

The directive DQ is used to define a quad word (8 bytes) type variable.

DT – Define Ten bytes :

The directive DT is used to define a Ten bytes type variable.

b) Program organization directives

SEGMENT : The segment directive is used to indicate the start of a logical segment. Preceding the segment directive the name you want to give the segment.

CODE SEGMENT

CODE ENDS

Indicates to the assembler the start of a logical segment called code. The SEGMENT and ENDS directives are used to identify a group of data items or a group of instructions that you want to be put together in a particular segment. A group of data statements or a group of instruction statements contained between segment and ends directives is called a logical segment. When you setup a logical segment, you give it a name of your choosing.

ENDS :- [end segment] : This directive is used with the name of a segment to indicate the end of the logical segment. ENDS is used with the segment directive to 'bracket' a logical segment containing instructions or data.

data segment

n1 db 05h

n2 db 04h

sum db ?

data ends

ASSUME :-

The assume directive is used to tell the assembler the name of the logical segment it should use for a specified segment. The 8086 program may have several logical segments. At any time the 8086 works directly with only four physical segments; a code segment, a data segment, a stack segment and an extra segment.

The statement

ASSUME CS : Code

tells the assembler that the instructions for a program are in a logical segment named code.

code segment

assume cs:code, ds:data

mov ax,data

mov ds,ax

---

code ends

data segment

---

data ends

end

c) Alignment Directives

EVEN :

Align as even memory address. The directive EVEN is used to inform the assembler to increment the location counter to the next even memory address if it is not pointing to even memory location already.

data segment

sum db 10

even

items dw 100 dup(?)

data ends

The data array items starts at the even memory location which makes access to its elements efficient; The directive even is used for the alignment of the data array item.

ORG : Originate :

The directive ORG assigns the location counter with the value specified in the directive. It helps in placing the machine code in the specified location while translating the instructions into machine codes by the assembler.

ORG 100

The above statement informs the assembler to initialize the location counter to 100.

d) Program end Directive

END – END PROGRAM

The END directive is put after the last statement of a program to tell the assembler that this is the end of the program module. A carriage return is required after the END directive. The last statement of every program must be an end directive.

code segment

---

ends

data segment

---

data ends

end

e) Value returning attribute directives

LENGTH:

The directive length informs the assembler about the number of elements in a data item such as an array. If an array is defined with DB then it returns the number of bytes allocated to the variable. If an array is defined with DW then it returns the number of words allocated to the array variable.

Ex1) MOV AX, LENGTH ITEMS

data segment

items db 08h,78h,56h,78h,98h

data ends

In the above example the number of elements assigned as array are 5. So five is the length of items which will be stored in AX.

Ex2) MOV AX, LENGTH ITEMS

data segment

items dw 0048h,0a78h,0b56h,0c78h,0d98h

data ends

In the above example the number of elements assigned as array are 5. So five is the length of items which will be stored in AX.

SIZE:

The directive SIZE is same as LENGTH except that it returns the number of bytes

allocated to the data item instead of the number of elements in it.

Ex1) MOV AX,SIZE ITEMS

data segment

items DB 08h,78h,56h,78h,98h

data ends

In the above example the number of bytes occupied by the array items are 5. So 5 is the size of items which will be stored in AX.

Ex2) MOV AX, SIZE num

data segment

num DW 0008h,0078h,0a56h,0b78h,0c98h

data ends

In the above example the number of bytes occupied by the array elements 10. So 10 is the size of num which will be stored in AX.

OFFSET :

The directive OFFSET informs the assembler to determine the displacement of the specified variable with respect to the base of data segment.

Offset variable_ name

Ex:

MOV DX, OFFSET MSG

Data segment

MSG DB ‘nalanda’

Data ends

f) Procedure definition directives

PROC:

The PROC directive is used to identify the start of a procedure. The PROC directive

follows a name you give the procedure. After the PROC directive the term NEAR or FAR is used to specify the type of the procedure.

Factorial PROC Near

RET

Factorial ENDP

ENDP :- [end procedure]

This directive is used along with the name of the procedure to indicate the end of a procedure to the assembler.

SQUARE_ROOT PROC NEAR

SQUARE_ROOT ENDP

g) Macro definition directives

MACRO:

A macro is a group of instructions we bracket and give a name to at the start of our program. Each time we call the macro in our program, the assembler insert the defined group of instructions in place of the call.

The MACRO directive is used to identify the start of a macro. The Macro directive follows a name you give the macro.

MACRONAME MACRO ; START OF MACRO

ENDM ; END OF MACRO

ENDM :-[end macro]

This directive is used along with the name of the macro to indicate the end of a macro to the assembler.

PUSHALL MACRO

PUSHF

PUSH AX

PUSH BX

PUSH CX

PUSH DX

ENDM

EQU :-[equate]

EQU is used to give a name to some value or symbol. Each time the assembler finds the given name in the program it will replace the name with the value or symbol equated with that name.

Ex1) SUM EQU 10

The above statement declares the symbol SUM with value 10. The assembler will replace every occurrence of the symbol in the program by its value.

Ex2) MOVEMENT EQU MOV

Every occurrence of MOVEMENT will be replaced by MOV.

Ex3) DECIMAL_ADJUST EQU DAA

Every occurrence of DECIMAL_ADJUST will be replaced by DAA.

h) Data control directives

LABEL:

The label directive is used to give a name to the current value in the location counter. The label directive must be followed by a term which specifies the type you want associated with that name.

STK SEGMENT

S DW 100 DUP(0)

S_TOP LABEL WORD

STK ENDS

i) Header file inclusion directives

INCLUDE:

The header file inclusion directive is used to define an include file header. The header file inclusion directive is INCLUDE.

The directive INCLUDE informs the assembler to include the statements defined in the include file. The name of the include file follows the statement INCLUDE. It is useful to place all the data and frequently used macros into a file known as include file or header file.

INCLUDE <file path specification>

Simple Programs involving Logical, Branch and Call Instructions Sorting, Evaluating Arithmetic Expressions

ALP to adding two multi byte numbers and store the result as the third number

```
DATA SEGMENT

BYTES EQU 08H

NUM1 DB 05H, 5AH, 6CH, 55H, 66H, 77H, 34H, 12H

NUM2 DB 04H, 56H, 04H, 57H, 32H, 12H, 19H, 13H

NUM3 DB 0AH DUP (00)

DATA ENDS

CODE SEGMENT

ASSUME CS: CODE, DS: DATA

START: MOV AX, DATA
 MOV DS, AX
 MOV CX, BYTES
 LEA SI, NUM1
 LEA DI, NUM2
 LEA BX, NUM3
MOV AX, 00
NEXT: MOV AL, [SI]
 ADC AL, [DI]
 MOV [BX], AL
 INC SI
```

```
 INC DI
 INC BX
 DEC CX
JNZ NEXT
INT 3H
CODE ENDS
END START
```

ALP to Subtracting two multi byte numbers and store the result as the third number

```
DATA SEGMENT
BYTES EQU 08H
NUM2 DB 05H, 5AH, 6CH, 55H, 66H, 77H, 34H, 12H
NUM1 DB 04H, 56H, 04H, 57H, 32H, 12H, 19H, 13H
NUM3 DB 0AH DUP (00)
DATA ENDS
CODE SEGMENT
ASSUME CS: CODE, DS: DATA
START: MOV AX, DATA
 MOV DS, AX
 MOV CX, BYTES
 LEA SI, NUM1
 LEA DI, NUM2
 LEA BX, NUM3
 MOV AX, 00
NEXT: MOV AL, [SI]
 SBB AL, [DI]
 MOV [BX], AL
 INC SI
```

```
 INC DI
 INC BX
 DEC CX
JNZ NEXT
INT 3H
CODE ENDS
END START
```

ALP to Multiplying two multi byte numbers and store the result as the third number

```
DATA SEGMENT
BYTES EQU 08H
NUM1 DB 05H, 5AH, 6CH, 55H, 66H, 77H, 34H, 12H
NUM2 DB 04H, 56H, 04H, 57H, 32H, 12H, 19H, 13H
NUM3 DB 0AH DUP (00)
DATA ENDS
CODE SEGMENT
ASSUME CS: CODE, DS: DATA
START: MOV AX, DATA
 MOV DS, AX
 MOV CX, BYTES
 LEA SI, NUM1
 LEA DI, NUM2
 LEA BX, NUM3
 MOV AX, 00
NEXT: MOV AL, [SI]
 MOV DL,[DI]
 MUL DL
 MOV [BX], AL
```

```
 MOV [BX+1],AH
 INC SI
 INC DI
 INC BX
 INC BX
 DEC CX
JNZ NEXT
INT 3H
CODE ENDS
END START
```

ALP to Dividing two multi byte numbers and store the result as the third number

```
DATA SEGMENT
BYTES EQU 08H
NUM2 DB 05H, 5AH, 6CH, 55H, 66H, 77H, 34H, 12H
NUM1 DB 04H, 56H, 04H, 57H, 32H, 12H, 19H, 13H
NUM3 DB 0AH DUP (00)
DATA ENDS
CODE SEGMENT
ASSUME CS: CODE, DS: DATA
START: MOV AX, DATA
 MOV DS, AX
 MOV CX, BYTES
 LEA SI, NUM1
 LEA DI, NUM2
 LEA BX, NUM3
NEXT: MOV AX, 00
MOV AL, [SI]
```

```
 MOV DL,[DI]
 MUL DL
 MOV [BX], AL
 MOV [BX+1],AH
 INC SI
 INC DI
 INC BX
 INC BX
 DEC CX
JNZ NEXT
INT 3H
CODE ENDS
END START
```

ALP to ASCII Addition:

```
CODE SEGMENT
ASSUME CS: CODE
START: MOV AL,'5'
 MOV BL,'9'
 ADD AL, BL
 AAA
 OR AX, 3030H
 INT 3H
CODE ENDS
END START
```

ALP to Converting Packed BCD to unpacked BCD:

```
DATA SEGMENT
NUM DB 45H
```

```
DATA ENDS
CODE SEGMENT
ASSUME CS: CODE, DS: DATA
START: MOV AX, DATA
 MOV DS, AX
 MOV AX, NUM
 MOV AH, AL
 MOV CL, 4
SHR AH, CL
AND AX, 0F0FH
INT 3H
CODE ENDS
END START
```

ALP to Moving a Block using strings

```
DATA SEGMENT
SRC DB 'MALLAREDDY ENGINEERING COLLEGE'
 DB 10 DUP (?)
DST DB 20 DUP (0)
DATA ENDS
CODE SEGMENT
ASSUME CS: CODE, DS: DATA, ES: DATA
START: MOV AX, DATA
 MOV DS, AX
 MOV ES, AX
 LEA SI, SRC
 LEA DI, DST
 MOV CX, 20
```

```
 CLDi
CODE ENDS
END START
```

ALP to move a string from one place to another place

```
CODE SEGMENT
ASSUME CS:CODE, DS:DATA, ES:DATA
MOV AX,DATA
MOV DS,AX
MOV ES,AX
LEA SI,SOURCE
LEA DI,DEST
MOV CX,0007H
CLD
REPE MOVSB
HLT
CODE ENDS
DATA SEGMENT
SOURCE DB 'MALLAREDDY ENGINEERING COLLEGE'
DEST DB ?
DATA ENDS
END
```

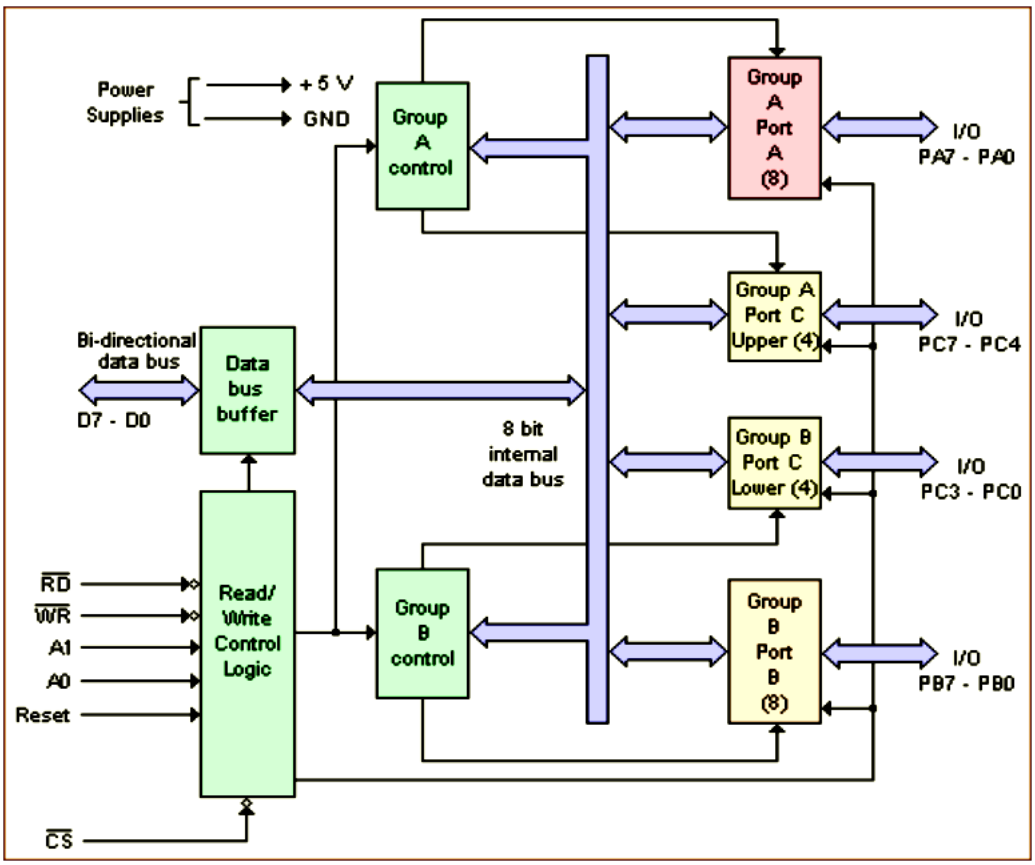
UNIT -IV:

I/O Interface:

8255 PPI, Various Modes of Operation and Interfacing to 8086

The 8255 is a widely used, programmable parallel I/O device. It can be programmed to transfer data under data under various conditions, from simple I/O to interrupt I/O. It is flexible, versatile and economical (when multiple I/O ports are required). It is an important general purpose I/O device that can be used with almost any

microprocessor. The 8255 has 24 I/O pins that can be grouped primarily into two 8 bit parallel ports: A and B, with the remaining 8 bits as Port C. The 8 bits of port C can be used as individual bits or be grouped into two 4 bit ports : CUpper (CU) and CLower (CL). The functions of these ports are defined by writing a control word in the control register. 8255 can be used in two modes: Bit set/Reset (BSR) mode and I/O mode. The BSR mode is used to set or reset the bits in port C. The I/O mode is further divided into 3 modes: mode 0, mode 1 and mode 2. In mode 0, all ports function as simple I/O ports. Mode 1 is a handshake mode whereby Port A and/or Port B use bits from Port C as handshake signals. In the handshake mode, two types of I/O data transfer can be implemented: status check and interrupt. In mode 2, Port A can be set up for bidirectional data transfer using handshake signals from Port C, and Port B can be set up either in mode 0 or mode 1.



RD (Read): This signal enables the Read operation. When the signal is low, microprocessor reads data from a selected I/O port of 8255.

WR (Write): This control signal enables the write operation.

RESET (Reset): It clears the control registers and sets all ports in input mode.

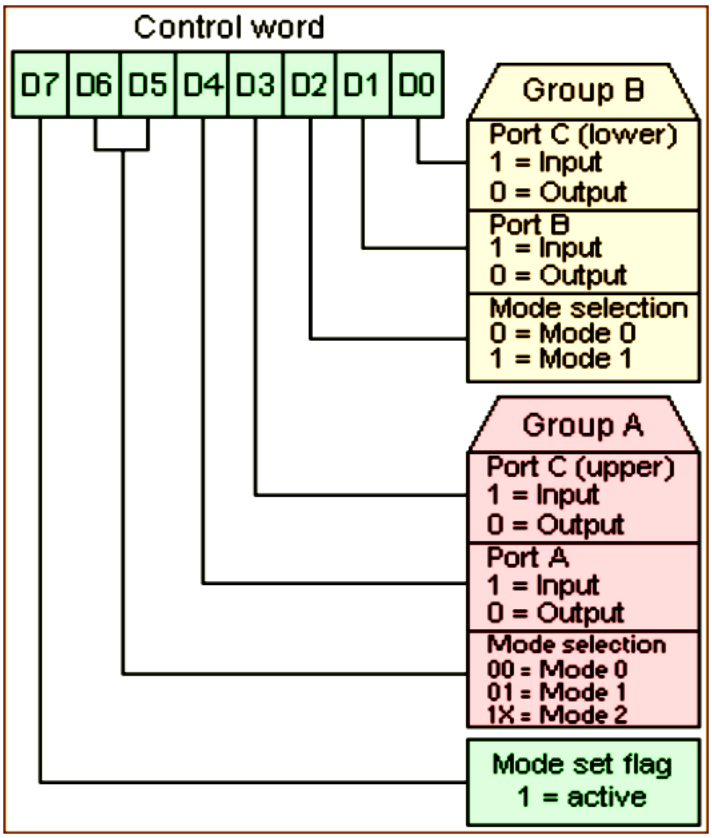
CS, A0, A1: These are device select signals. is connected to a decoded address and

A0, A1 are connected to A0, A1 of microprocessor.

CS	A_0	A_1	Selected

0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	X	X	8255 Not Selected

Control Word Format of 8255:



This mode is selected by making D7 = '1'.
D0, D1, D3, D4 are for lower port C, port B, upper port C and port A respectively. When D0 or D1 or D3 or D4 are "SET", the corresponding ports act as input ports.

Eg: if D0= D4 = '1', then lower port C and port A act as input ports.

If these bits are "RESET", then the corresponding ports act as output ports.

Eg, if D1 = D3 = '0', then port B and upper port C act as output ports.

D2 is used for mode selection for group B (Port B and Lower Port C).
When D2 = '0', mode 0 is selected and when D2 = '1', mode 1 is selected.
D5, D6 are used for mode selection for group A (Upper Port C and Port A). The format is as follows:

D6	D5	mode
0	0	0
0	1	1
1	x	2

BSR Mode of 8255

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

This mode is selected by making D7='0'.
D0 is used for bit set/reset. When D0= '1', the port C bit selected (selection of a port C bit is shown in the next point) is SET, when D0 = '0', the port C bit is RESET.
D1, D2, D3 are used to select a particular port C bit whose value may be altered using D0 bit as mentioned above. The selection of the port C bits is done as follows:

D3	D2	D1	bit/pin of port C selected
0	0	0	PC0
0	0	1	PC1
0	1	0	PC2
0	1	1	PC3
1	0	0	PC4
1	0	1	PC5
1	1	0	PC6
1	1	1	PC7

D4, D5, D6 are not used.

I/O Modes of 8255

Mode 0 : Simple Input or Output

In this mode, Port A and Port B are used as two simple 8-bit I/O ports and Port C as two 4-bit I/O ports. Each port (or half-port, in case of Port C) can be programmed to function as simply an input port or an output port. The input/output features in mode 0 are: Outputs are latched, Inputs are not latched. Ports do not have handshake or interrupt capability.

Mode 1 : Input or Output with handshake

In mode 1, handshake signals are exchanged between the microprocessor and peripherals prior to data transfer. The ports (A and B) function as 8-bit I/O ports. They can be configured either as input or output ports. Each port (Port A and Port B) uses 3 lines from port C as handshake signals. The remaining two lines of port C can be used for simple I/O functions. Input and output data are latched and Interrupt

logic is supported.

Input control signals

STB (Strobe Input) : This signal (active low) is generated by a peripheral device that it has transmitted a byte of data. The 8255, in response to, generates IBF and INTR.

IBF (Input buffer full) : This signal is an acknowledgement by the 8255 to indicate that the input latch has received the data byte. This is reset when the microprocessor reads the data.

INTR (Interrupt Request) : This is an output signal that may be used to interrupt the microprocessor. This signal is generated if STB, IBF and INTE are all at logic 1.

INTE (Interrupt Enable) : This is an internal flip-flop to a port and needs to be set to generate the INTR signal. The two flip-flops INTEA and INTEB are set /reset using the BSR mode. The INTEA is enabled or disabled through PC4, and INTEB is enabled or disabled through PC2.

OBF (Output Buffer Full) : This is an output signal that goes low when the microprocessor writes data into the output latch of the 8255. This signal indicates to an output peripheral that new data is ready to be read. It goes high again after the 8255 receives a signal from the peripheral.

ACK (Acknowledge) : This is an input signal from a peripheral that must output a low when the peripheral receives the data from the 8255 ports.

INTR (Interrupt Request) : This is an output signal, and it is set by the rising edge of the signal. This signal can be used to interrupt the microprocessor to request the next data byte for output. INTE (Interrupt Enable) : This is an internal flip-flop to a port and needs to be set to generate the INTR signal. The two flip-flops INTEA and INTEB are set /reset using the BSR mode. The INTEA signal can be enabled or disabled through PC6, and INTEB is enabled or disabled through PC2.

Mode 2: Bidirectional Data Transfer

This mode is used primarily in applications such as data transfer between the two computers or floppy disk controller interface. Port A can be configured as the bidirectional port and Port B either in mode 0 or mode 1. Port A uses five signals from Port C as handshake signals for data transfer. The remaining three lines from Port C can be used either as simple I/O or as handshake signals for Port B.

Interfacing Keyboard

Getting meaningful data from a keyboard, it requires the following three major tasks:

1. Detect a key press.

2. Debounce the key press.

3. Encode the key press

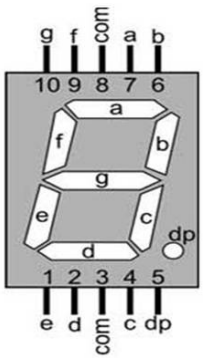
Display

7-segment display, it is composed of 8 LEDs, 7 segments are arranged as a rectangle for symbol displaying and there is an additional segment for decimal point displaying. In order to simplify connecting, anodes and cathodes of all diodes are connected to the common pin so that there are

Common Anode displays.

Common Cathode displays.

Segments are marked with the letters from A to G, plus DP, as shown in the figure below. On connecting, each diode is treated separately, which means that each must have its own current limiting resistor.



A seven segment display, as its name indicates, is composed of seven elements. Individually on or off, they can be combined to produce the representations numbers. In most applications, the seven segments are of nearly uniform shape and size, though in the case of adding machines, the vertical segments are longer and more oddly shaped at the ends in an effort to further enhance readability.

Since the seven segment display works on negative logic, we will have to provide logic 0 to the corresponding pin to make an LED glow. Table below shows the hex values used to display the different digits.

DIGIT	a	b	c	d	e	f	g	HEX Value
0	0	0	0	0	0	0	1	0x40
1	1	0	0	1	1	1	1	0xF9
2	0	0	1	0	0	1	0	0x24
3	0	0	0	0	1	1	0	0x30
4	1	0	0	1	1	0	0	0x19
5	0	1	0	0	1	0	0	0x12
6	0	1	0	0	0	0	0	0x02
7	0	0	0	1	1	1	1	0xF8

8	0	0	0	0	0	0	0	0x00
9	0	0	0	1	1	0	0	0x10

Assembly Language Program for seven segment display interface:

```
DATA SEGMENT

PORTA EQU 120H

PORTB EQU 121H

PORTC EQU 122H

CWRD EQU 123H

TABLE DB 8CH, 0C7H, 86H, 89H

DATA ENDS

CODE SEGMENT

ASSUME CS: CODE, DS:DATA

START: MOV AX, DATA; initialize data segment

MOV DS, AX

MOV AL, 80H; initialize 8255 port-b and port-c as o/p

MOV DX, CWRD

OUT DX, AL

MOV BH, 04; BH = no of digits to be displayed

LEA SI, TABLE; SI = starting address of lookup table

NEXTDIGIT: MOV CL, 08; CL = no of segments = 08

MOV AL, [SI]

NEXTBIT: ROL AL, 01

MOV CH, AL; save al

MOV DX, PORTB; one bit is sent out on portb

OUT DX, AL

MOV AL, 01

MOV DX, PORTC; one clock pulse sent on pc0
```

```
OUT DX, AL

DEC AL

MOV DX, PORTC

OUT DX, AL

MOV AL, CH; get the seven segment code back in al

DEC CL; send all 8 bits, thus one digit is displayed

JNZ NEXTBIT

DEC BH

INC SI; display all the four digits

JNZ NEXTDIGIT

MOV AH, 4CH; exit to dos

INT 21H

CODE ENDS

END START
```

INTERFACING ANALOG TO DIGITAL DATA CONVERTERS

The function of an A/D converter is to produce a digital word which represents the magnitude of some analog voltage or current. The specifications for an A/D converter are very similar to those for D/A converter. The resolution of an A/D converter refers to the number of bits in the output binary word. An 8-bit converter for example has a resolution of 1 part in 256. Accuracy and linearity specifications have the same meaning for an A/D converter as they do for a D/A converter. Another important specification for an ADC is its conversion time. This is simply the time it takes the converter to produce a valid output binary code for an applied input voltage. When we refer to a converter as high speed, we mean that it has a short conversion time.

The analog to digital converter is treated as an input device by the microprocessor that sends an initializing signal to the ADC to start the analog to digital data conversation process. The start of conversion signal is a pulse of a specific duration. The process of analog to digital conversion is a slow process, and the microprocessor has to wait for the digital data till the conversion is over. After the conversion is over, the ADC sends end of conversion (EOC) signal to inform the microprocessor that the conversion is over and the result is ready at the output buffer of the ADC. These tasks of issuing an SOC pulse to ADC, reading EOC signal from the ADC and reading the digital output of the ADC are carried out by the CPU

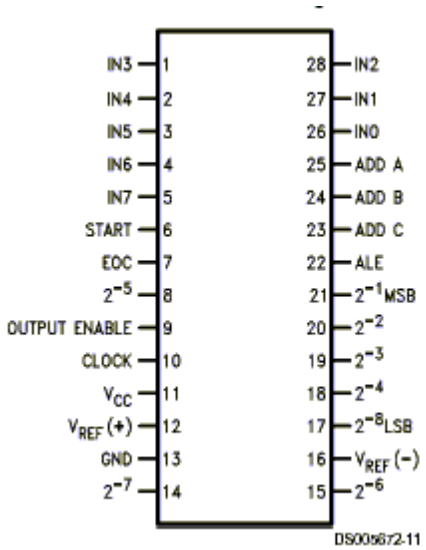
using 8255 I/O ports.

The time taken by the ADC from the active edge of SOC pulse (the edge at which the conversion process actually starts) till the active edge of EOC signal is called as the conversion delay of the ADC. In other words the time taken by the converter, to calculate the equivalent digital data output from the instant of the start of conversion is known as conversion delay. It may range anywhere from a few microseconds in case of fast ADCs to even a few hundred milliseconds in case of slow ADCs. A number of ADCs are available in the market, The selection of ADC for a particular application is done, keeping in mind the required speed, resolution range of operation, power supply requirements, sample and hold device requirements and the cost factors are considered.

The available ADCs in the market use different conversion techniques for the conversion of analog signals to digital signals. Parallel converter or flash converter, Successive approximation and dual slope integration techniques are the most popular techniques used in the integrated ADC chips. Whatever may be the technique used for conversion, a general algorithm for ADC interfacing contains the following steps.

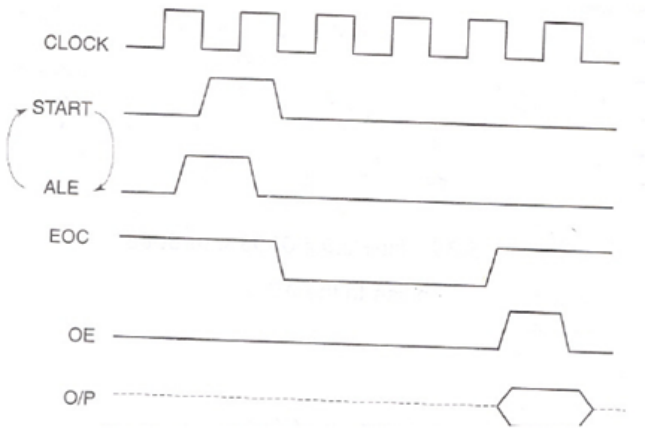
1. Ensure the stability of analog input, applied to the ADC.
2. Issue start of conversion (SOC) pulse to ADC.
3. Read end of conversion (EOC) signal to mark the end of conversion process.
4. Read digital data output of the ADC as equivalent digital output.

It may be noted that analog input voltage must be constant at the input of the ADC right from the start of conversion till the end of conversion to get correct results. This may be ensured by a sample and hold circuit which samples the analog signal and holds it constant for specified time duration. The microprocessor may issue a hold signal to the sample and Hold circuit. If the applied input changes before the complete conversion process is over, the digital equivalent of the analog input calculated by the ADC may not be correct.



I/P0-I/P7 Analog inputs
ADD A, B, C
O_7 - O_0 Digital 8-bit output with O_7 MSB and O_0 LSB
SOC Start of conversion signal pin
EOC End of conversion signal pin
OE Output latch enable pin, if high enables output
CLK Clock input for ADC
Vcc, GND Supply pins +5V and GND
Vref+ and Vref- Reference voltage positive (+5 Volts max.) and Reference voltage negative (0V minimum)

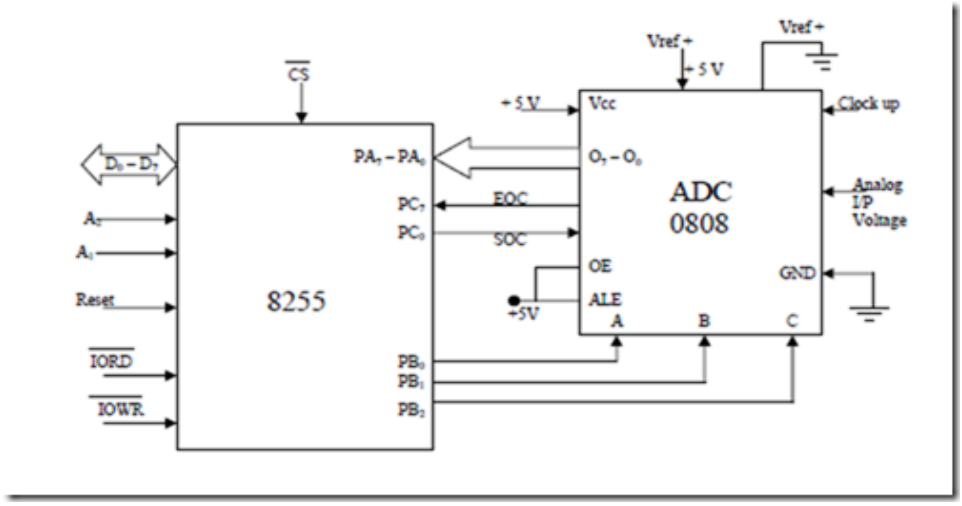
Some electrical specifications of ADC 0808/0809.
Minimum SOC pulse width 100ns
Minimum ALE pulse width 100ns
Clock frequency 10 to 1280 KHz
Conversion time 100μs at 640kHz
Resolution 8-bit
Error ±1 LSB
V_{ref}^{+} Not more than +5V
V_{ref}^{-} Not less than GND
$+V_{cc}$ supply +5V DC
Logical 1 i/p voltage minimum Vcc -1.5V
Logical 0 i/p voltage maximum 1.5V
Logical 1 o/p voltage minimum Vcc -0.4V
Logical 0 o/p voltage maximum 0.45V



Timing Diagram of ADC 0808/0809

Example: Interface ADC 0808 with 8086 using 8255 ports. Use Port A of 8255 for transferring digital data output of ADC to the CPU and Port C for control signals. Assume that an analog input is present at I/P2 of the ADC and a clock input of suitable frequency is available for ADC. Draw the schematic and write required ALP.
Solution: Following Figure shows the interfacing connections of ADC0808 with 8086

using 8255. The analog input I/P2 is used and therefore address pins A, B, C should be 0,1,0 respectively to select I/P2. The OE and ALE pins are already kept at +5V to select the ADC and enable the outputs. Port C upper acts as the input port to receive the EOC signal while port C lower acts as the output port to send SOC to the ADC.



Interfacing the 0808 with 8255

The required ALP is given as follows:

```
MOV AL, 98 H ; Initialization of 8255
OUT CWR, AL ;
MOV AL, 02 H ; Select I/P 2 as analog
OUT Port B, AL ; input.
MOV AL,00H ; Give start of conversion
OUT Port C,AL ; pulse to the ADC
MOV AL,01H
OUT Port C,AL
Wait: IN AL, PortC ; Check for EOC by
RCR ; reading port C upper and rotate through carry
JNC Wait
IN AL, PortA ; If EOC, read digital equivalent in AL
HLT ; Stop
```

INTERFACING DIGITAL TO ANALOG ONVERTERS:

The digital to analog converters convert binary numbers into their analog equivalent voltages or currents. Several techniques are employed for digital to analog conversion.

i. Weighted resistor network
ii. R-2R ladder network
iii. Current output D/A converter

The DAC find applications in areas like digitally controlled gains, motor speed control, programmable gain amplifiers, digital voltmeters, panel meters, etc. D/A converter have many applications besides those where they are used with a microcomputer. In a compact disk audio player for example a 14-or16-bit D/A converter is used to

convert the binary data read off the disk by a laser to an analog audio signal. Most speech synthesizer integrated circuits contain a D/A converter to convert stored binary data words into analog audio signals. Characteristics

1. Resolution: It is a change in analog output for one LSB change in digital input.

It is given by$(1/2^n)*V_{ref}$. If n=8 (i.e.8-bit DAC)

1/256*5V=39.06mV

2. Settling time: It is the time required for the DAC to settle for a full scale code change.

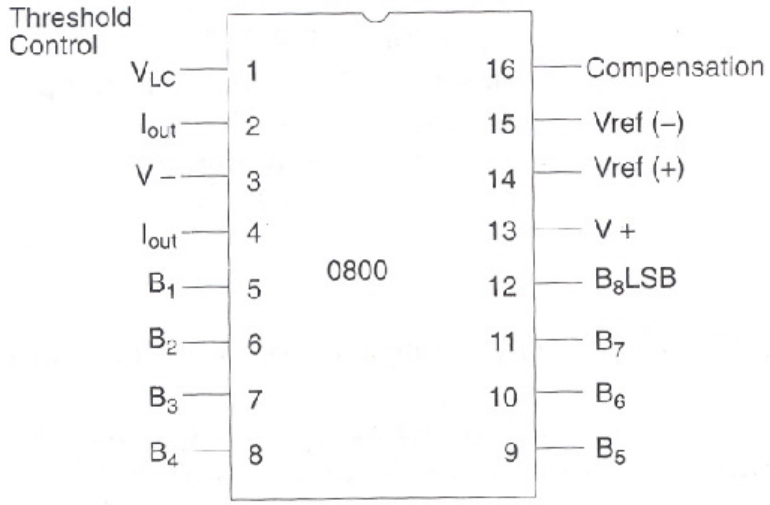
DAC 0800 8-bit Digital to Analog converter Features:

i. DAC0800 is a monolithic 8-bit DAC manufactured by National semiconductor.

ii. It has settling time around 100ms

iii. It can operate on a range of power supply voltage i.e. from 4.5V to +18V. Usually the supply V^+ is 5V or +12V. The V- pin can be kept at a minimum of -12V.

iv. Resolution of the DAC is 39.06mV



Pin Diagram of DAC0800

Communication Interface:

Serial Communication Standards

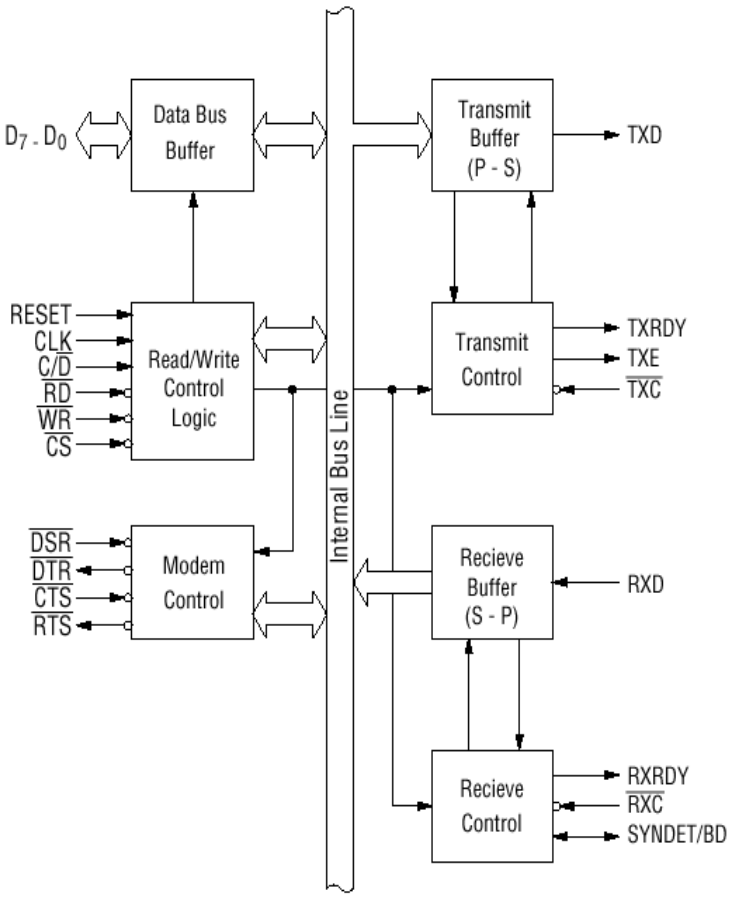
Serial Data Transfer Schemes

UART	USART
UART requires only data signal	In USART, Synchronous mode requires both data and a clock.
In UART, the data does not have to be transmitted at a fixed rate.	In USART's synchronous mode, the data is transmitted at a fixed rate.
In UART, data is normally transmitted	In USART, Synchronous data is

one byte at a time.	normally transmitted in the form of blocks
In UART, data transfer speed is set around specific values like 4800, 9600, 38400 bps, etc.	Synchronous mode allows for a higher DTR (data transfer rate) than asynchronous mode does, if all other factors are held constant.
UART speed is limited around 115200 bps	USART is faster than 115kb
Full duplex	Half duplex

8251 USART Architecture and Interfacing

The 8251 is a USART (Universal Synchronous Asynchronous Receiver Transmitter) for serial data communication. As a peripheral device of a microcomputer system, the 8251 receives parallel data from the CPU and transmits serial data after conversion. This device also receives serial data from the outside and transmits parallel data to the CPU after conversion.



Block diagram of the 8251 USART (Universal Synchronous Asynchronous Receiver

Transmitter)

The 8251 functional configuration is programmed by software. Operation between the 8251 and a CPU is executed by program control. Table 1 shows the operation between a CPU and the device.

$\overline{CS}$	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	
1	×	×	×	Data Bus 3-State
0	×	1	1	Data Bus 3-State
0	1	0	1	Status → CPU
0	1	1	0	Control Word ← CPU
0	0	0	1	Data → CPU
0	0	1	0	Data ← CPU

Table 1 Operation between a CPU and 8251

Control Words

There are two types of control word.
1. Mode instruction (setting of function)
2. Command (setting of operation)

1) Mode Instruction
Mode instruction is used for setting the function of the 8251. Mode instruction will be in "wait for write" at either internal reset or external reset. That is, the writing of a control word after resetting will be recognized as a "mode instruction."
Items set by mode instruction are as follows:
• Synchronous/asynchronous mode
• Stop bit length (asynchronous mode)
• Character length
• Parity bit
• Baud rate factor (asynchronous mode)
• Internal/external synchronization (synchronous mode)
• Number of synchronous characters (Synchronous mode)
The bit configuration of mode instruction is shown in Figures 2 and 3. In the case of synchronous mode, it is necessary to write one-or two byte sync characters. If sync characters were written, a function will be set because the writing of sync characters constitutes part of mode instruction.

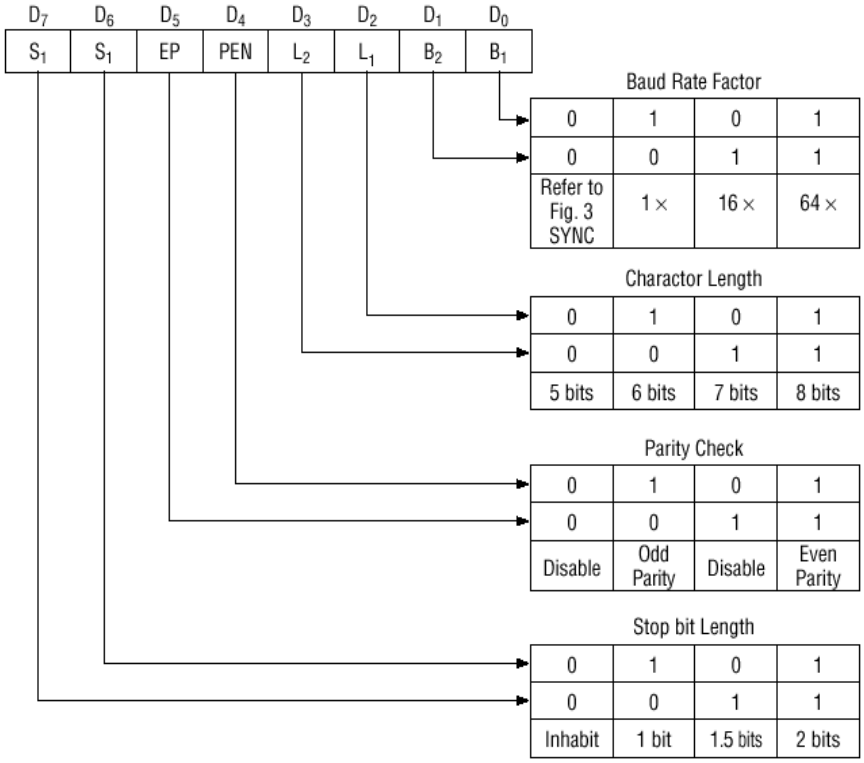


Fig. 2 Bit Configuration of Mode Instruction (Asynchronous)

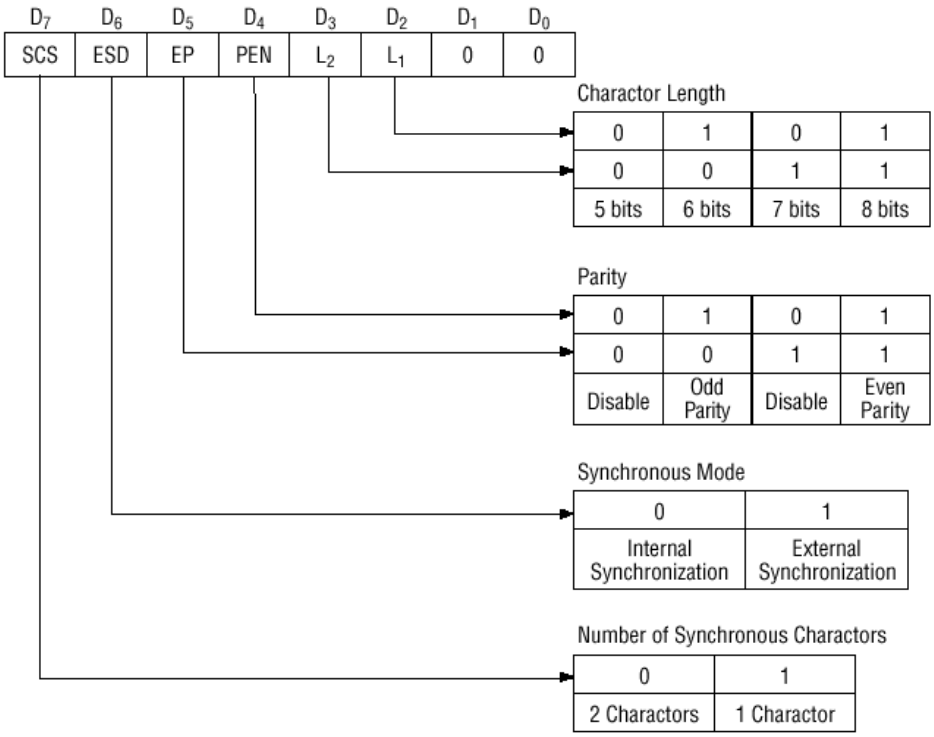


Fig. 3 Bit Configuration of Mode Instruction (Synchronous)

2) Command

Command is used for setting the operation of the 8251. It is possible to write a command whenever necessary after writing a mode instruction and sync characters. Items to be set by command are as follows:

- Transmit Enable/Disable
- Receive Enable/Disable
- DTR, RTS Output of data.
- Resetting of error flag.
- Sending to break characters
- Internal resetting
- Hunt mode (synchronous mode)

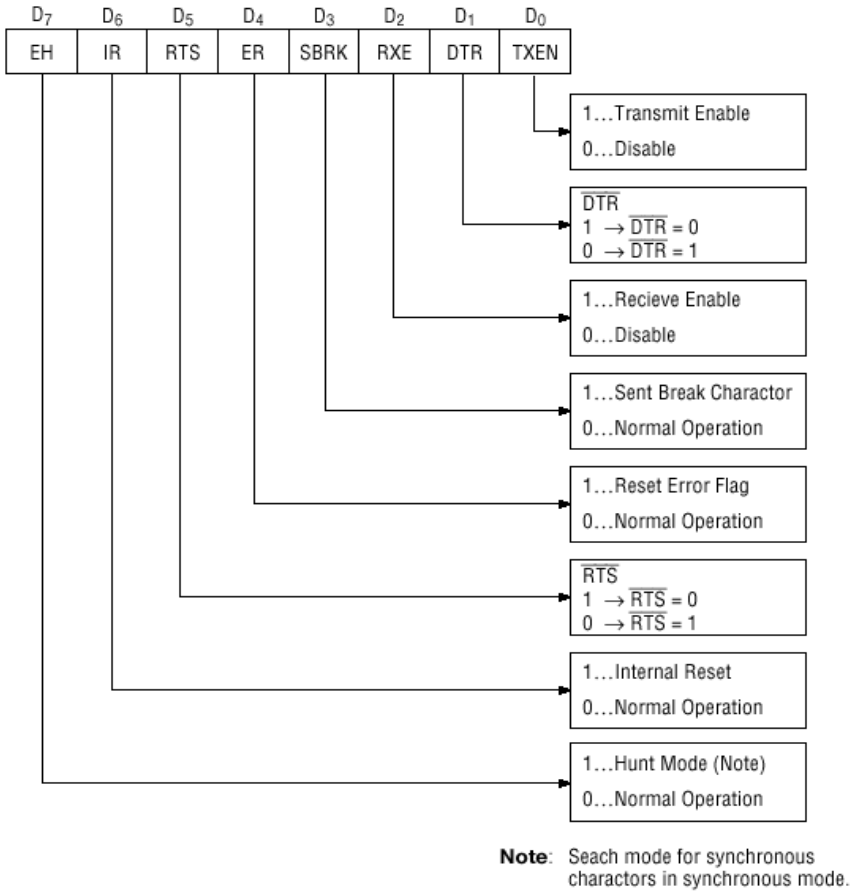


Fig. 4 Bit Configuration of Command

Status Word

It is possible to see the internal status of the 8251 by reading a status word. The bit configuration of status word is shown in Fig. 5.

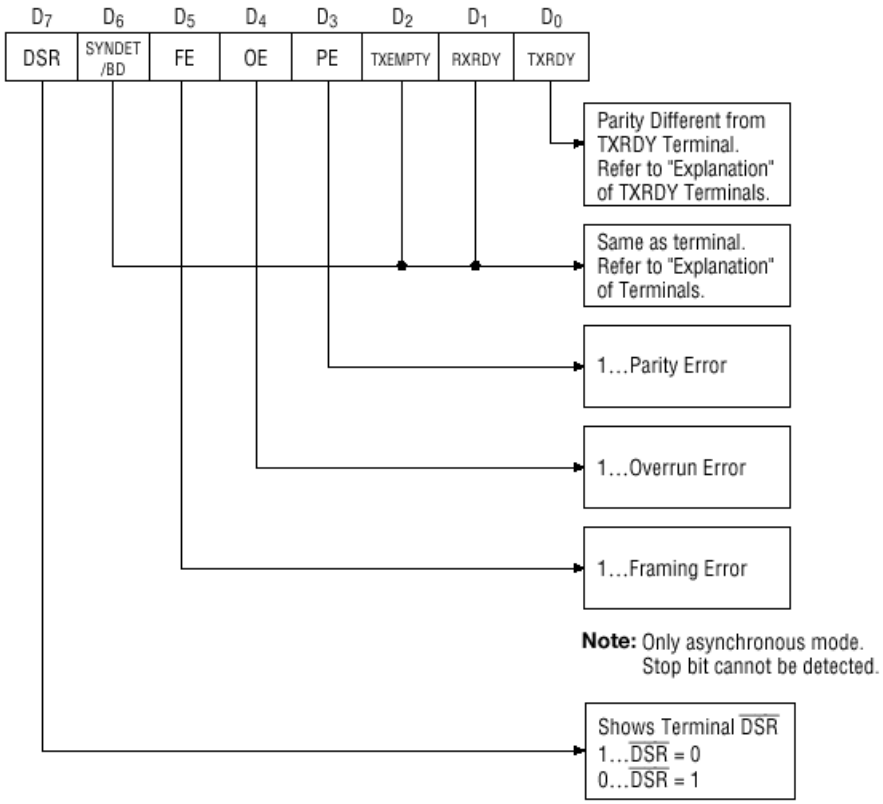


Fig. 5 Bit Configuration of Status Word

Pin Description

D 0 to D 7 (I/O terminal)

This is bidirectional data bus which receives control words and transmits data from the CPU and sends status words and received data to CPU.

RESET (Input terminal)

A "High" on this input forces the 8251 into "reset status." The device waits for the writing of "mode instruction." The min. reset width is six clock inputs during the operating status of CLK.

CLK (Input terminal)

CLK signal is used to generate internal device timing. CLK signal is independent of RXC or TXC. However, the frequency of CLK must be greater than 30 times the RXC and TXC at Synchronous mode and Asynchronous "x1" mode, and must be greater than 5 times at Asynchronous "x16" and "x64" mode.

WR (Input terminal)

This is the "active low" input terminal which receives a signal for writing transmit data and control words from the CPU into the 8251.

RD (Input terminal)

This is the "active low" input terminal which receives a signal for reading receive data and status words from the 8251.

C/D (Input terminal)

This is an input terminal which receives a signal for selecting data or command words and status words when the 8251 is accessed by the CPU. If C/D = low, data will be accessed. If C/D = high, command word or status word will be accessed.

CS (Input terminal)

This is the "active low" input terminal which selects the 8251 at low level when the CPU accesses. Note: The device won’t be in "standby status"; only setting CS = High.

TXD (output terminal)

This is an output terminal for transmitting data from which serial-converted data is sent out. The device is in "mark status" (high level) after resetting or during a status when transmit is disabled. It is also possible to set the device in "break status" (low level) by a command.

TXRDY (output terminal)

This is an output terminal which indicates that the 8251is ready to accept a transmitted data character. But the terminal is always at low level if CTS = high or the device was set in "TX disable status" by a command. Note: TXRDY status word indicates that transmit data character is receivable, regardless of CTS or command. If the CPU writes a data character, TXRDY will be reset by the leading edge or WR signal.

TXEMPTY (Output terminal)

This is an output terminal which indicates that the 8251 has transmitted all the characters and had no data character. In "synchronous mode," the terminal is at high level, if transmit data characters are no longer remaining and sync characters are automatically transmitted. If the CPU writes a data character, TXEMPTY will be reset by the leading edge of WR signal. Note : As the transmitter is disabled by setting CTS "High" or command, data written before disable will be sent out. Then TXD and

TXEMPTY will be "High". Even if a data is written after disable, that data is not sent out and TXE will be "High".After the transmitter is enabled, it sent out. (Refer to Timing Chart of Transmitter Control and Flag Timing)

TXC (Input terminal)

This is a clock input signal which determines the transfer speed of transmitted data. In "synchronous mode," the baud rate will be the same as the frequency of TXC. In "asynchronous mode", it is possible to select the baud rate factor by mode instruction. It can be 1, 1/16 or 1/64 the TXC. The falling edge of TXC sifts the serial data out of the 8251.

RXD (input terminal)

This is a terminal which receives serial data.

RXRDY (Output terminal)

This is a terminal which indicates that the 8251 contains a character that is ready to READ. If the CPU reads a data character, RXRDY will be reset by the leading edge of RD signal. Unless the CPU reads a data character before the next one is received completely, the preceding data will be lost. In such a case, an overrun error flag status word will be set.

RXC (Input terminal)

This is a clock input signal which determines the transfer speed of received data. In "synchronous mode," the baud rate is the same as the frequency of RXC. In "asynchronous mode," it is possible to select the baud rate factor by mode instruction. It can be 1, 1/16, 1/64 the RXC.

SYNDET/BD (Input or output terminal)

This is a terminal whose function changes according to mode. In "internal synchronous mode." this terminal is at high level, if sync characters are received and synchronized. If a status word is read, the terminal will be reset. In "external synchronous mode, "this is an input terminal. A "High" on this input forces the 8251 to start receiving data characters.

In "asynchronous mode," this is an output terminal which generates "high level"output upon the detection of a "break" character if receiver data contains a "low -level" space between the stop bits of two continuous characters. The terminal will be reset, if RXD is at high level. After Reset is active, the terminal will be output at low level.

DSR (Input terminal)

This is an input port for MODEM interface. The input status of the terminal can be recognized by the CPU reading status words.

DTR (Output terminal)

This is an output port for MODEM interface. It is possible to set the status of DTR by a command.

CTS (Input terminal)

This is an input terminal for MODEM interface which is used for controlling a transmit circuit. The terminal controls data transmission if the device is set in "TX Enable" status by a command. Data is transmitable if the terminal is at low level.

RTS (Output terminal)

This is an output port for MODEM interface. It is possible to set the status RTS by a command.

Interfacing with advanced devices:

Memory Interfacing to 8086

We have four common types of memory:

1. Read only memory (ROM)
2. Flash memory (EEPROM)
3. Static Random access memory (SARAM)
4. Dynamic Random access memory (DRAM)

Pin connections common to all memory devices are: The address input, data output or input/outputs, selection input and control input used to select a read or write operation.

Address connections: All memory devices have address inputs that select a memory location within the memory device. Address inputs are labeled from A0 to An.

Data connections: All memory devices have a set of data outputs or input/outputs. Today many of them have bi-directional common I/O pins.

Selection connections: Each memory device has an input, that selects or enables the memory device. This kind of input is most often called a chip select (CS), chip enable (CE) or simply select (S) input

RAM memory generally has at least one CS or S input and ROM at least one CE .

If the CE, CS, S input is active the memory device perform the read or write.

If it is inactive the memory device cannot perform read or write operation.

If more than one CS connection is present, all most be active to perform read or write data.

Control connections: A ROM usually has only one control input, while a RAM often has one or two control inputs.

The control input most often found on the ROM is the output enable (OE) or gate (G), this allows data to flow out of the output data pins of the ROM.

If OE and the selected input are both active, then the output is enable, if OE is inactive, the output is disabled at its high-impedance state.

The OE connection enables and disables a set of three-state buffer located within the memory device and must be active to read data.

A RAM memory device has either one or two control inputs. If there is one control input it is often called R/ W.

This pin selects a read operation or a write operation only if the device is selected by the selection input (CS).

If the RAM has two control inputs, they are usually labeled WE or W and OE or G.

(WE) write enable must be active to perform a memory write operation and OE must be active to perform a memory read operation.

When these two controls WE and OE are present, they must never be active at the same time.

The ROM read only memory permanently stores programs and data and data was always present, even when power is disconnected.

It is also called as nonvolatile memory.

EPROM (erasable programmable read only memory) is also erasable if exposed to high intensity ultraviolet light for about 20 minutes or less, depending upon the type of EPROM.

We have PROM (programmable read only memory)

RMM (read mostly memory) is also called the flash memory.

The flash memory is also called as an EEPROM (electrically erasable programmable ROM), EAROM (electrically alterable ROM), or a NOVROM (nonvolatile ROM).

These memory devices are electrically erasable in the system, but require more time to erase than a normal RAM.

EPROM contains the series of 27XXX contains the following part numbers :

2704(512 * 8), 2708(1K * 8), 2716(2K * 8), 2732(4K * 8), 2764(8K * 8), 27128(16K * 8) etc.

Each of these parts contains address pins, eight data connections, one or more chip selection inputs (CE) and an output enable pin (OE).

This device contains 11 address inputs and 8 data outputs.

If both the pin connection CE and OE are at logic 0, data will appear on the output connection . If both the pins are not at logic 0, the data output connections remains at their high impedance or off state.

To read data from the EPROM Vpp pin must be placed at logic 1.

SRAM

Static RAM memory device retain data for as long as DC power is applied. Because no special action is required to retain stored data, these devices are called as static memory. They are also called volatile memory because they will not retain data without power.

The main difference between a ROM and RAM is that a RAM is written under normal operation, while ROM is programmed outside the computer and is only normally read.

The SRAM stores temporary data and is used when the size of read/write memory is relatively small.

The semiconductor RAM is broadly two types – Static RAM and Dynamic RAM.

The semiconductor memories are organized as two dimensional arrays of memory locations.

For example 4K * 8 or 4K byte memory contains 4096 locations, where each locations contains 8-bit data and only one of the 4096 locations can be selected at a time. Once a location is selected all the bits in it are accessible using a group of conductors called Data bus.

For addressing the 4K bytes of memory, 12 address lines are required.

In general to address a memory location out of N memory locations, we will require at least n bits of address, i.e. n address lines where n = Log2 N.

Thus if the microprocessor has n address lines, then it is able to address at the most N locations of memory, where 2n=N. If out of N locations only P memory locations are to be interfaced, then the least significant p address lines out of the available n

lines can be directly connected from the microprocessor to the memory chip while the remaining (n-p) higher order address lines may be used for address decoding as inputs to the chip selection logic.

The memory address depends upon the hardware circuit used for decoding the chip select (CS). The output of the decoding circuit is connected with the CS pin of the memory chip.

The general procedure of static memory interfacing with 8086 is briefly described as follows:

Arrange the available memory chip so as to obtain 16- bit data bus width. The upper 8-bit bank is called as odd address memory bank and the lower 8-bit bank is called as even address memory bank.

Connect available memory address lines of memory chip with those of the microprocessor and also connect the memory RD and WR inputs to the corresponding processor control signals. Connect the 16-bit data bus of the memory bank with that of the microprocessor 8086.

The remaining address lines of the microprocessor, BHE and A0 are used for decoding the required chip select signals for the odd and even memory banks. The CS of memory is derived from the o/p of the decoding circuit.

As a good and efficient interfacing practice, the address map of the system should be continuous as far as possible, i.e. there should not be no windows in the map and no fold back space should be allowed.

A memory location should have a single address corresponding to it, i.e. absolute decoding should be preferred and minimum hardware should be used for decoding.

Dynamic RAM

Whenever a large capacity memory is required in a microcomputer system, the memory subsystem is generally designed using dynamic RAM because there are various advantages of dynamic RAM.

E.g. higher packing density, lower cost and less power consumption. A typical static RAM cell may require six transistors while the dynamic RAM cell requires only a transistors along with a capacitor. Hence it is possible to obtain higher packaging density and hence low cost units are available.

The basic dynamic RAM cell uses a capacitor to store the charge as a representation of data. This capacitor is manufactured as a diode that is reverse-biased so that the storage capacitance comes into the picture.

This storage capacitance is utilized for storing the charge representation of data but the reverse-biased diode has leakage current that tends to discharge the capacitor

giving rise to the possibility of data loss. To avoid this possible data loss, the data stored in a dynamic RAM cell must be refreshed after a fixed time interval regularly. The process of refreshing the data in RAM is called as Refresh cycle.

The refresh activity is similar to reading the data from each and every cell of memory, independent of the requirement of microprocessor. During this refresh period all other operations related to the memory subsystem are suspended. Hence the refresh activity causes loss of time, & results in reduce of system performance.

However keeping in view the advantages of dynamic RAM, like low power consumption, high packaging density and low cost, most of the advanced computing system are designed using dynamic RAM, at the cost of operating speed.

A dedicated hardware chip called as dynamic RAM controller is the most important part of the interfacing circuit.

The Refresh cycle is different from the memory read cycle in the following aspects.

1. The memory address is not provided by the CPU address bus, rather it is generated by a refresh mechanism counter called as refresh counter.

2. Unlike memory read cycle, more than one memory chip may be enabled at a time so as to reduce the number of total memory refresh cycles.

3. The data enable control of the selected memory chip is deactivated, and data is not allowed to appear on the system data bus during refresh, as more than one memory units are refreshed simultaneously. This is to avoid the data from the different chips to appear on the bus simultaneously.

4. Memory read is either a processor initiated or an external bus master initiated and carried out by the refresh mechanism.

Dynamic RAM is available in units of several kilobits to megabits of memory. This memory is arranged internally in a two dimensional matrix array so that it will have n rows and m columns. The row address n and column address m are important for the refreshing operation.

For example, a typical 4K bit dynamic RAM chip has an internally arranged bit array of dimension 64 * 64 , i.e. 64 rows and 64 columns. The row address and column address will require 6 bits each. These 6 bits for each row address and column address will be generated by the refresh counter, during the refresh cycles.

A complete row of 64 cells is refreshed at a time to minimizes the refreshing time. Thus the refresh counter needs to generate only row addresses. The row address are multiplexed, over lower order address lines.

The refresh signals act to control the multiplexer, i.e. when refresh cycle is in process the refresh counter puts the row address over the address bus for

refreshing. Otherwise, the address bus of the processor is connected to the address bus of DRAM, during normal processor initiated activities.

A timer, called refresh timer, derives a pulse for refreshing action after each refresh interval.

Refresh interval can be qualitatively defined as the time for which a dynamic RAM cell can hold data charge level practically constant, i.e. no data loss takes place.

Suppose the typical dynamic RAM chip has 64 rows, then each row should be refreshed after each refresh interval or in other words, all the 64 rows are to refreshed in a single refresh interval.

This refresh interval depends upon the manufacturing technology of the dynamic RAM cell. It may range anywhere from 1ms to 3ms.

Let us consider 2ms as a typical refresh time interval. Hence, the frequency of the refresh pulses will be calculated as follows:

Refresh Time (per row) tr = (2 * 10 -3) / 64.

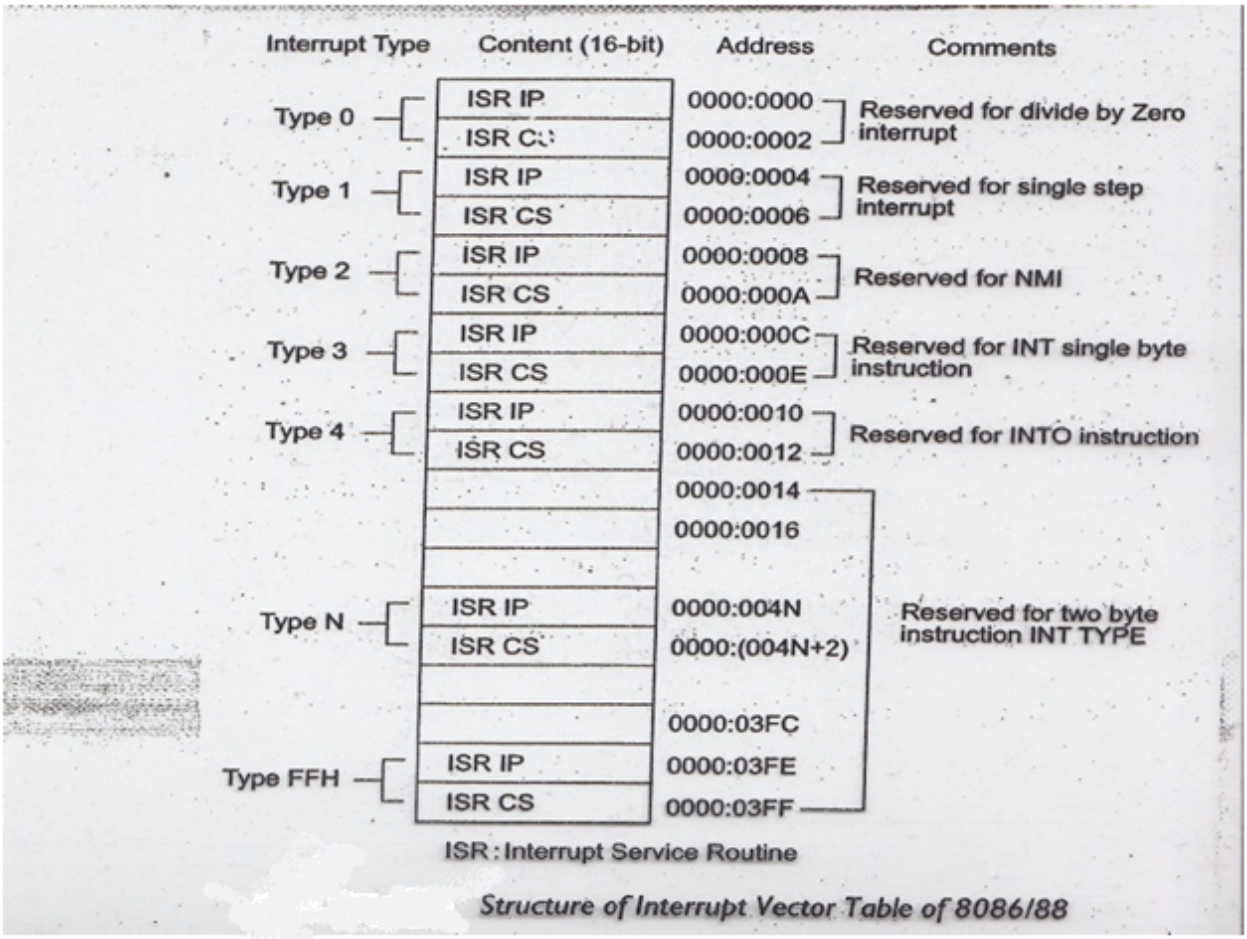
Refresh Frequency fr = 64 / (2 * 10 -3) = 32 * 103 Hz.

The following block diagram explains the refreshing logic and 8086 interfacing with dynamic RAM.

Each chip is of 16K * 1-bit dynamic RAM cell array. The system contains two 16K byte dynamic RAM units. All the address and data lines are assumed to be available from an 8086 microprocessor system.

Interrupt Structure of 8086

Vector Interrupt Table



Structure of Interrupt Vector Table of 8086/88

Type 0: Divide error – Division overflow or division by zero

Type 1: Single step or Trap – After the execution of each instruction when trap flag set

Type 2: NMI Hardware Interrupt – '1' in the NMI pin

Type 3: One-byte Interrupt – INT3 instruction (used for breakpoints)

Type 4: Overflow – INTO instruction with an overflow flag

Type 5: BOUND – Register contents out-of-bounds

Type 6: Invalid Opcode – Undefined opcode occurred in program

Type 7: Coprocessor not available – MSW indicates a coprocessor

Type 8: Double Fault – Two separate interrupts occur during the same instruction

Type 9: Coprocessor Segment Overrun – Coprocessor call operand exceeds FFFFH

Type 10: Invalid Task State Segment – TSS invalid (probably not initialized)

Type 11: Segment not present – Descriptor P bit indicates segment not present or invalid

Type 12: Stack Segment Overrun – Stack segment not present or exceeded

Type 13: General Protection – Protection violation in 286 (general protection fault)

Type 14: Page Fault – 80386 and above

Type 16: Coprocessor Error – ERROR′ = '0' (80386 and above)

Type 17: Alignment Check – Word/Doubleword data addressed at odd location (486 and above)

Type 18: Machine Check – Memory Management interrupt (Pentium and above)

Type 0 interrupts: This interrupt is also known as the divide by zero interrupt. The 8086 will automatically do a type 0 interrupt if the result of a DIV operation or an IDIV operation is too large to fit in the destination register. For a type 0 interrupt, the 8086 pushes the flag register on the stack, resets IF and TF and pushes the return addresses on the stack.

Type 1 interrupts: This is also known as the single step interrupt. The use of single step feature found in some monitor programs and debugger programs. When you tell a system to single step, it will execute one instruction and stop. If they are correct we can tell a system to single step, it will execute one instruction and stop. We can then examine the contents of registers and memory locations. In other words, when in single step mode a system will stop after it executes each instruction and wait for further direction from you. The 8086 trap flag and type 1 interrupt response make it quite easy to implement a single step feature direction.

Type 2 interrupts: also known as the non-maskable NMI interrupts. The 8086 will automatically do a type 2 interrupt response when it receives a low to high transition on its NMI pin. When it does a type 2 interrupt, the 8086 will push the flags on the stack, reset TF and IF, and push the CS value and the IP value for the next instruction on the stack. It will then get the CS value for the start of the type 2 interrupt service procedure from address 0000AH and the IP value for the start of the procedure from address 00008H.

Type 3 interrupts: These types of interrupts are also known as breakpoint interrupts. The type 3 interrupt is produced by execution of the INT3 instruction. The main use of the type 3 interrupt is to implement a breakpoint function in a system. When we insert a breakpoint, the system executes the instructions up to the breakpoint and then goes to the breakpoint procedure. Unlike the single step which stops execution after each instruction, the breakpoint feature executes all the instructions up to the inserted breakpoint and then stops execution.

Type 4 interrupts: Also known as overflow interrupts is generally existent after an arithmetic operation was performed. The 8086 overflow flag will be set if the signed result of an arithmetic operation on two signed numbers is too large to be

represented in the destination register or memory location. For example, if you add the 8 bit signed number 01101100 and the 8 bit signed number 010111101, the result will be 10111101. This would be the correct result if we were adding unsigned binary numbers, but it is not the correct signed result.

The characteristics of internal interrupts are as follows:

The type of code of an interrupt is either predefined or can be contained within the instruction itself.

In case of INTR interrupt inputs the generation of complementary INTA bus cycles are not generated.

No internal interrupt can be disabled in the case of such interrupts barring single step interrupts.

Priority Wise always the internal interrupts barring single step interrupts are always given higher priority as compared to external interrupts.

Software interrupts-type 0 through 255:

The 8086 INT instruction can be used to cause the 8086 to do any one of the 256 possible interrupt types. The desired interrupt type is specified as part of the instruction. The instruction INT32, for example will cause the 8086 to do a type 32 interrupt response. The 8086 will push the flag register on the stack, reset TF and IF, and push the CS and IP values of the next instruction on the stack.

INTR INTERRUPTS-TYPES 0 THROUGH 255:

The 8086 INTR input allows some external signal to interrupt execution of a program. Unlike the NMI input, however, INTR can be masked so that it cannot cause an interrupt. If the interrupt flag is cleared, then the INTR input is disabled. IF can be cleared at any time with CLEAR instruction.

PRIORITY OF 8086 INTERRUPTS:

If two or more interrupts occur at the same time then the highest priority interrupt will be serviced first, and then the next highest priority interrupt will be serviced. As a example suppose that the INTR input is enabled, the 8086 receives an INTR signal during the execution of a divide instruction, and the divide operation produces a divide by zero interrupt. Since the internal interrupts-such as divide error, INT, and INTO have higher priority than INTR the 8086 will do a divide error interrupt response first.

Interrupt Service Routine.

The processor jumps to a special program called Interrupt Service Routine to service the peripheral