Department of Electrical Engineering
Indian Institute of Technology Jodhpur

B.Tech. Project Report

Title of the B.Tech. Project : **Optimisation Of 32 Bit Adders**
Name of BTP Supervisor : **Dr. Shree Prakash Tiwari**

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Abstract

The aim of this B.Tech project is to compare the performance of different types of 32-bit adders in mainly three parameters, i.e. total time delay, total area and total power consumption because, for a different type of application, different parameters need to be optimised. Since 32-bit is the most common and widely used for digital systems and processors, in this project we have made a comparative analysis of six algorithms for adding two numbers of 32 bit each The adders implemented in this project are: Ripple Carry Adder, Carry Lookahead Adder[9], Carry Select Adder[2], Carry Skip Adder, Kogge Stone Adder[7] and Hybrid Adder. Comparative analysis of these architectures is done using Verilog HDL and Xilinx software.

Contents

1. Motivation

Adders are the most essential and fundamental blocks of ALU (arithmetic logic unit) and this arithmetic logic unit is the basic block of any embedded or non-embedded device. For every digital application, design of optimised adders is of high importance. There are different type of adders, each having different performance. Adder is selected depending on where the adder is to be used. They can be high in speed, less in area or less in power consumption. For various applications of VLSI, not only the speed but the area and power consumption also need to be optimised.

This project focuses on comparing the performance of different adders in different aspects.

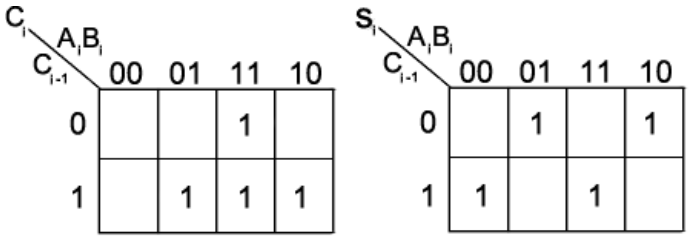
2. Objective

- To study and discuss some of the existing algorithms for 32-bit adders.
- To implement the methods by Verilog HDL using Xilinx.
- To compare the performance of adders based on factors like delay, area-LUTs and power consumption.

3. Algorithms for adders implemented

3.0 Full Adder

Its function is to add two 1-bit binary numbers. Its logic can be fabricated by K-map minimization and the resultant circuit is shown in figure (1). Here S denotes the sum of the two numbers and C_{out} represents the output carry signal.



$$S = A \oplus B \oplus C_{in}\ C_{Out} = A \bullet B + B \bullet C_{in} + A \bullet C_{out}$$

The delay occurred due to various gates can be understood by inspecting the circuit of a full adder. A full adder runs through one-2 input XOR gate, two-2 input AND gate, one XOR gate andone-2 input OR gate, so the total delay can be calculated as

$$T_F = T_{XOR} + T_{AND} + T_{OR} = D + D + D = 3D$$

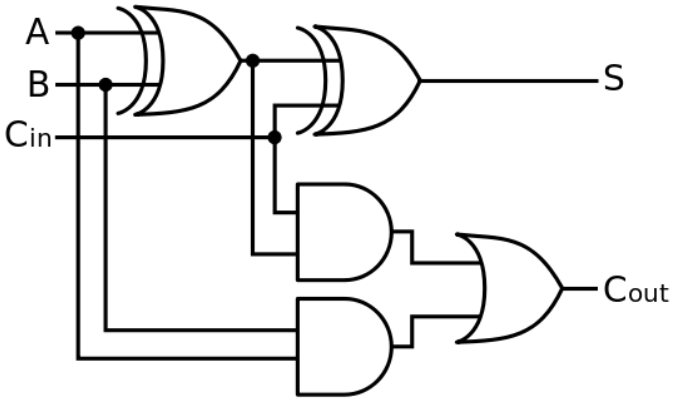


Figure (1): Full adder (Gate Level) [3]

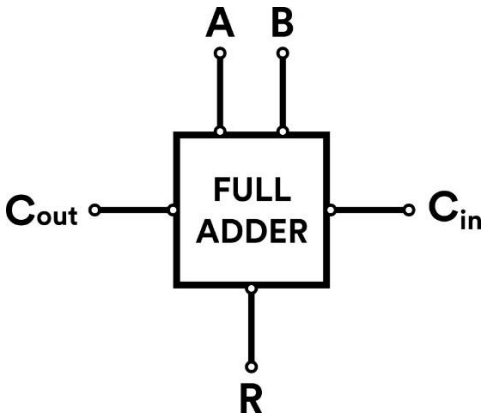


Figure (2): Full adder (Block diagram)

3.1 Ripple Carry Adder

A Ripple Carry adder used to add 2 numbers of n bits is a cascaded chain of n-single bit adders. Although the time required to add two numbers of size 32 bits is high, it takes the lowest area among all the adders. It is serial adder and the method of its working is similar to the approach followed while manually adding binary numbers.

3.1.1 Algorithm

In the ripple carry adder, each full adder takes input Ai, Bi (i: number of Full adder from right) and C_{in} (input carry). The input carry of i^{th} full adder is, in turn, is the C_{out} (Output carry) of the $i\text{-}1^{th}$ full adder. In this process, each carry bit passes (ripples) to the next full adder; therefore it is called Ripple Carry Adder. This algorithm is comparatively very slow and has a high value of delay, as each stage of full adder has to wait until the carry bit is calculated from the previous stage of a full adder. For ripple-carry adder of 32 bits, the total time delay is:

$$T_D = 32 \times T_F = 32 \times 3D = 96$$

3.1.2 Circuit

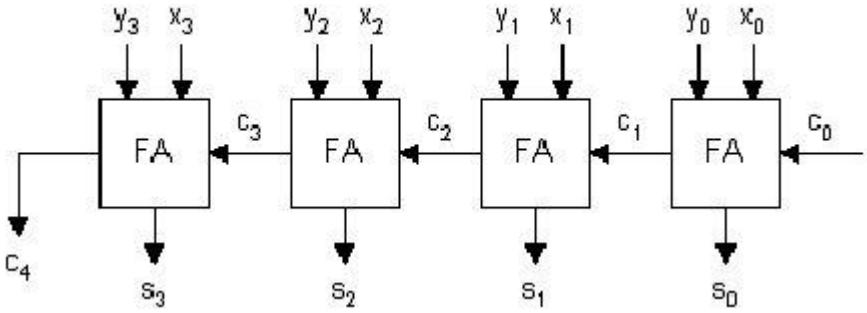


Figure (3): Block diagram of 4-bit Ripple Carry adder [5]

3.2 Carry-Lookahead Adder

Its logic is based on the concept of generation and propagation of carries. Generate means a carry will be produced in the sum, does not matter whether there is a carry at any less significant digit of the sum or not. Propagate means a carry signal is generated at a particular bit if there is a carry signal at the previous bit (having one less significance order).

3.2.1 Algorithm

For each bit of the binary numbers to be added, whether carry will be generated or propagated by a bit pair is determined by the look ahead logic. Due to this, the carry can be determined without waiting for previous carries to be processed. This greatly reduces the time delay in generating output carry signal. The carry-lookahead logic is explained below with an example of 4-bit number.

$$G_i = A_i \cdot B_i$$
$$P_i = A \oplus \mathrm{B}$$
$$C_1 = G_0 + P_0 \cdot C_0$$
$$C_2 = G_1 + P_1 \cdot C_1$$
$$C_3 = G_2 + P_2 \cdot C_2$$
$$C_4 = G_3 + P_3 \cdot C_3$$

Substituting C_1 in C_2, C_2 inC_3 andC_3 inC_4, the equations get modified as follows:

$$C_1 = G_0 + P_0 \cdot C_0$$
$$C_2 = G_1 + G_0 \cdot P_1 + P_0 \cdot C_0 \cdot P_1$$
$$C_3 = G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + C_0 \cdot P_0 \cdot P_1 \cdot P_2$$
$$C_4 = G_3 + G_2 \cdot P_3 + G_1 \cdot P_2 \cdot P_3 + G_0 \cdot P_1 \cdot P_2 \cdot P_3 + C_0 \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3$$

3.2.2 Circuit

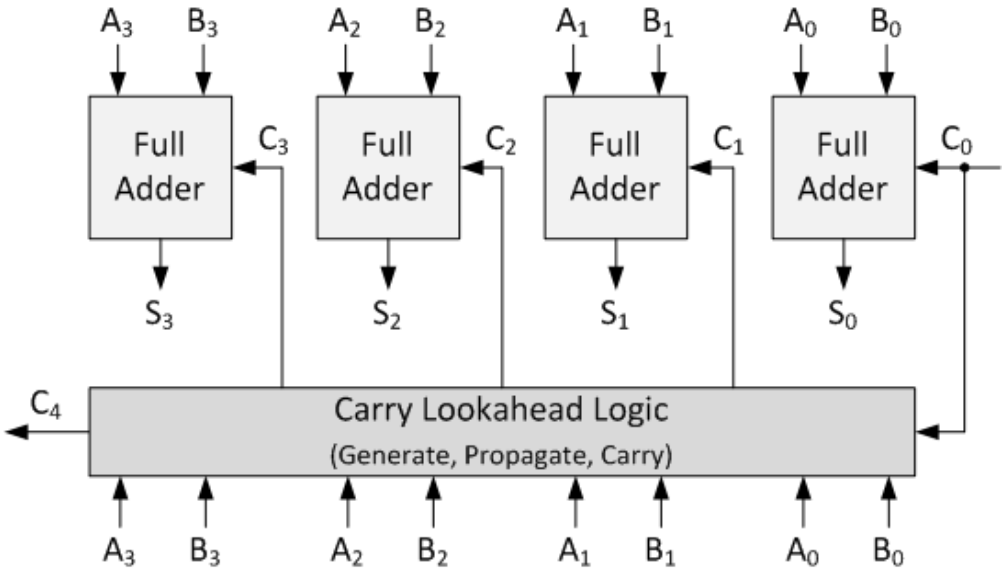


Figure (4): Block diagram of Carry Lookahead adder adding 2 numbers of 4 bits

3.3 Carry Select Adder

It is a fast adder based on parallel addition concept with less delay that adds two numbers of n bit in size.

3.3.1 Algorithm

This adder adds two numbers with the help of ripple carry adders and multiplexers. It calculates the sum of two numbers twice in a parallel manner assuming carry to be zero for one time, and one for other. The resultant sum and carry out is selected with the help of a 2x1 MUX after results are generated. The diagram for the addition of numbers of 4 bits is shown below. For 32-bit addition, 7 4-bit adders are attached serially, and the first 4-bits are calculated using a simple ripple carry adder because the carry is known for first 4 bits of addition. The total delay in the signal produced by this adder will be the sum of 4 times delay of the full adder and 7 times MUX delay. The area of this adder will be two times of the area of a single ripple carry adder plus 35(7x5) times 2x1 MUX area.

3.3.2 Circuit

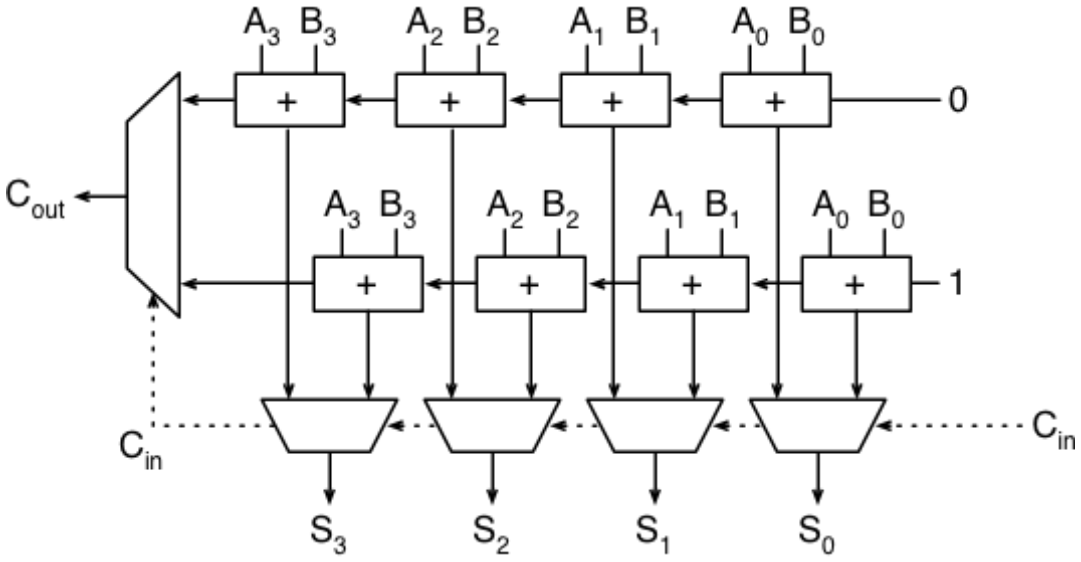


Figure (5): Diagram of 4-bit addition using carry select adder [6]

3.4 Carry Skip Adder

It improves performance of the ripple-carry adder with comparatively less effort than other algorithms.

3.4.1 Algorithm

Carry skip adder of n bit comprises bit ripple-carry adder chain of size n bits, an AND gate with n inputs, and a MUX. Every propagate bit obtained from the ripple carry chain is given input to the AND gate. The output signal generated by AND gate is known as “block propagate” which is given as input to select line of a 2x1 MUX, which gives output equal to either C_n or C_o.

$$s = p_{n-1} \cdot p_{n-2} \cdots \cdot p_1 \cdot p_0 = p_{[0:n-1]}$$

By using multiple blocks of skip logic to form multiple layers, the adder becomes even faster. For 32-bit adder, 8 layers of skip-blocks of 4-bits each are connected in series.

3.4.2 Circuit

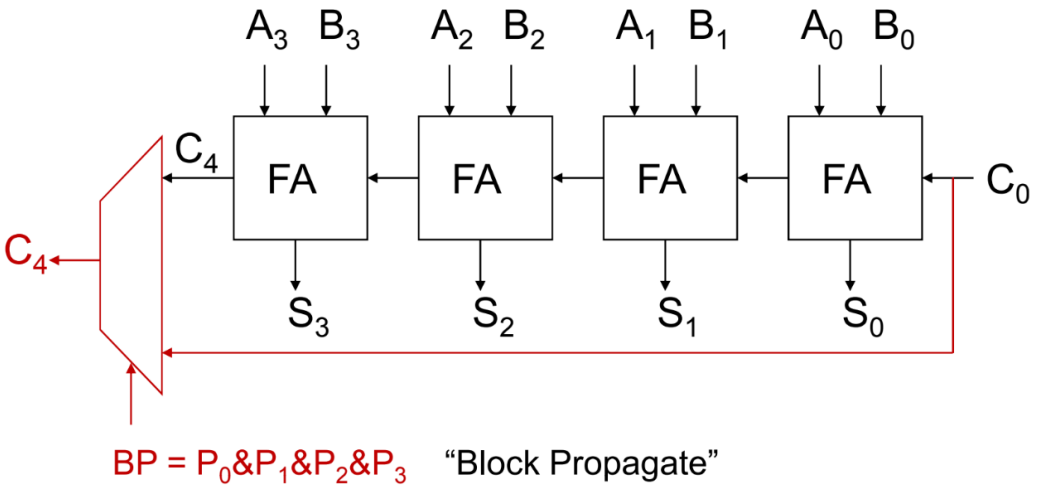


Figure (6): addition using 4-bit carry skip adder [8]

3.5 Kogge Stone Adder

It is an adder of the type Parallel Prefix adders, which are based on the associative property of addition. Different processes are carried out in a parallel way, which increases hardware requirement, but decreases the delay time. This adder is a high speed adder and is very widely used in industries in arithmetic circuits.

3.5.1 Algorithm

The algorithm for all the parallel prefix adders is almost the same, the main difference comes in parallel connecting capacity, fan out, etc. The general steps [7] are:

(1) Before Processing:

In this stage, generate signal and propagate signal is produced. The logic equations are:

$$G_i = A_i \cdot B_i$$

$$P_i = A \oplus B$$

(2) Generation stage:

Carries of each bit are calculated in this stage. The operation is executed in parallel. The carry propagates and carry generate are used as intermediate signals. The logic equations are as shown below.

$$CP_{i:j} = P_{i:k+1} \cdot G_{k:j}$$
$$CG_{i:j} = G_{i:k+1} + (P_{i:k+1} \cdot G_{k:j})$$

(3) After processing:

The sum bits are calculated in this stage. Logic equation is:

$$S_i = P_i \oplus C_{i-1}$$
$$C_{i-1} = (P_i \cdot C_{in}) + G_i$$

3.5.2 Circuit

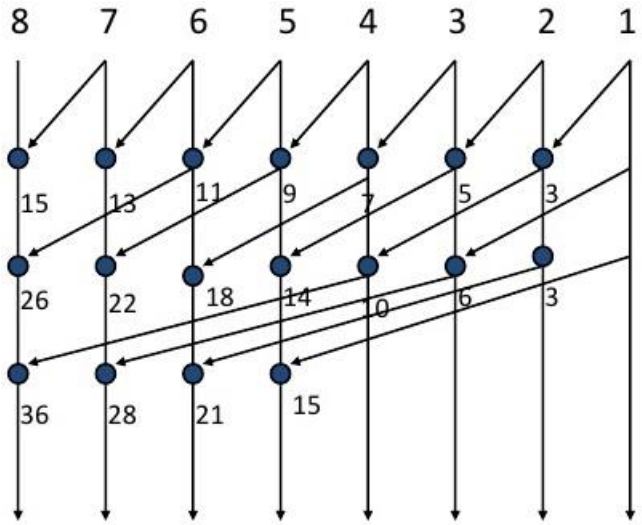


Figure (7): Block diagram of 8 bit Kogge stone adder [7]

3.6 Hybrid Adder

Hybrid adder is a mixture of previous two adders- Kogge Stone Adder, and Carry Lookahead Adder, aiming at reduced area than Kogge stone adder, with the disadvantage of increase in delay.

3.6.1 Algorithm

For a hybrid adder of 32 bits, the carry of first 16 bits (less significant) is generated using carry lookahead adder, and the carry of last 16 bits (more significant) is obtained using Kogge stone adder. It is seen in the performance report that the area gets significantly reduced from that of Kogge stone adder.

3.6.2 Circuit

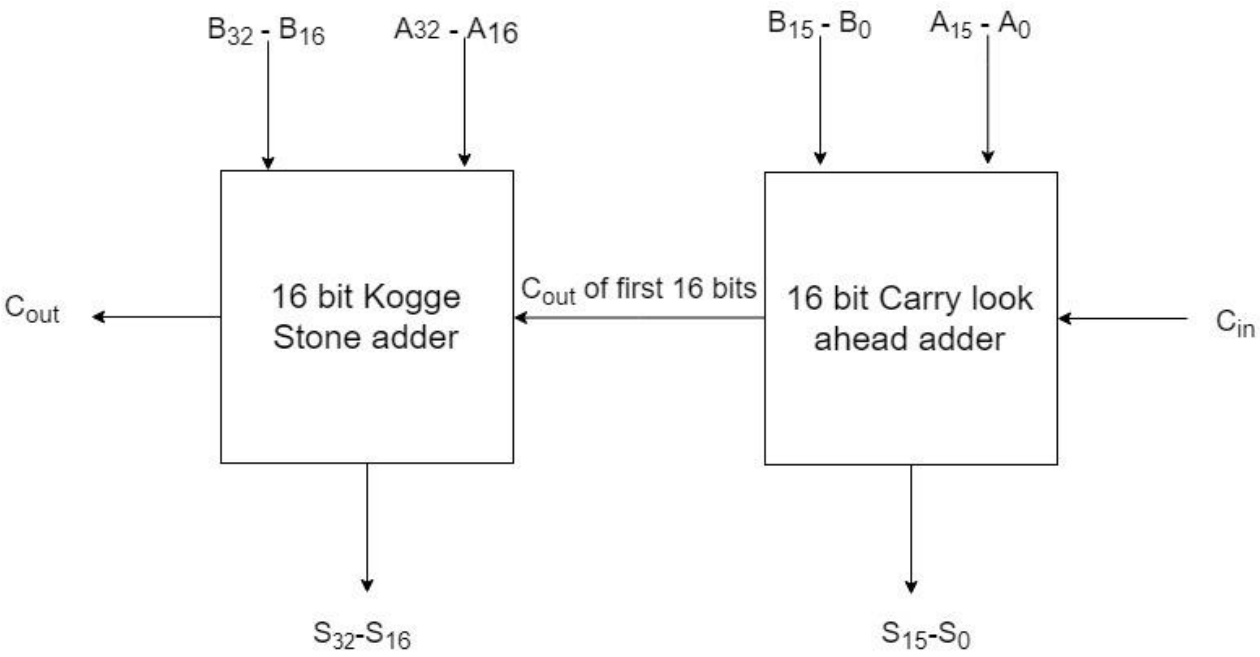


Figure (8): Block diagram of 32-bit hybrid adder

4. Simulation Result

Simulation and synthesis are done using automotive Spartan 6 family devices with speed grade of -3.

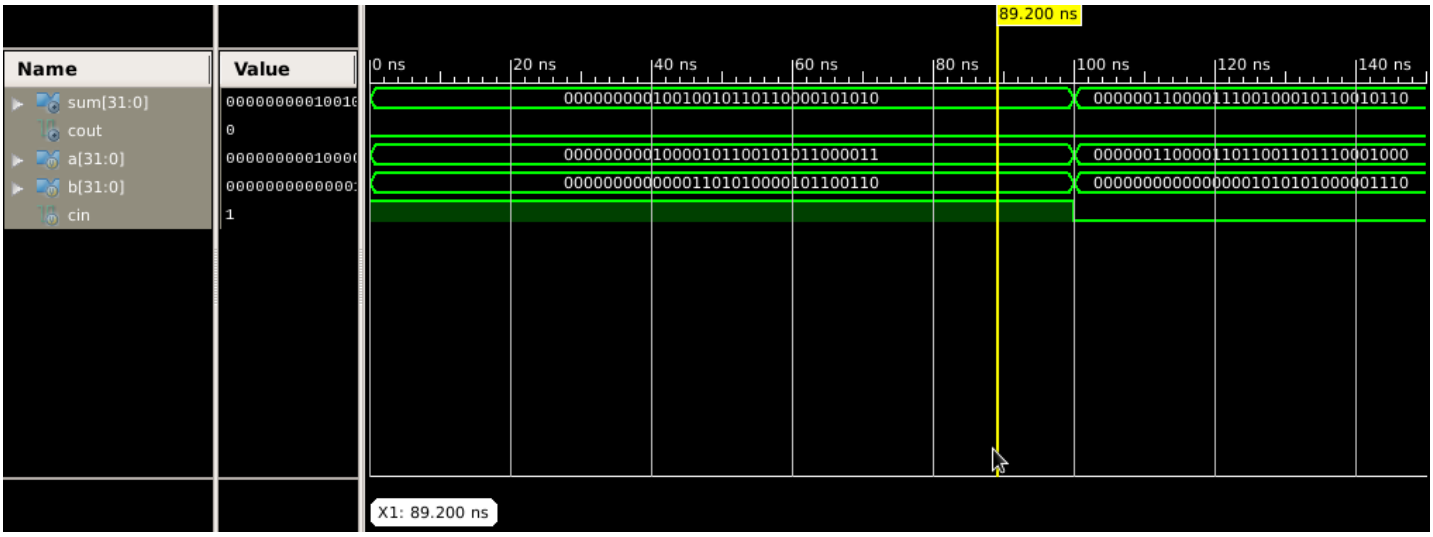


Figure (9): Simulation result of 32-bit Ripple carry adder

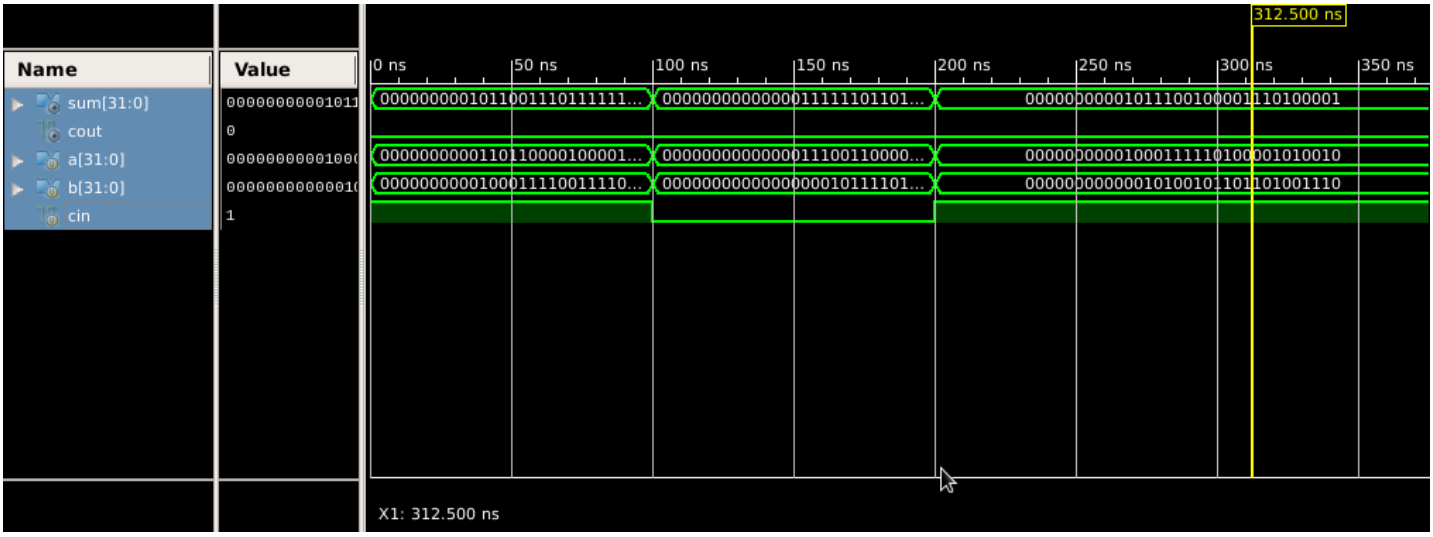


Figure (10): Simulation result of 32-bit Carry Look ahead Adder

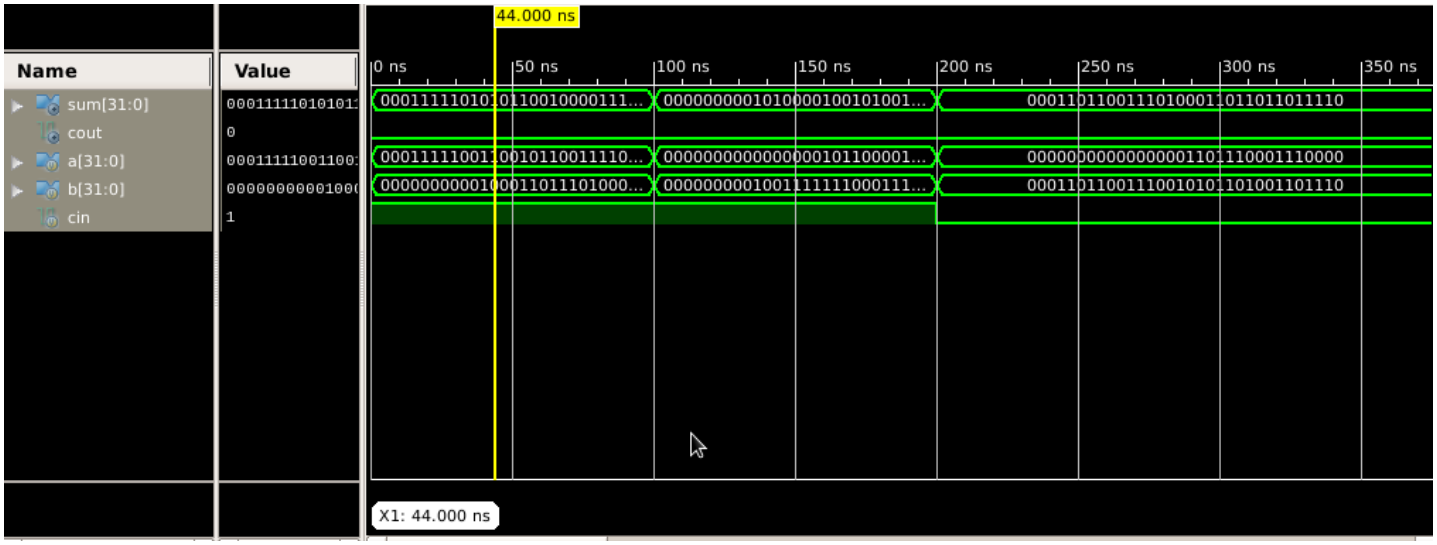


Figure (11): Simulation result of 32-bit Carry select adder

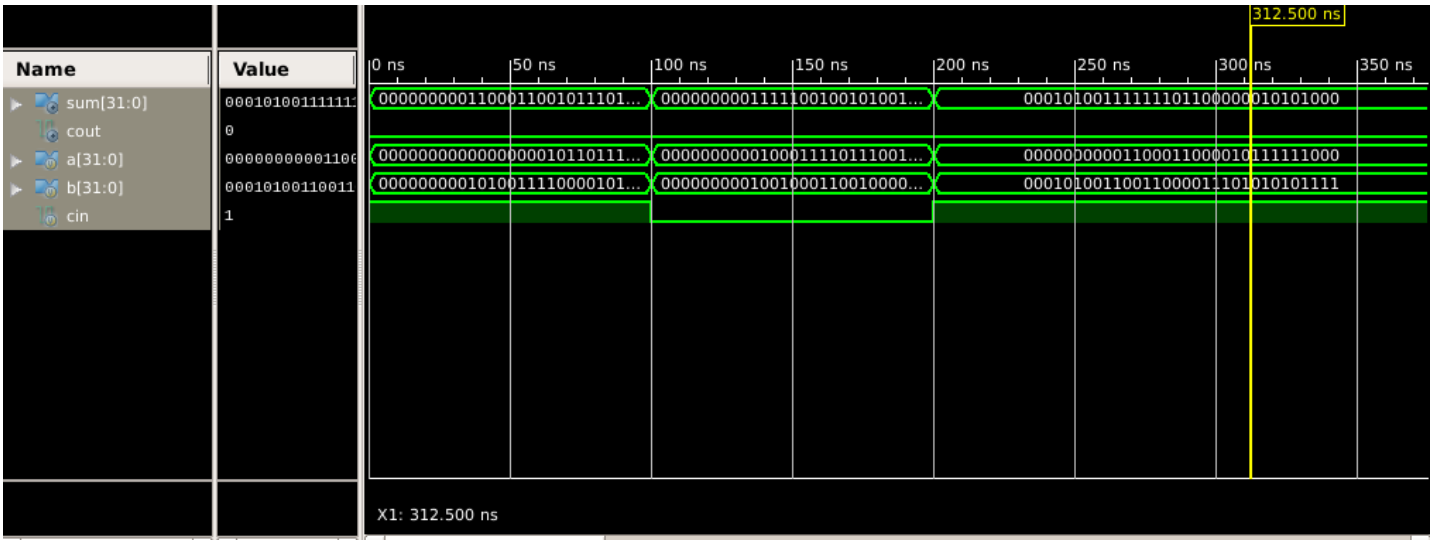


Figure (12): Simulation result of 32-bit carry skip adder

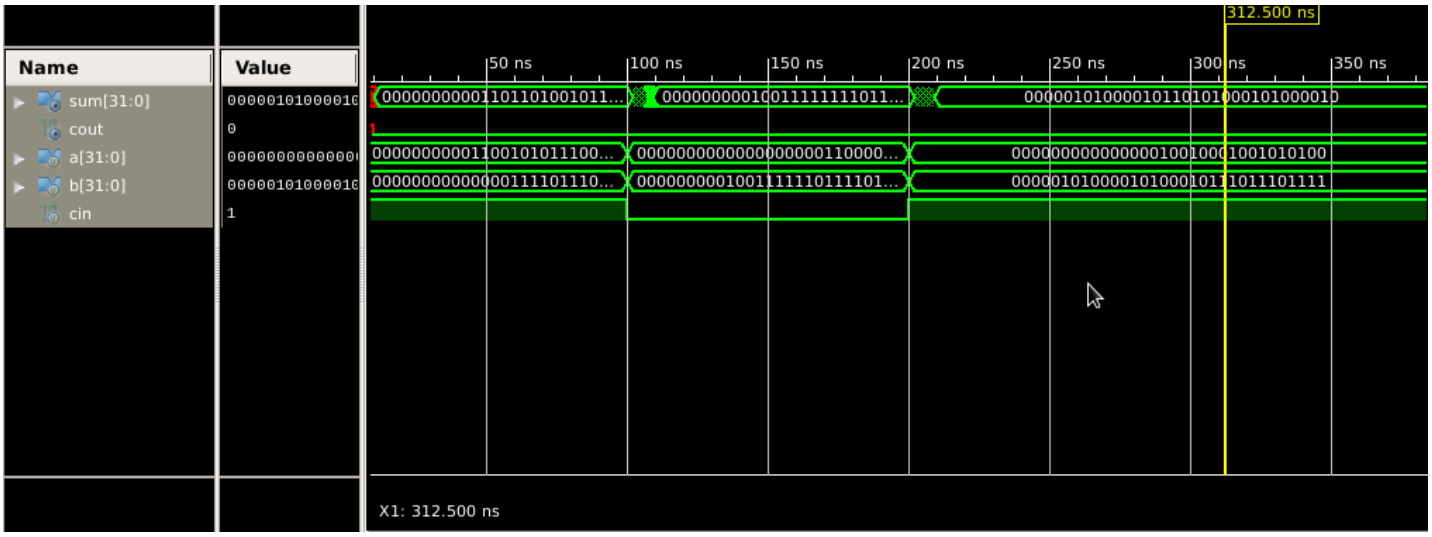


Figure (13): Simulation result of 32-bit Kogge-Stone adder

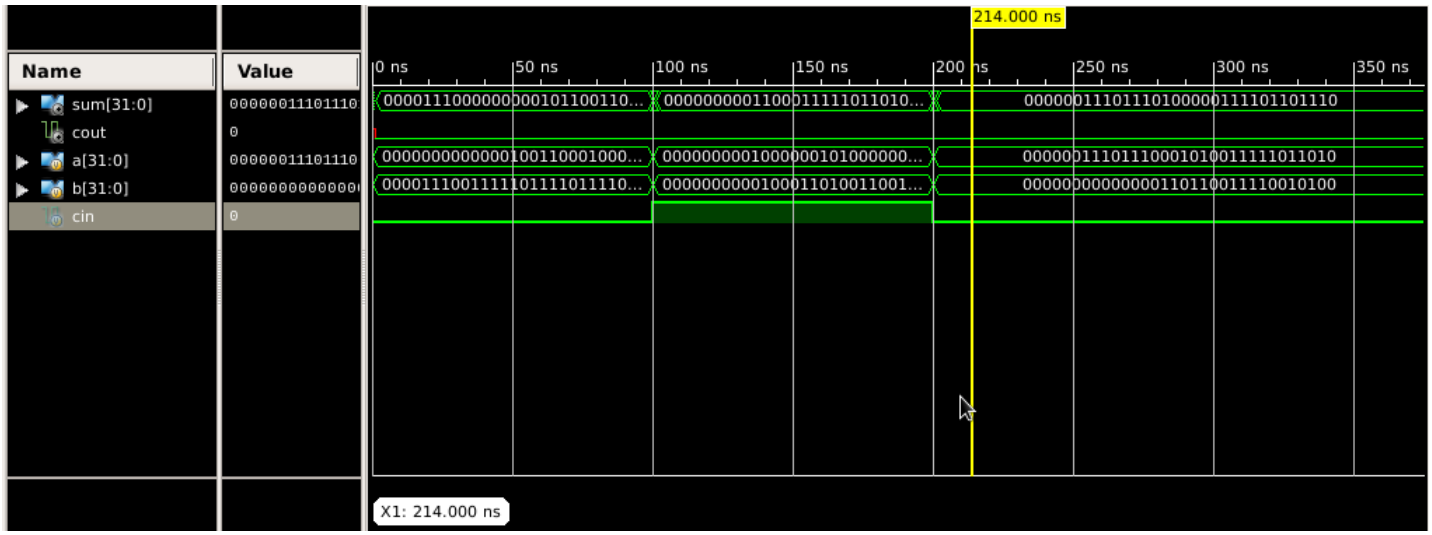


Figure (14): Simulation result of 32-bit hybrid adder

5. Performance Comparison and Analysis

Name of Adder	Delay(ns)	Power(mW)	LUTs
Ripple Carry adder	23.328	23.314	48
Carry Lookahead adder	20.803	23.289	49
Carry select adder	18.219	23.527	54
Carry Skip adder	18.438	23.731	66
Kogge Stone adder	13.054	24.131	144
Hybrid adder	15.907	23.598	78

Table (1): Comparative analysis of all six adders

6. Conclusion

The above-mentioned algorithms were implemented with satisfactory results in most cases. From the comparative analysis of the adders in the above segment, it is observed that among all the adders, ripple carry adder shows the maximum delay, and Kogge stone adder has the minimum delay while the Kogge stone adder has the maximum area. Total power of all the adders is almost the same because the power in any combinational circuit mostly depends on the frequency which is the same for all.

References

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