To all our customers

Regarding the change of names mentioned in the document, such as Hitachi Electric and Hitachi XX, to Renesas Technology Corp.

The semiconductor operations of Mitsubishi Electric and Hitachi were transferred to Renesas Technology Corporation on April 1st 2003.
These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.)

Accordingly, although Hitachi, Hitachi, Ltd., Hitachi Semiconductors, and other Hitachi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp.

Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

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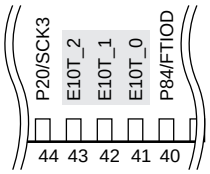
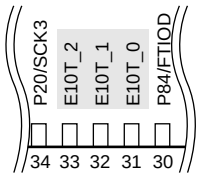
Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

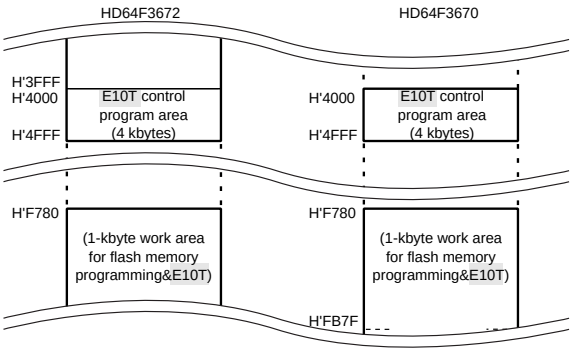
HITACHI SEMICONDUCTOR TECHNICAL UPDATE

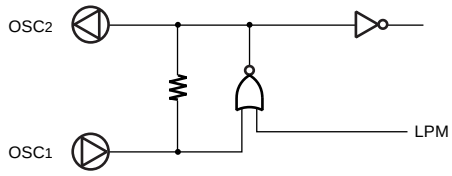
Classification of Production	Microcomputer			No	TN-H8*-233A/E	Rev	1.0
THEME	Amendments, Deletions, and Additions to H8/3672 Series Hardware Manual when Issuing the Second Edition		Classification of Information	1. Spec change (2) Supplement of Documents 3. Limitation of Use 4. Change of Mask 5. Change of Production Line			
PRODUCT NAME	H8/3672 Series Hardware Manual	Lot No. All Lots	Reference Documents	H8/3672 Series Hardware Manual ADE-602-239A Rev.2.0		Effective Date From Now	

We would like to inform you about the amendments to be made and the descriptions to be deleted and added to the first edition of the H8/3672 Series (H8/3672 and H8/3670) Hardware Manual when issuing the second edition.

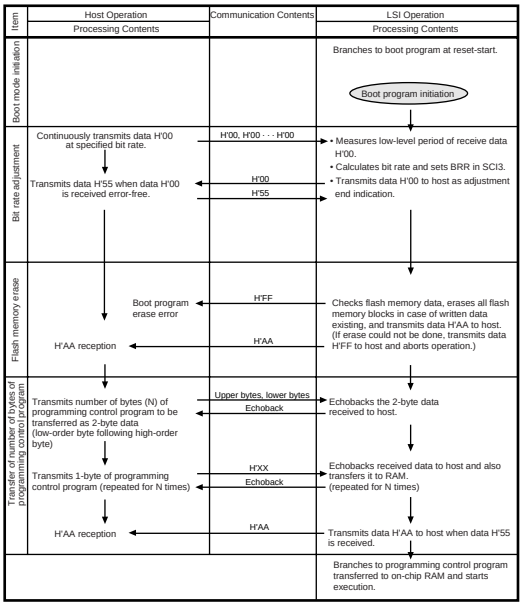
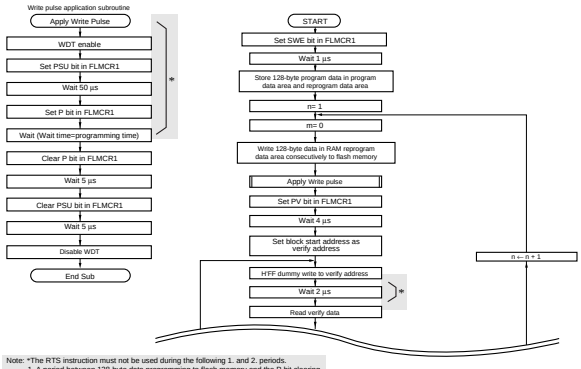
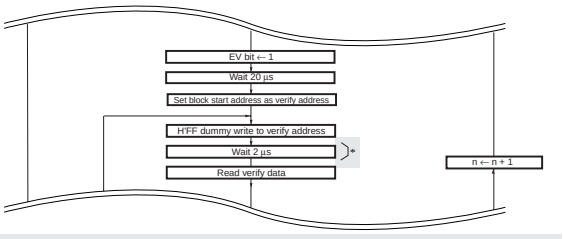
Main Revisions and Additions in this Edition

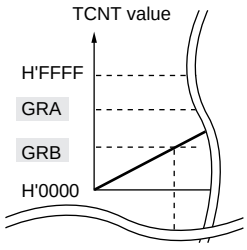
Item	Page	Revisions (See Manual for Details)
General Precautions on Handling of Product	iii	Added.
Configuration of This Manual	iv	Added.
Preface	v	Notes added. Restrictions 1 to 5 when using an on-chip emulator (E10T) for H8/3672 program development and debugging
1.1 Features Compact package	1	Package added. LQFP-48 (FP-48B)
1.2 Internal Block Diagram Figure 1.1 Internal Block Diagram	2	↔ E10T_0 ↔ E10T_1 ↔ E10T_2
1.3 Pin Arrangement Figure 1.2 Pin Arrangement (FP-64E)	3	 Note: Do not connect NC pins (these pins are not connecte to the internal circuitry).
1.3 Pin Arrangement Figure 1.3 Pin Arrangement (FP-48F, FP-48B)	4	 Note: Do not connect NC pins (these pins are not connecte to the internal circuitry).

Item	Page	Revisions (See Manual for Details)
1.4 Pin Functions Table 1.1 Pin Functions	6	Syrial communication interface (SCI): TXD 46 36 Output; RXD 45 35 Input; SCK3 44 34 I/O
1.4 Pin Functions Table 1.1 Pin Functions	6	E10T: E10T_0, E10T_1, E10T_2; 41, 42, 43; 31, 32, 33; Interface pin for E10T emulator
2.1 Address Space and Memory Map Figure 2.1 Memory Map	8	
4.1.1 Address Break Control Register (ABRKCR)	56	Bit 4: ACMP2; Bit 3: ACMP1; Bit 2: ACMP0 Address Compare Condition Select 2 to 0 These bits comparison condition between the address set in BAR and the internal address bus. 000: Compares 16-bit addresses 001: Compares upper 12-bit addresses 010: Compares upper 8-bit addresses 011: Compares upper 4-bit addresses 1XX: Reserved (setting prohibited)
4.2 Operation	58	Description amended. When the ABIF and ABIE bits in ABRKSR are set to 1, the address break function generates an interrupt request to the CPU. The ABIF bit in ABRKSR is set to 1 by the combination of the address set in BAR, the data set in BDR, and the conditions set in ABRKCR.
4.2 Operation Figure 4.2 Address Break Interrupt Operation Example (3)	59	Deleted.
4.3 Usage Notes	59	Added.

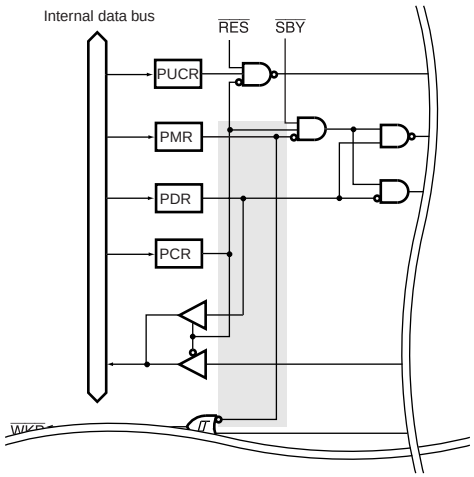
<table>
<tr><th>Item</th><th>Page</th><th>Revisions (See Manual for Details)</th></tr>
<tr><td>5.1 System Clock Generator
Figure 5.2 Block Diagram of System Clock Generator</td><td>61</td><td>Added.
 

LPM: Low-power mode (standby mode, subsleep mode)</td></tr>
<tr><td>5.2.1 Prescaler S</td><td>63</td><td>Description amended.
In active mode and sleep mode, the clock input to prescaler S is determined by the division factor designated by MA2 to MA0 in SYSCR2.</td></tr>
<tr><td>6.1.1 System Control Register 1 (SYSCR1)</td><td>66</td><td>
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>6</td><td>STS2</td><td rowspan="4">Standby Timer Select 2 to 0
These bits designate the time the CPU and peripheral modules wait for stable clock operation after exiting from standby mode, to active mode or sleep mode due to an interrupt. The designation should be made according to the clock frequency so that the waiting time is at least 6.5 ms. The relationship between the specified value and the number of wait states is shown in table 6.1. When an external clock is to be used, the minimum value (STS2 = STS1 = STS0 =1) is recommended.</td></tr>
<tr><td>5</td><td>STS1</td></tr>
<tr><td>4</td><td>STS0</td></tr>
</table>
</td></tr>
<tr><td>6.1.4 Module Standby Control Register 2 (MSTCR2)</td><td>69</td><td>Deleted.</td></tr>
<tr><td>Section 7 ROM</td><td>75</td><td>Description amended.
EIOT → E10T
• Reprogramming capability
The flash memory can be reprogrammed up to 1,000 times.
Description deleted.
• Power-down mode</td></tr>
<tr><td>7.2.4 Flash Memory Enable Register (FENR)</td><td>79</td><td>Description amended.
Bit 7 (FLSHE) in FENR enables or disables the CPU access to the flash memory control registers, FLMCR1, FLMCR2, and EBR1.</td></tr>
<tr><td>7.3 On-Board Programming Modes
Table 7.1 Setting Programming Modes</td><td>79</td><td>Description amended.
EIOT_0 → E10T_0</td></tr>
</table>

Item	Page	Revisions (See Manual for Details)
7.3.1 Boot Mode Table 7.2 Boot Mode Operation	81	Changed. 
7.4.1 Program/Program-Verify	83	Description amended. 7. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower 2 bits are B'00. Verify data can be read in words or in longwords from the address to which a dummy write was performed.
7.4.1 Program/Program-Verify Figure 7.3 Program/Program-Verify Flowchart	84	
7.4.3 Interrupt Handling when Programming/Erasing Flash Memory Figure 7.4 Erase/Erase-Verify Flowchart	87	
9.5.1 Port Control Register 8 (PCR8)	106	**Bit** **Bi Name** **Initial** **R/W** **Description** 7 — — — Reserved 6 — — — 5 — — —

<table>
<tr><th>Item</th><th>Page</th><th>Revisions (See Manual for Details)</th></tr>
<tr><td>10.3.2 Time Constant Registers A and B (TCORA, TCORB)</td><td>113</td><td>Initial value added.
TCORA and TCORB are initialized to H'FF.</td></tr>
<tr><td>10.3.5 Timer Control Register V1 (TCRV1)</td><td>117</td><td>
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Description</th></tr>
<tr><td>2</td><td>TRGE</td><td>TCNTV starts counting up by the input of the edge which is selected by TVEG1 and TVEG0.
0: Disables starting counting-up TCNTV by the input of the TRGV pin and halting counting-up TCNTV when TCNTV is cleared by a compare match.
1: Enables starting counting-up TCNTV by the input of the TRGV pin and halting counting-up TCNTV when TCNTV is cleared by a compare match.</td></tr>
</table>
</td></tr>
<tr><td>11.3.2 Timer Control Register W (TCRW)</td><td>130</td><td>Description amended
TCRW selects the timer counter clock source, selects a clearing condition, and specifies the timer output levels.
<table>
<tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th><th>Description</th></tr>
<tr><td>3</td><td>TOD</td><td>0</td><td>R/W</td><td>Timer Output Level Setting D
0: Output value is 0*
1: Output value is 1*</td></tr>
<tr><td>2</td><td>TOC</td><td>0</td><td>R/W</td><td>Timer Output Level Setting C
0: Output value is 0*
1: Output value is 1*</td></tr>
<tr><td>1</td><td>TOB</td><td>0</td><td>R/W</td><td>Timer Output Level Setting B
0: Output value is 0*
1: Output value is 1*</td></tr>
<tr><td>0</td><td>TOA</td><td>0</td><td>R/W</td><td>Timer Output Level Setting A
0: Output value is 0*
1: Output value is 1*</td></tr>
</table>
Note: * The change of the setting is immediately reflected in the output value.</td></tr>
<tr><td>11.4.1 Normal Operation
Figure 11.6 Toggle Output Example (TOA = 0, TOB = 1)</td><td>137</td><td> 
</td></tr>
<tr><td>12.1 Features</td><td>151</td><td>Description amended.
• Selectable from nine counter input clocks.
Eight clock sources (ϕ/64, ϕ/128, ϕ/256, ϕ/512, ϕ/1024, ϕ/2048, ϕ/4096, and ϕ/8192) or the internal oscillator can be selected as the timer-counter clock. When the internal oscillator is selected, it can operate as the watchdog timer in any operating mode.</td></tr>
</table>

<table>
<tr><th>Item</th><th>Page</th><th>Revisions (See Manual for Details)</th></tr>
<tr><td>12.2.1 Timer Control/Status Register WD (TCSRWD)</td><td>152</td><td>TCSRWD performs the TCSRWD and TCWD write control. TCSRWD also controls the watchdog timer operation and indicates the operating state. TCSRWD must be rewritten by using the MOV instruction. The bit manipulation instruction cannot be used to change the setting value.

<table><tr><th>Bit</th><th>R/W</th></tr><tr><td>7</td><td>R/W</td></tr><tr><td>5</td><td>R/W</td></tr><tr><td>3</td><td>R/W</td></tr><tr><td>1</td><td>R/W</td></tr></table></td></tr>
<tr><td>13.3.4 Transmit Data Register (TDR)</td><td>158</td><td>Initial value added.
TDR is initialized to H'FF.</td></tr>
<tr><td>13.3.7 Serial Status Register (SSR)</td><td>163</td><td><table><tr><th>Bit</th><th>Bit Name</th><th>Initial Value</th><th>R/W</th></tr><tr><td>2</td><td>TEND</td><td>1</td><td>R</td></tr></table></td></tr>
<tr><td>15.1 When Using Internal Power Supply Step-Down Circuit</td><td>207</td><td>Description amended.
Connect the external power supply to the V_{CC} pin, and connect a capacitance of approximately 0.1 µF between V_{CL} and V_{SS}, as shown in figure 15.1.</td></tr>
<tr><td>15.2 When Not Using Internal Power Supply Step-Down Circuit</td><td>208</td><td>Description amended.
When the internal power supply step-down circuit is not used, connect the external power supply to the V_{CL} pin and V_{CC} pin, as shown in figure 15.2.</td></tr>
<tr><td>17.2.6 Flash Memory Characteristics (Preliminary)
Table 17.7 Flash Memory Characteristics (Preliminary)</td><td>231</td><td><table><tr><th rowspan="2">Item</th><th rowspan="2">Symbol</th><th rowspan="2">Test Condition</th><th colspan="3">Values</th><th rowspan="2">Unit</th></tr><tr><th>Min</th><th>Typ</th><th>Max</th></tr><tr><td>Reprogramming count</td><td>N_{WEC}</td><td>—</td><td>—</td><td>—</td><td>1000</td><td>Times</td></tr></table></td></tr>
<tr><td>B.1 I/O Port Block
Figure B.10 Port 5 Block Diagram (P54 to P50)</td><td>267</td><td> 
</td></tr>
</table>