

3V3 Generation

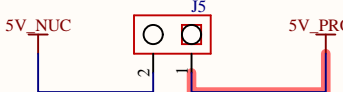
5V Input Choice Jumper

3V3 Choice Jumper

PCB Note:
Routing must be carefully done following P.11 of the datasheet

Design Note:
Use CL = 20uF or more when VIN-VOUT (T) <1.5V. Otherwise : CL = 10uF

5V Nucleo jumper



The diagram shows a 5V_NUC pin connected to a 5V_PROT pin via a jumper. The jumper is represented by a red line. A blue line connects the 5V_NUC pin to a 5V_PROT pin. A yellow box labeled J5 is shown with two pins. A red line connects the 5V_PROT pin to the J5 pin. A blue line connects the 5V_NUC pin to the J5 pin. A yellow box labeled J6 is shown with two pins. A red line connects the 5V_PROT pin to the J6 pin. A blue line connects the 5V_NUC pin to the J6 pin.

J5

5V_NUC

5V_PROT

J6

SNT-100-BK-T-H

[illegible]

Sheet Name				POWER			
Project Title				HiveSight			
Global Project				PMC			
Size		Group				Revision	
11x17		SwarmUS				1.000	
Date			2020-07-13		Sheet		
					1 of 10		
Filename					Designers		
HIVE_SIGHT_POWER.SchDoc					Philippe Arsenault Hubert Dube Louis-Daniel Gaulin		

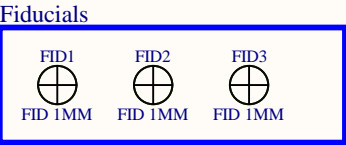
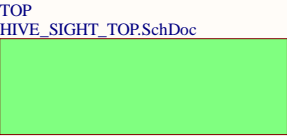
HiveSight

PMC

SwarmUS

Revision 1.000

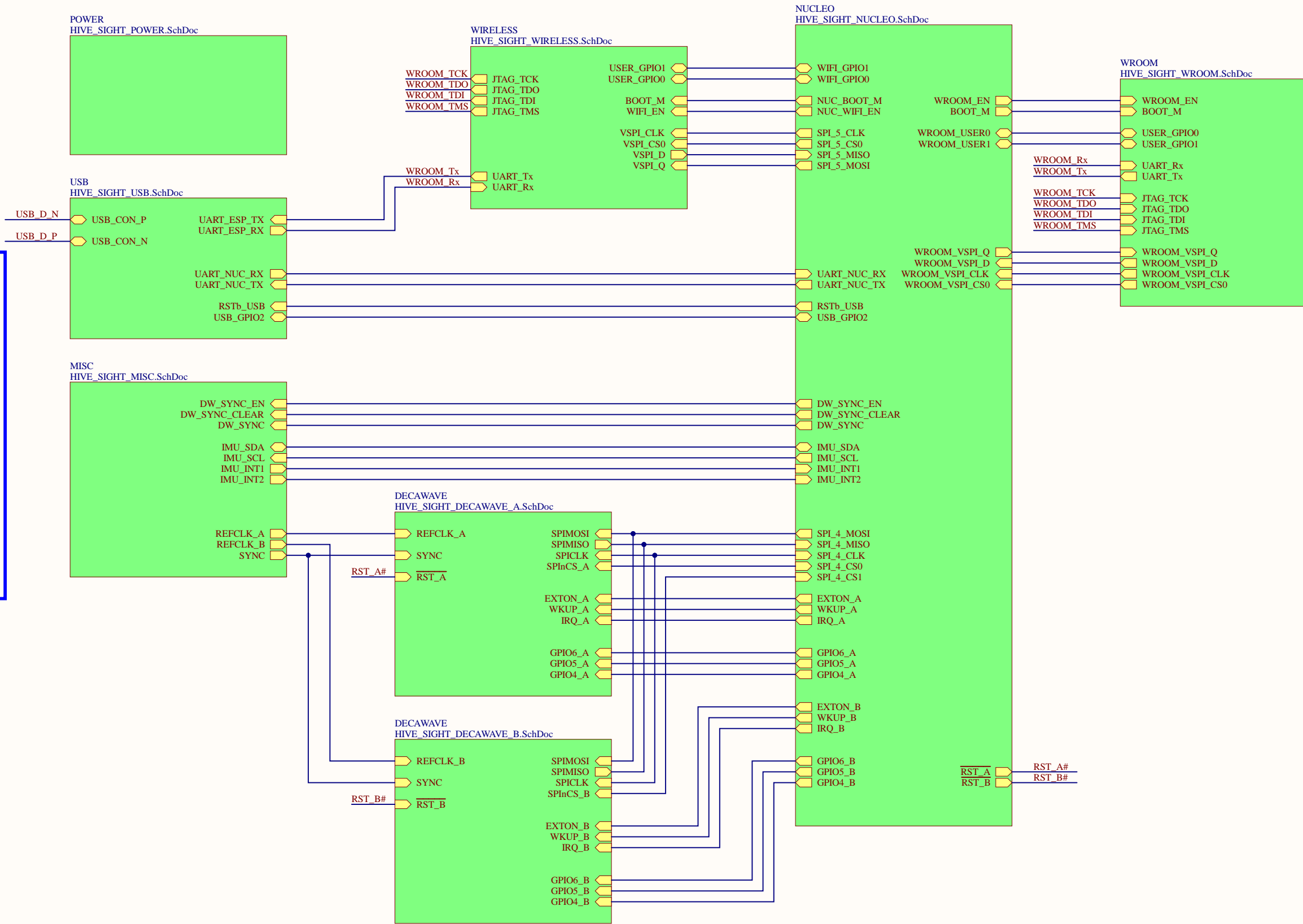
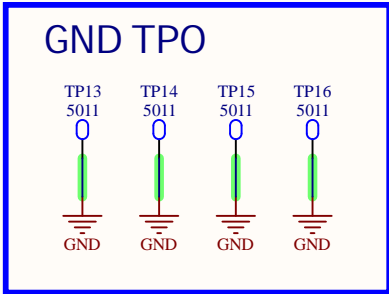
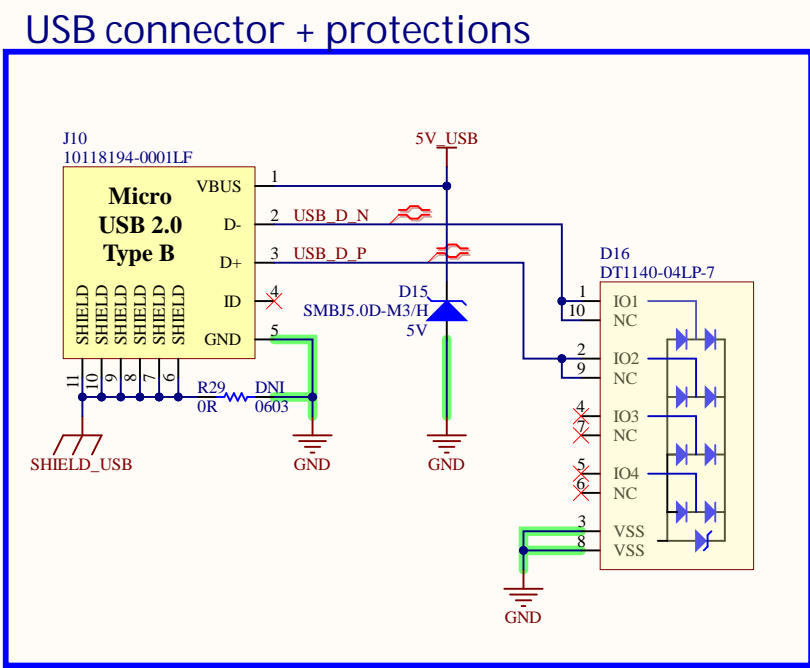
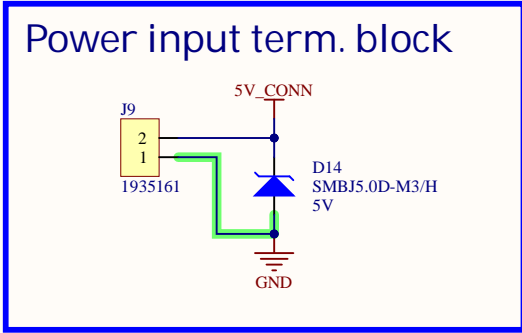
Date : 2020-07-13



Revision history	

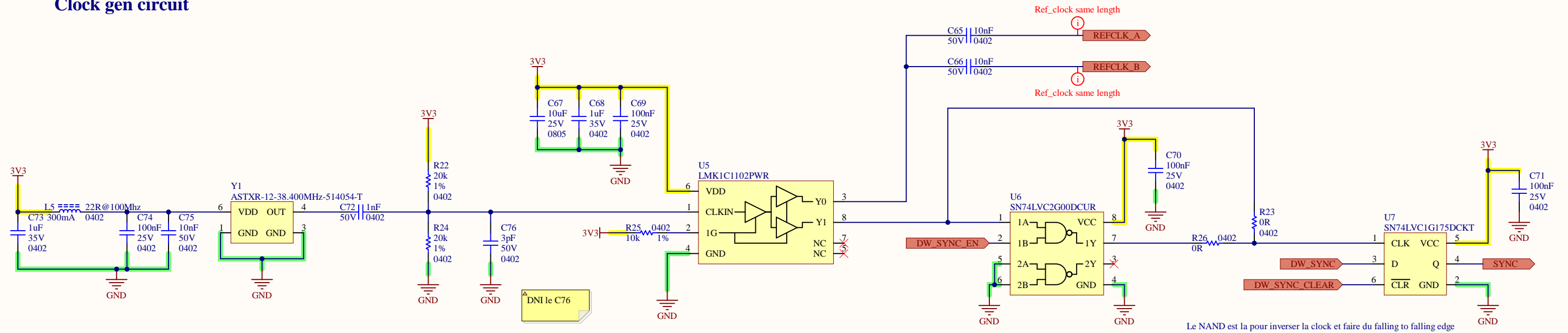
Package size conversion	
<i>Metric</i>	<i>Imperial</i>
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

Project Title		HiveSight	
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Size	11x17	Group	SwarmUS
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Filename		Designers	
HIVE_SIGHT_TITLE.SchDoc		Philippe Arsenault Hubert Dube Louis-Daniel Gaulin	

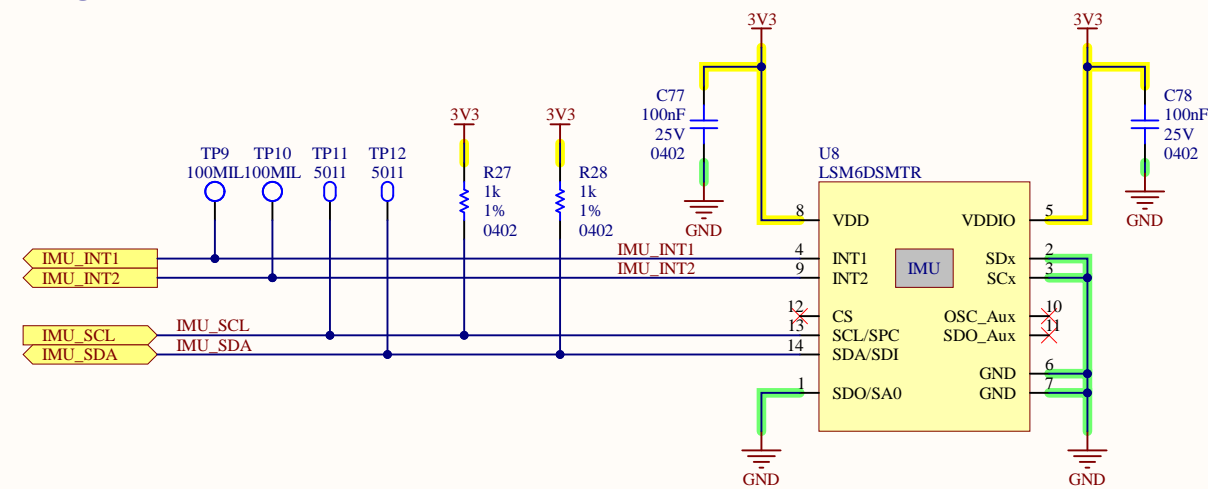


Sheet Name			Top		
Project Title			HiveSight		
Global Project			PMC		
Size	11x17	Group	SwarmUS	Revision	1.000
Date	2020-07-13			Sheet	3 of 10
Filename	HIVE_SIGHT_TOP.SchDoc			Designers	Philippe Arsenault Hubert Dube Louis-Daniel Gaulin

Clock gen circuit

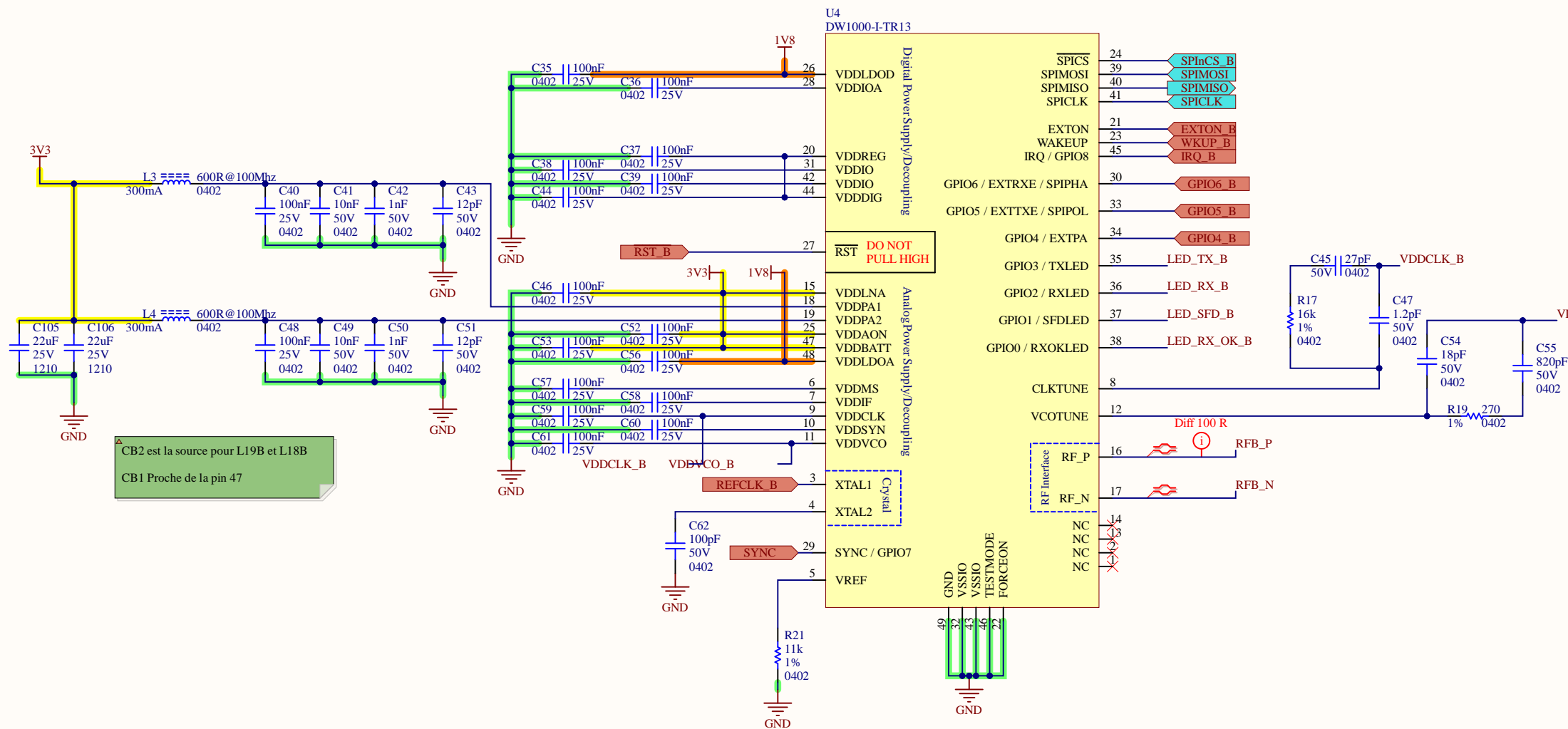


IMU

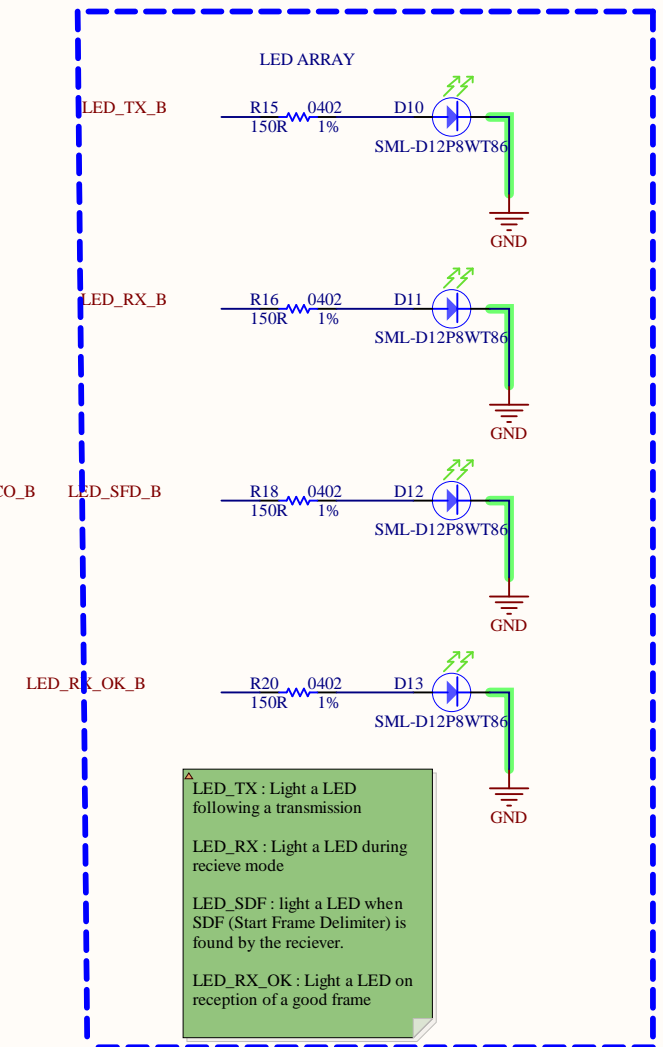


Sheet Name			DECAWAVE		
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Global Project			PMC		
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11x17	SwarmUS		1.000		
Date	2020-07-13		Sheet	4	of 10
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HIVE_SIGHT_MISC.SchDoc			Philippe Arsenault Hubert Dube Louis-Daniel Gaulin		

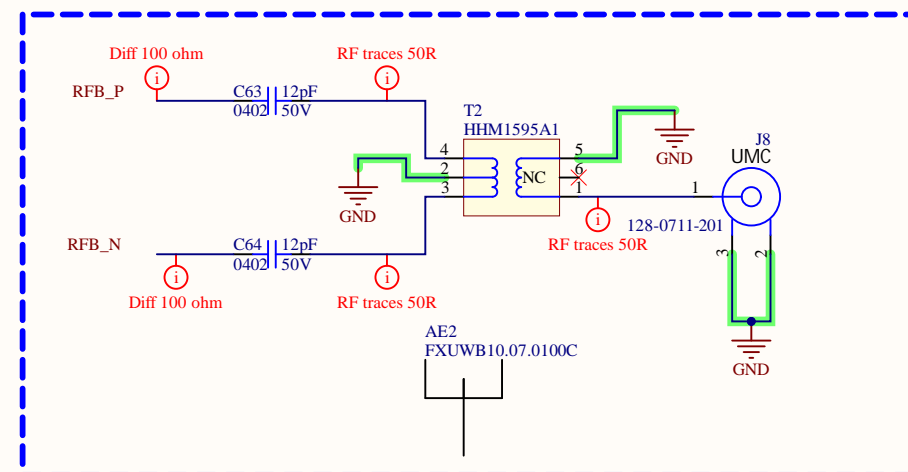
Decawave B



DEBUG LED

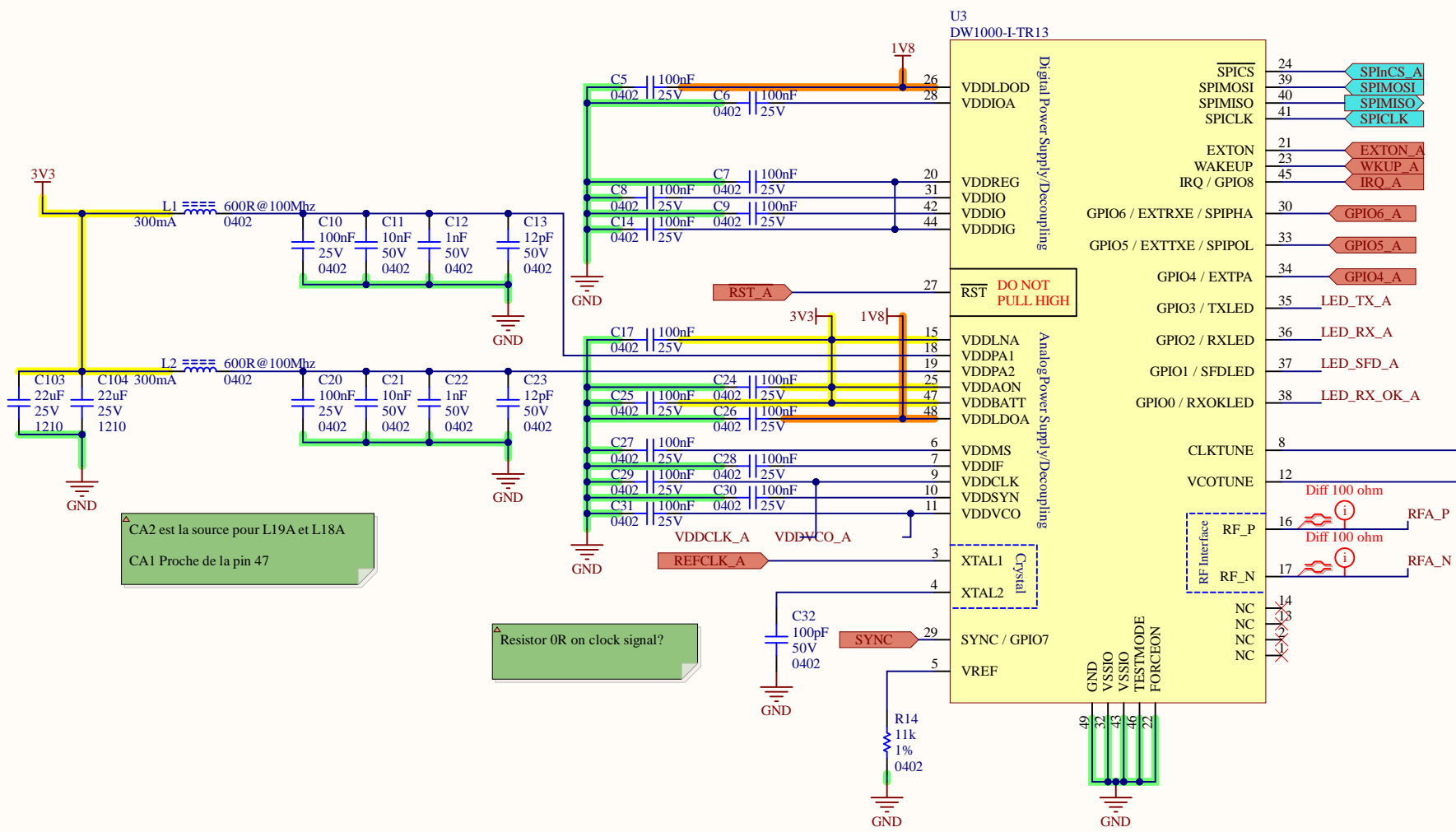


RF Circuit

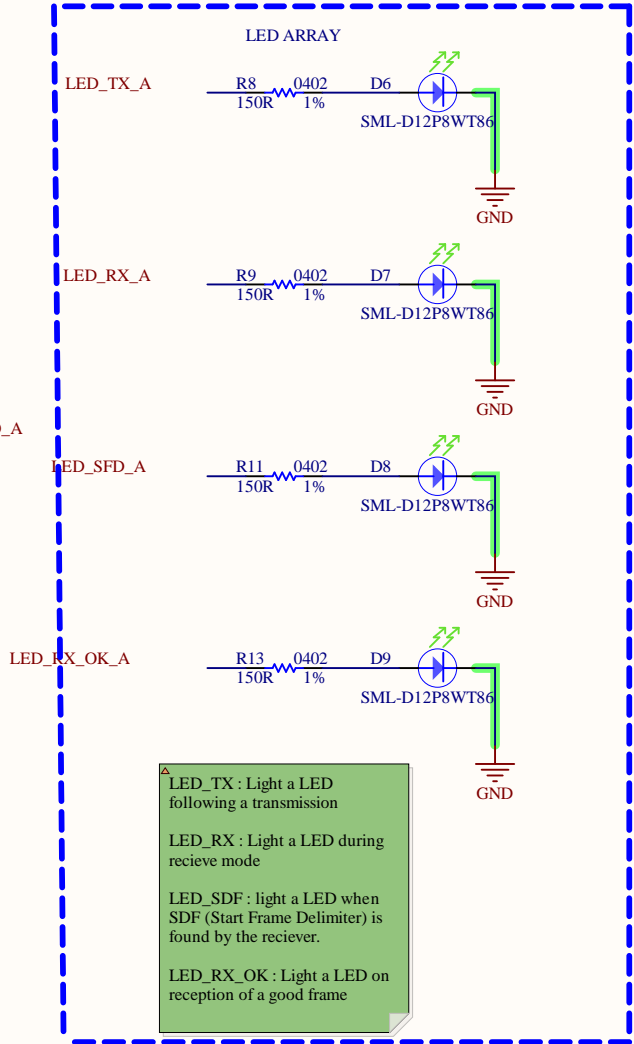


Sheet Name			DECAWAVE		
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11x17	SwarmUS			1.000	
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HIVE_SIGHT_DECAWAVE_B.SchDoc				Philippe Arsenault Hubert Dube Louis-Daniel Gaulin	

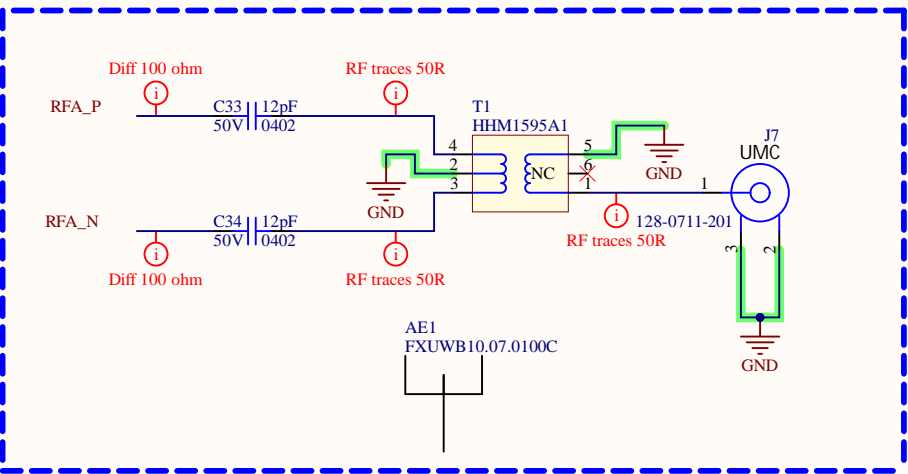
Decawave A



DEBUG LED



RF Circuit



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Filename			Designers		
HIVE_SIGHT_DECAWAVE_A.SchDoc			Philippe Arsenault Hubert Dube Louis-Daniel Gaulin		

Header JTAG

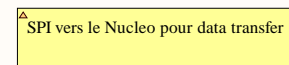
The schematic diagram illustrates the SPI flash memory circuit. The top section shows the connection of the MX25L323FM1I-08Q (U10) to the 3V3 supply and ground. The bottom section shows the connection of the M20-7810445 (J12) to the SPI signals.

U10: MX25L323FM1I-08Q

Pin	Signal
8	VCC
4	GND
5	SI/SIO0
2	SO/SIO1
3	WP/SIO1
7	HD/SIO2
6	HD/SIO3
SCLK	SCLK
CS	CS

J12: M20-7810445

Pin	Signal
1	SPI_CS0
2	SPI_Q
3	SPI_WP
4	SPI_HD
5	GND
6	SPI_CLK
7	SPI_CLK
8	SPI_D



BANK SUPPLIES

The image displays five schematic diagrams for bank supplies in a 3V3 SDIO interface. The first diagram shows a 3V3 SDIO pin connected to a 3V3 supply line, with a 1µF 35V capacitor (C93) and a 100nF 25V capacitor (C94) connected to ground. A 1% resistor (R36, 6R2) is connected between the 3V3 SDIO pin and the 3V3 supply line. The second diagram shows a 3V3 supply line connected to a 3V3 pin, with a 100nF 25V capacitor (C88) connected to ground. The third diagram shows a 3V3 supply line connected to a 3V3 pin, with a 100pF 50V capacitor (C89) and a 1µF 35V capacitor (C90) connected to ground. The fourth diagram shows a 3V3 supply line connected to a 3V3 pin, with a 100nF 25V capacitor (C91) connected to ground. The fifth diagram shows a 3V3 supply line connected to a 3V3 pin, with a 100nF 25V capacitor (C91) connected to ground.

As they are bank supplies, the caps must be placed the closest possible to their pin, with the smallest values closer to the pin

[illegible]

JTAG SELECT

The diagram illustrates the JTAG SELECT circuit. It consists of four signal lines, each connected to a resistor and a pull-down resistor to ground. The signals are labeled JTAG_TMS, JTAG_TCK, JTAG_TDO, and JTAG_TDI.

- JTAG_TMS_SW** is connected to **R55** and **0R** (0402). The signal is labeled **JTAG_TMS**.
- JTAG_TCK_SW** is connected to **R57** and **0R** (0402). The signal is labeled **JTAG_TCK**.
- JTAG_TDO_SW** is connected to **R59** and **0R** (0402). The signal is labeled **JTAG_TDO**.
- JTAG_TDI_SW** is connected to **R61** and **0R** (0402). The signal is labeled **JTAG_TDI**.

32K_X_P
32K_X_N

R33 1%
6R2 0402

X1 32kHz

CM7V-T1A-32KHZ

C85 13pF
50V 0402

C86 13pF
50V 0402

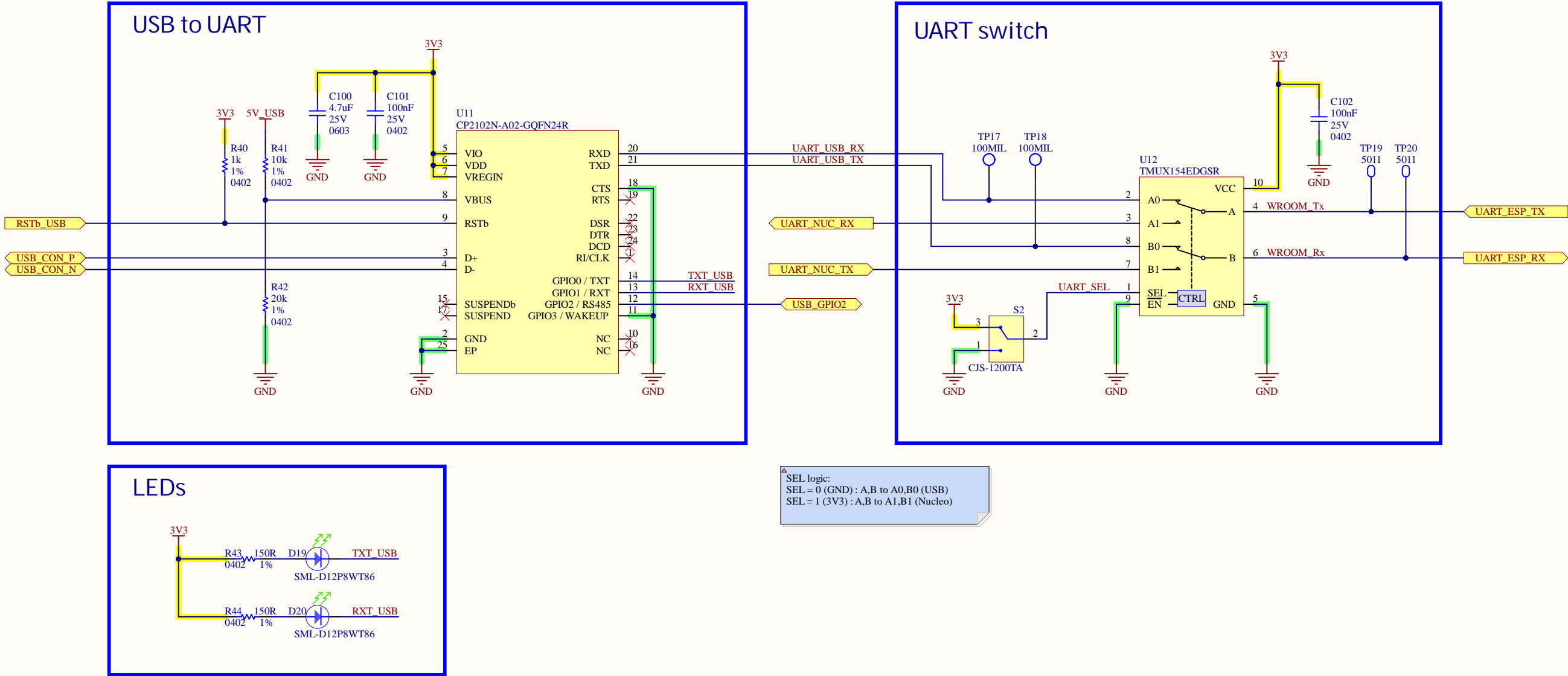
GND GND

NOT ACTUAL VALUE: TBD

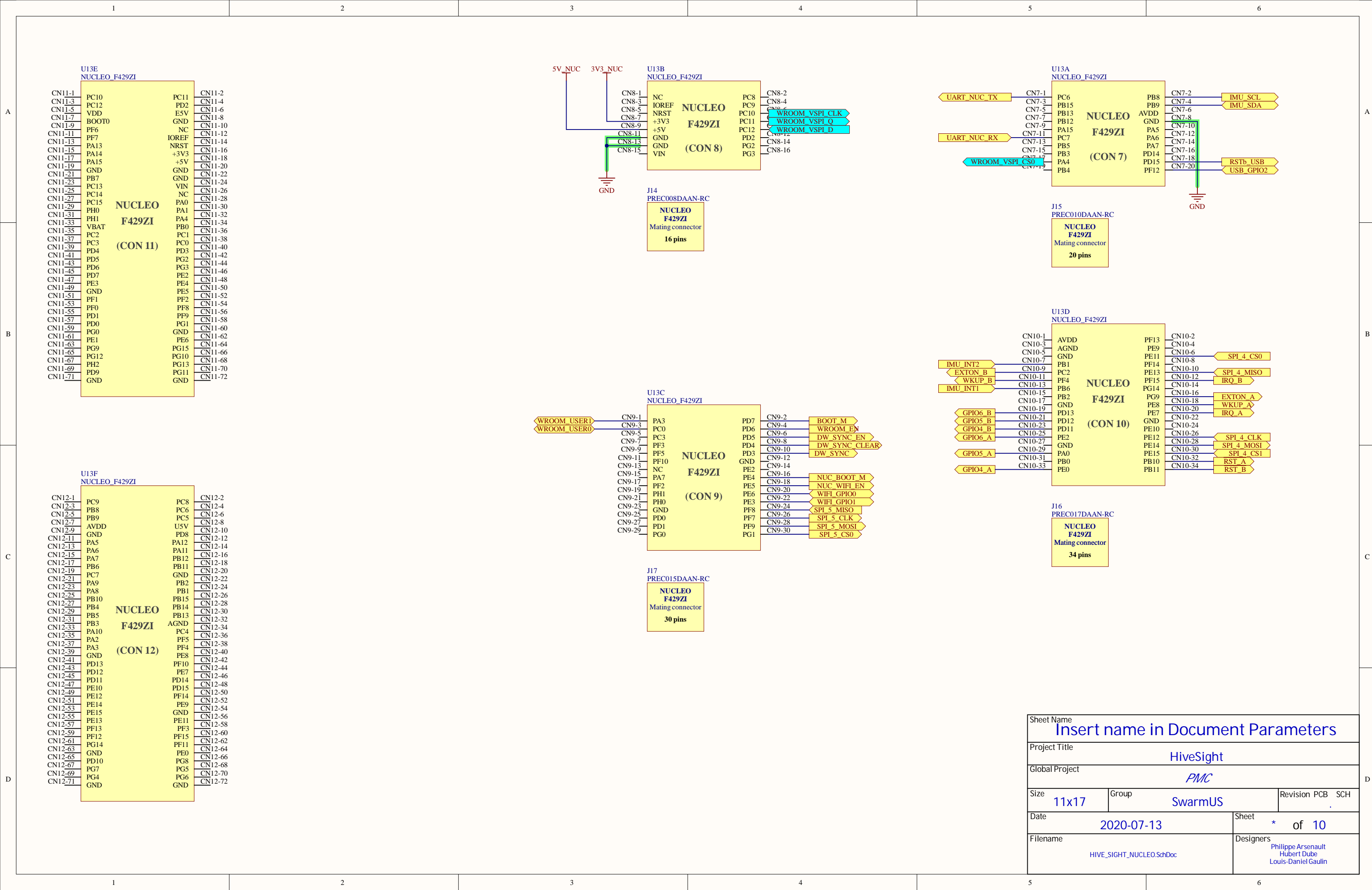
Put closest possible to the chip

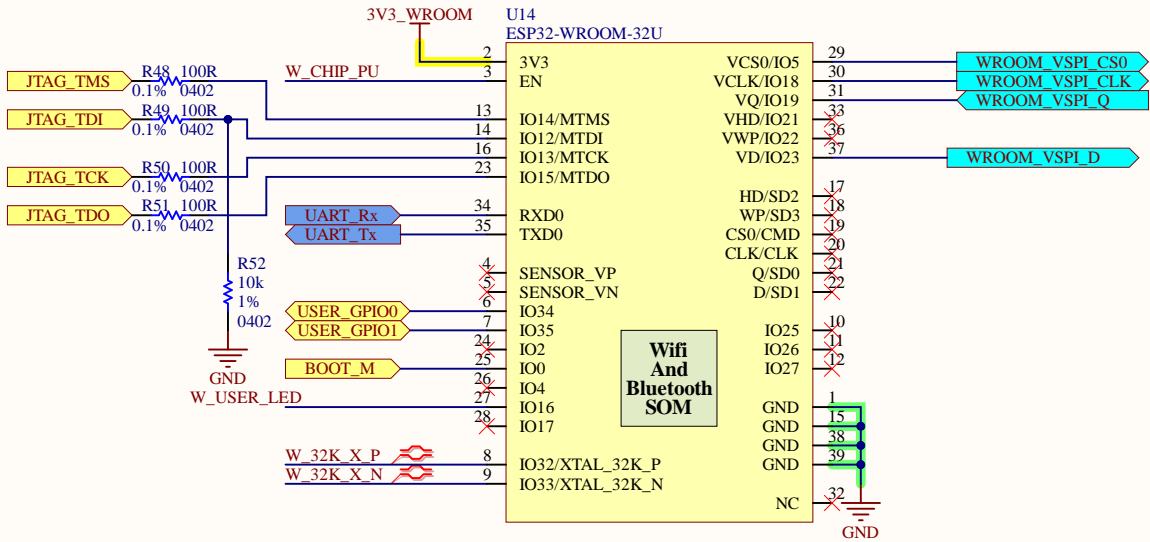
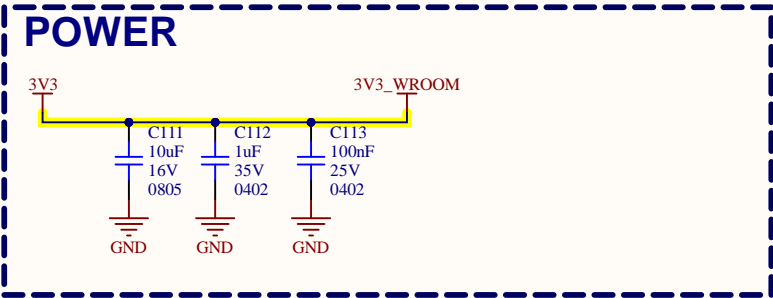
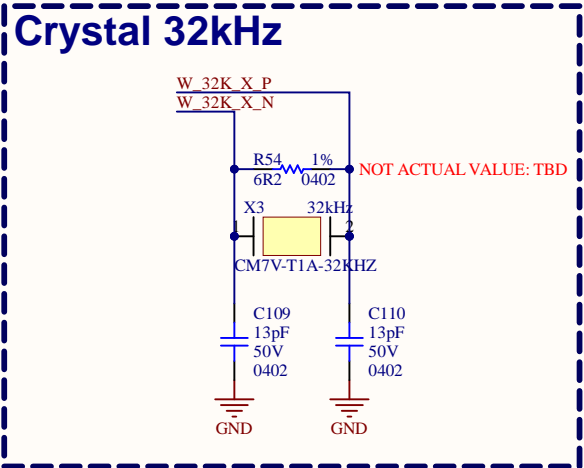
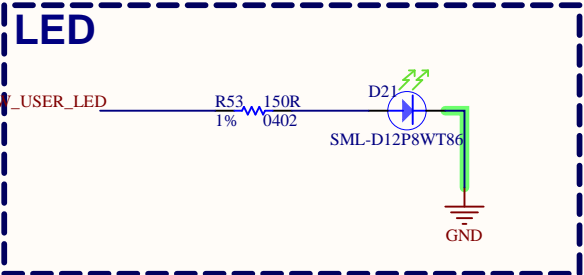
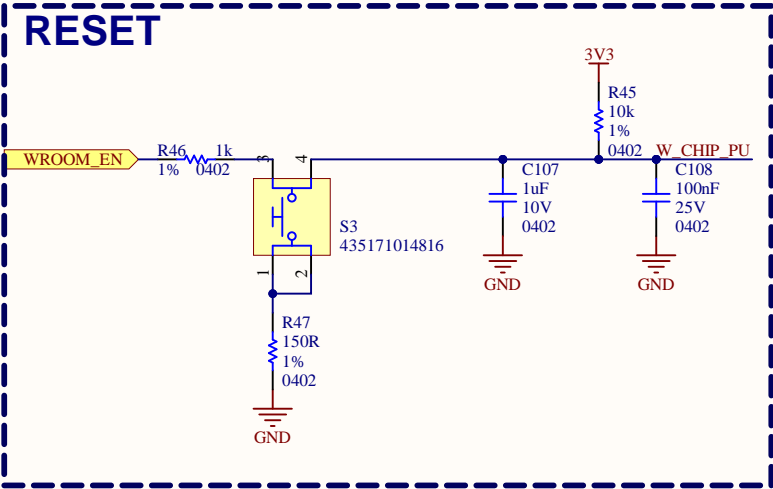
The diagram illustrates the placement of two capacitors, C95 and C92, relative to the FA-20H oscillator chip (X2). The chip is labeled with '40MHz' and 'FA-20H 40.0000MF10Z K3'. Pin 1 is connected to XTAL_P, and pin 2 is connected to GND. Pin 3 is connected to the output of the oscillator, and pin 4 is connected to GND. Capacitor C95 (80pF, 50V, 0402) is placed between XTAL_P and GND. Capacitor C92 (8pF, 50V, 0402) is placed between the output of the oscillator and GND. The text 'Put closest possible to the chip' is shown in a blue box, indicating the recommended placement for these components.

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Project Title		HiveSight	
Global Project		PMC	
Size 11x17	Group SwarmUS	Revision 1.000	
Date 2020-07-13	Sheet 5	of 10	
Filename HIVE_SIGHT_WIRELESS.SchDoc		Designers Philippe Arsenault Hubert Dube Louis-Daniel Gaulin	



Sheet Name		USB	
Project Title		HiveSight	
Global Project		PMC	
Size	Group	Revision	
11x17	SwarmUS	1.000	
Date	2020-07-13	Sheet	6 of 10
Filename		Designers	
HIVE_SIGHT_USB.SchDoc		Philippe Arsenault Hubert Dube Louis-Daniel Gaulin	





Sheet Name		WROOM	
Project Title		HiveSight	
Global Project		PMC	
Size	Group	Revision	
11x17	SwarmUS	1.000	
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Filename		Designers	
HIVE_SIGHT_WROOM.SchDoc		Philippe Arsenault Hubert Dube Louis-Daniel Gaulin	