

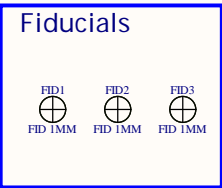
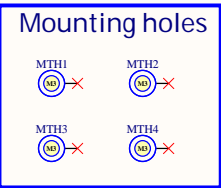
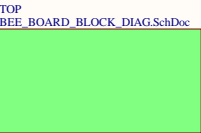
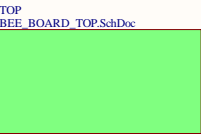
# BeeBoard

## PMC

SwarmUS

Revision 1.000

Date: 2021-03-18



Revision history	

Section name

power

Power notes

Questions / TODO

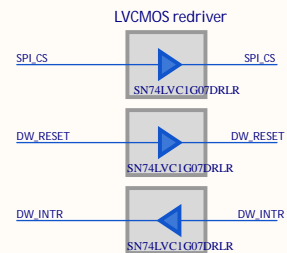
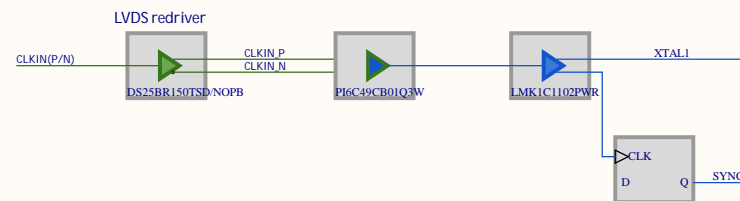
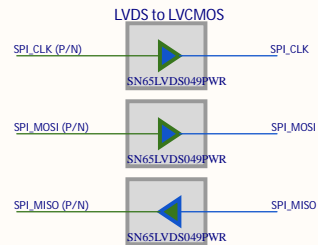
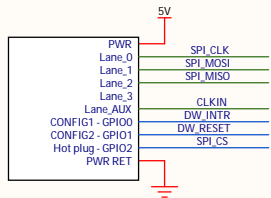
Package size conversion	
Metric	Imperial
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

Usage notes

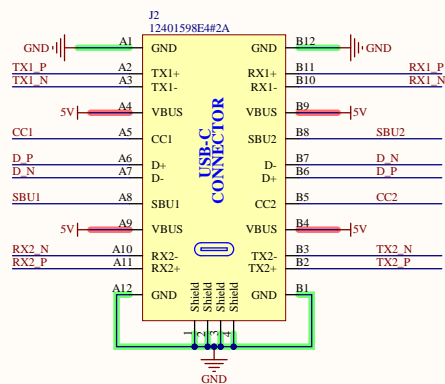
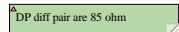
Routing notes



Project Title			BeeBoard		
Global Project			PMC		
Size	11x17	Group	SwarmUS	Revision	1.000
Date	2021-03-18			Sheet	1 of 6
Filename	BEE_BOARD_TITLE.SchDoc			Designers	Philippe Arsenaull Hubert Dube Louis-Daniel Gaulin

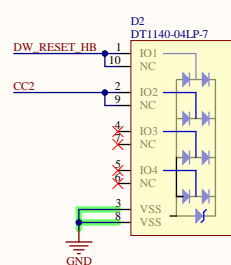
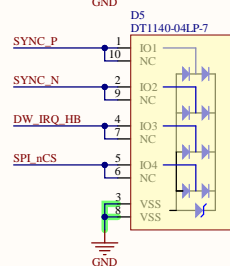
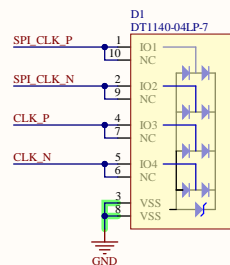
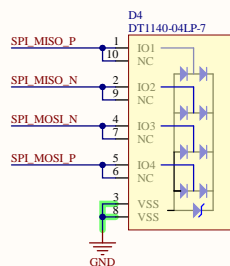
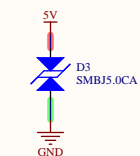
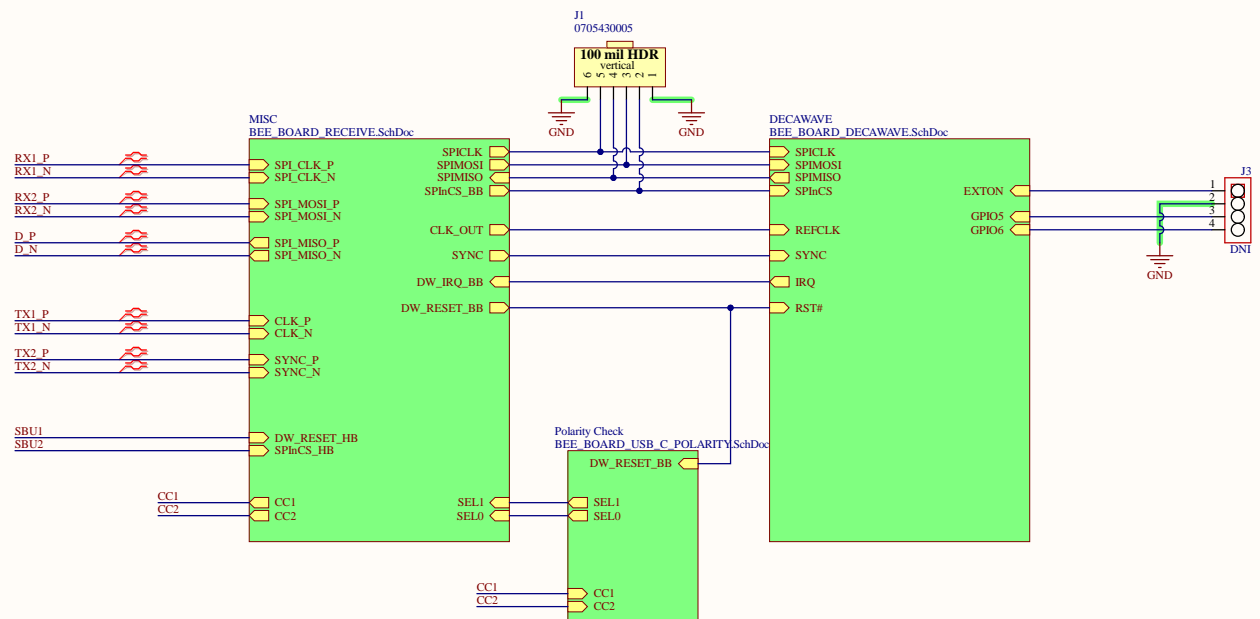


Sheet Name			
Insert name in Document Parameters			
Project Title		BeeBoard	
Global Project		PMC	
Size	Group	Revision	
11x17	SwarmUS	1.000	
Date	2021-03-18	Sheet	2 of 6
Filename		Designers	
BEE_BOARD_BLOCK_DIAG.SchDoc		Philippe Arsenault Hubert Dube Louis-Daniel Gaulin	



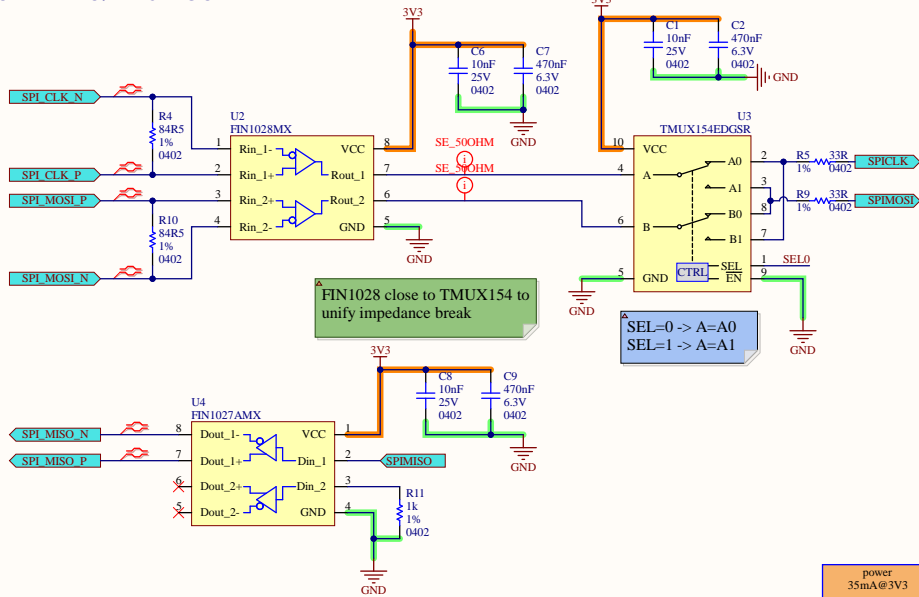
On flat cable (no twisting) :

- RX1 : SPI\_CLK
- RX2 : SPI\_MOSI
- TX1 : CLK\_38.4MHz
- TX2 : SYNC
- D+/D- : MISO
- SBU1 : DW\_RESET
- SBU2 : SPI\_nCS
- CC1 : outputs IRQ
- CC2 : NC

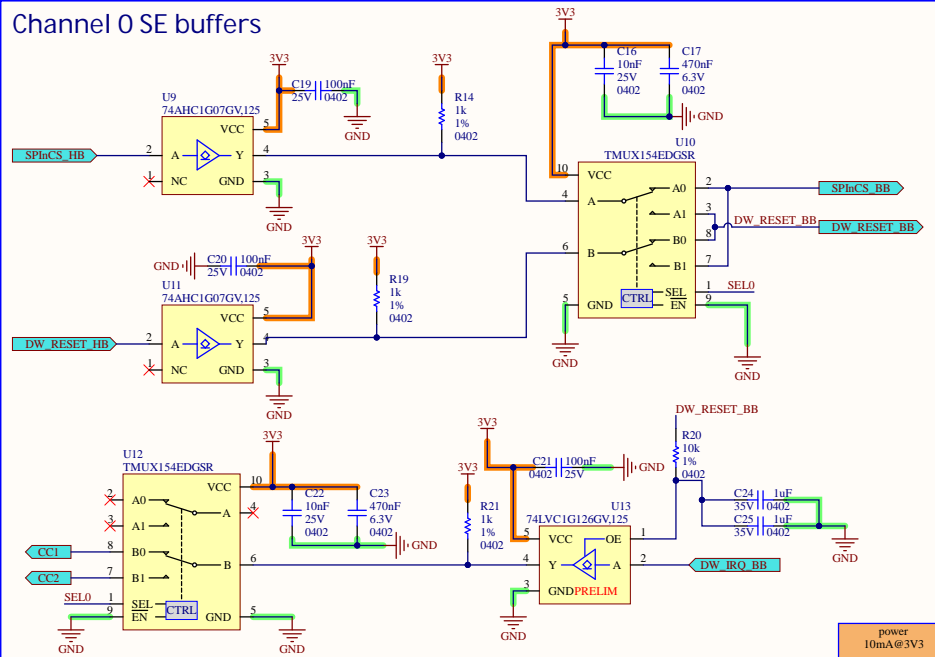


Sheet Name			Top		
Project Title			BeeBoard		
Global Project			PMC		
Size	11x17	Group	SwarmUS		Revision
					1.000
Date	2021-03-18		Sheet	3 of 6	
Filename	BEE_BOARD_TOP SchDoc		Designers	Philippe Arsenault Hubert Dube Louis-Daniel Gauvin	

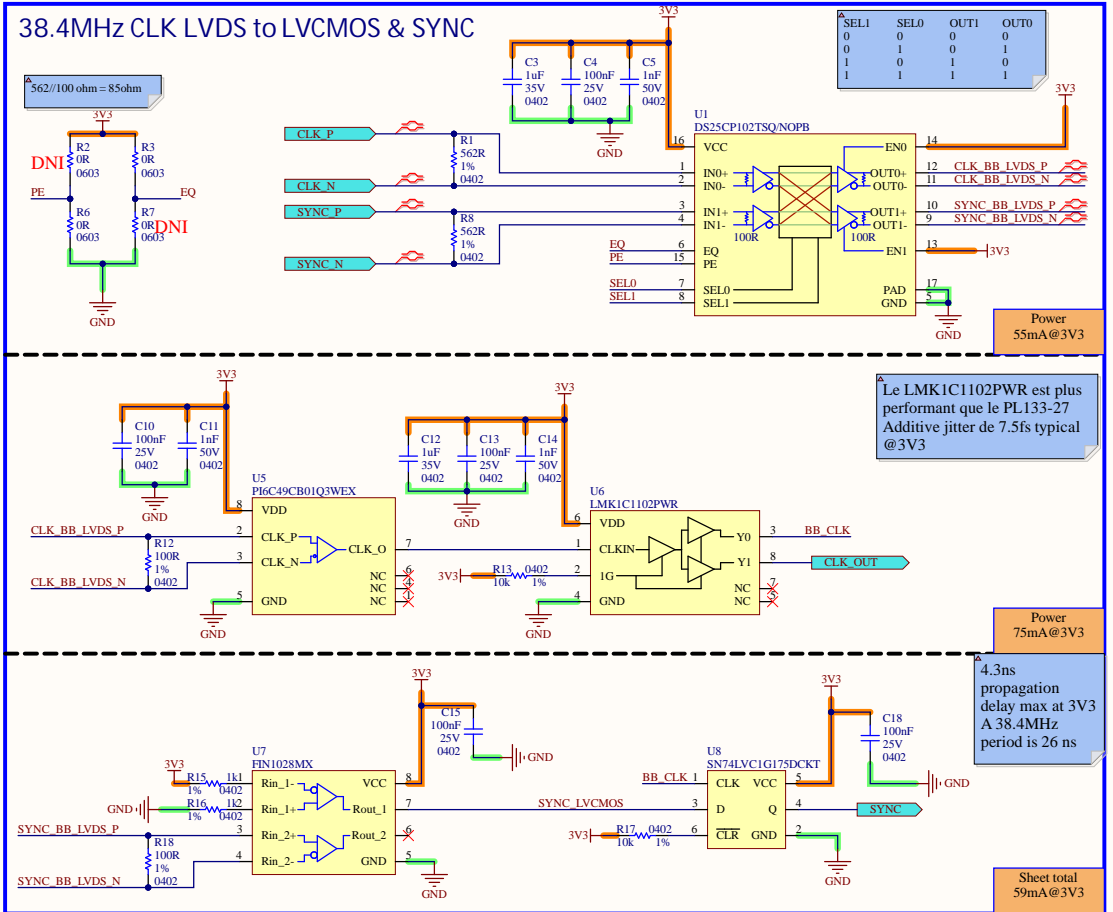
## SPI LVDS/LVCMOS



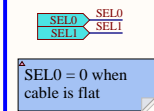
## Channel 0 SE buffers



## 38.4MHz CLK LVDS to LVCMOS & SYNC



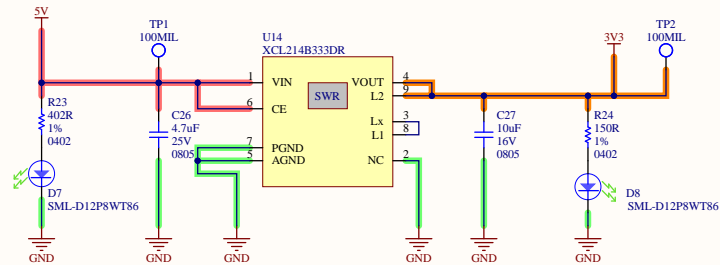
## Pol. SEL



RC = 0.02  
VIH is 2V  
OE = 2V after DW\_RESET = 3V3  
for 18ms

Sheet Name		Receive modules	
Project Title		BeeBoard	
Global Project		PMC	
Size	Group	SwarmUS	Revision
11x17			1.000
Date	2021-03-18	Sheet	4 of 6
Filename		Designers	
BEE_BOARD_RECEIVE.SchDoc		Philippe Arsenault Hubert Dube Louis-Daniel Gaulin	

### 3V3 Generation



395mA@5V  
MAX

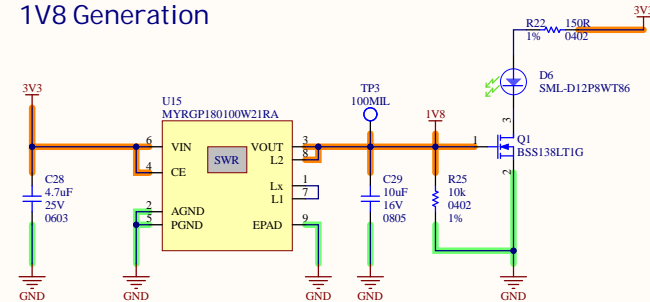
EFFICENCY = 90%+ @250mA

512mA@3V3  
MAX

Design Note:  
Use CL = 20uF or more  
when VIN-VOUT (T) <1.5V.  
Otherwise : CL = 10uF

PCB Note:  
Routing must be  
carefully done following  
P.11 of the datasheet

### 1V8 Generation



138mA@3V3  
MAX

EFFICENCY = 90%+ @180mA

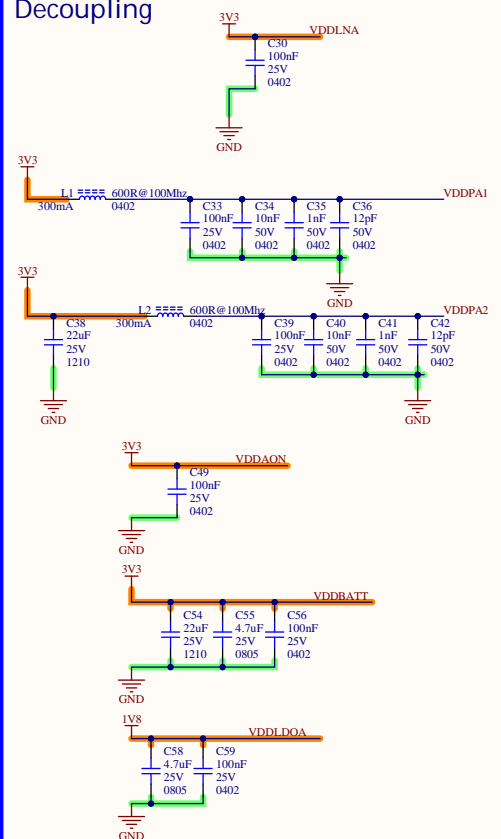
228mA@1V8  
MAX

PCB Note:  
Routing must be  
carefully done following  
P.12 of the datasheet

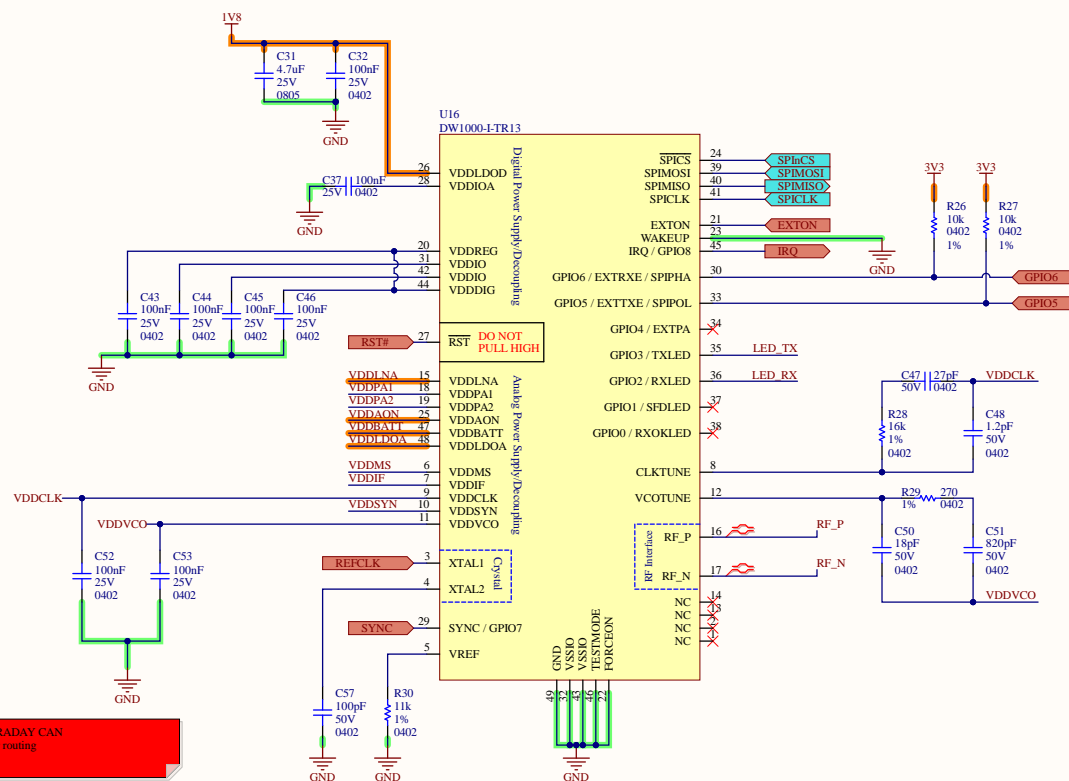
Close to DW

Sheet Name		POWER	
Project Title		BeeBoard	
Global Project		PMC	
Size	Group	Revision	
11x17	SwarmUS	1.000	
Date	2021-03-18	Sheet	5 of 6
Filename		Designers	
BEE_BOARD_POWER.SchDoc		Philippe Arsenault Hubert Dube Louis-Daniel Gaulin	

## Decoupling

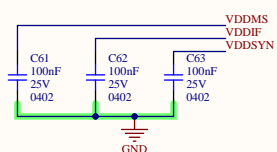


## Decawave

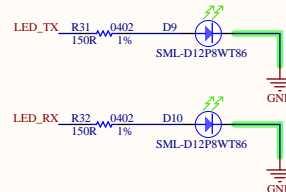


power  
30mA@3V3  
210mA@1V8

## Off-chip capacitance

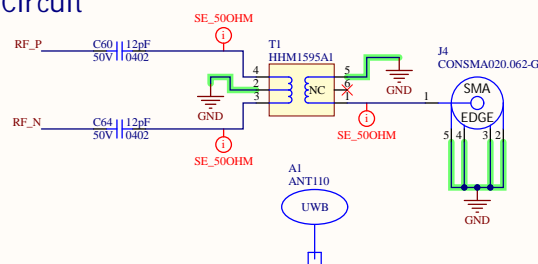


## Debug LED



power  
40mA@3V3

## RF Circuit



Sheet Name		DECAWAVE	
Project Title		BeeBoard	
Global Project		PMC	
Size	Group	Revision	
11x17	SwarmUS	1.000	
Date	Sheet		
2021-03-18	6 of 6		
Filename		Designers	
BEE_BOARD_DECAWAVE.SchDoc		Philippe Arseneault Hubert Dube Louis-Daniel Gaulin	

Sheet total  
70mA@3V3  
210mA@1V8

**USB-C Entry**

The circuit diagram shows a USB-C entry interface. It features a rail-to-rail op-amp (U17, LM339LVRT) configured as a 4-input XOR gate. The op-amp's non-inverting input (IN1) is connected to a 5V supply through a 100K resistor (R33) and a 1% resistor (0402). The inverting input (IN2) is connected to a 5V supply through a 100K resistor (R40) and a 1% resistor (0402). The op-amp's output (OUT1) is connected to a 5V supply through a 100K resistor (R33) and a 1% resistor (0402). The op-amp's output (OUT2) is connected to a 5V supply through a 100K resistor (R40) and a 1% resistor (0402). The op-amp's output (OUT3) is connected to a 5V supply through a 100K resistor (R33) and a 1% resistor (0402). The op-amp's output (OUT4) is connected to a 5V supply through a 100K resistor (R40) and a 1% resistor (0402).

The 74VHC1G386GW (U18) is configured as a 4-input XOR gate. Its inputs A, B, C, and D are connected to the outputs of the op-amp. The output Y is connected to a 5V supply through a 100K resistor (R33) and a 1% resistor (0402). The output Y is also connected to a 5V supply through a 100K resistor (R40) and a 1% resistor (0402).

**Truth Table for 4-input XOR Gate:**

Inputs	outputs		
W	X	Y	Q = A⊕B⊕C⊕D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Inputs			outputs
W	X	Y	$Q = A \oplus B \oplus C$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

# Resistor comparative

The image shows two circuit diagrams side-by-side, labeled 'PRELIMINARY' in red text. Both circuits are connected to a 5V supply at the top and GND at the bottom. Each circuit contains a resistor (R34/R38 on the left, R35/R39 on the right) with a value of 374K or 124K and a tolerance of 1% 0402. The left circuit has a 1V25 REF voltage across the resistor, while the right circuit has a .3V75 REF voltage across the resistor.

Component	Value	Tolerance	Part Number
Resistor (Left)	374K	1%	0402
Resistor (Right)	124K	1%	0402

## USB-C Polarity Check REFERENCE FIGURES

[illegible]

VA VOIR LE JIRA (its a link btw)

Sheet Name		USB Polarity Check	
Project Title		BeeBoard	
Global Project		PMC	
Size	Group	Revision	
11x17	SwarmUS	1.000	
Date	2021-03-18	Sheet	* of *
Filename		Designers	
BEE_BOARD_USB_C_POLARITYSchDoc		Philippe Arsenault Hubert Dube Louis-Daniel Gaulin	