HiveBoard

PMC

SwarmUS

Revision 1.000

Date : 2020-06-01

Revision history	

GENERAL_POWER_PORT
INSIDE_SHEET_POWER_PORT
ISOLATED_GROUND
GENERAL_GROUND

Package size conversion	
Metric	*Imperial*
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

TOP
HIVE_BOARD_TOP.SchDoc

Block diagram
HIVE_BOARD_BLOCK_DIAG.SchDoc

The following components were changed:

BSS138LT1G → BVSS138LT1G

SMLVT3V3 → SMBJ3V3-M3/5B

Usage notes

Routing notes

Power notes

Questions / TODO

Section name

power

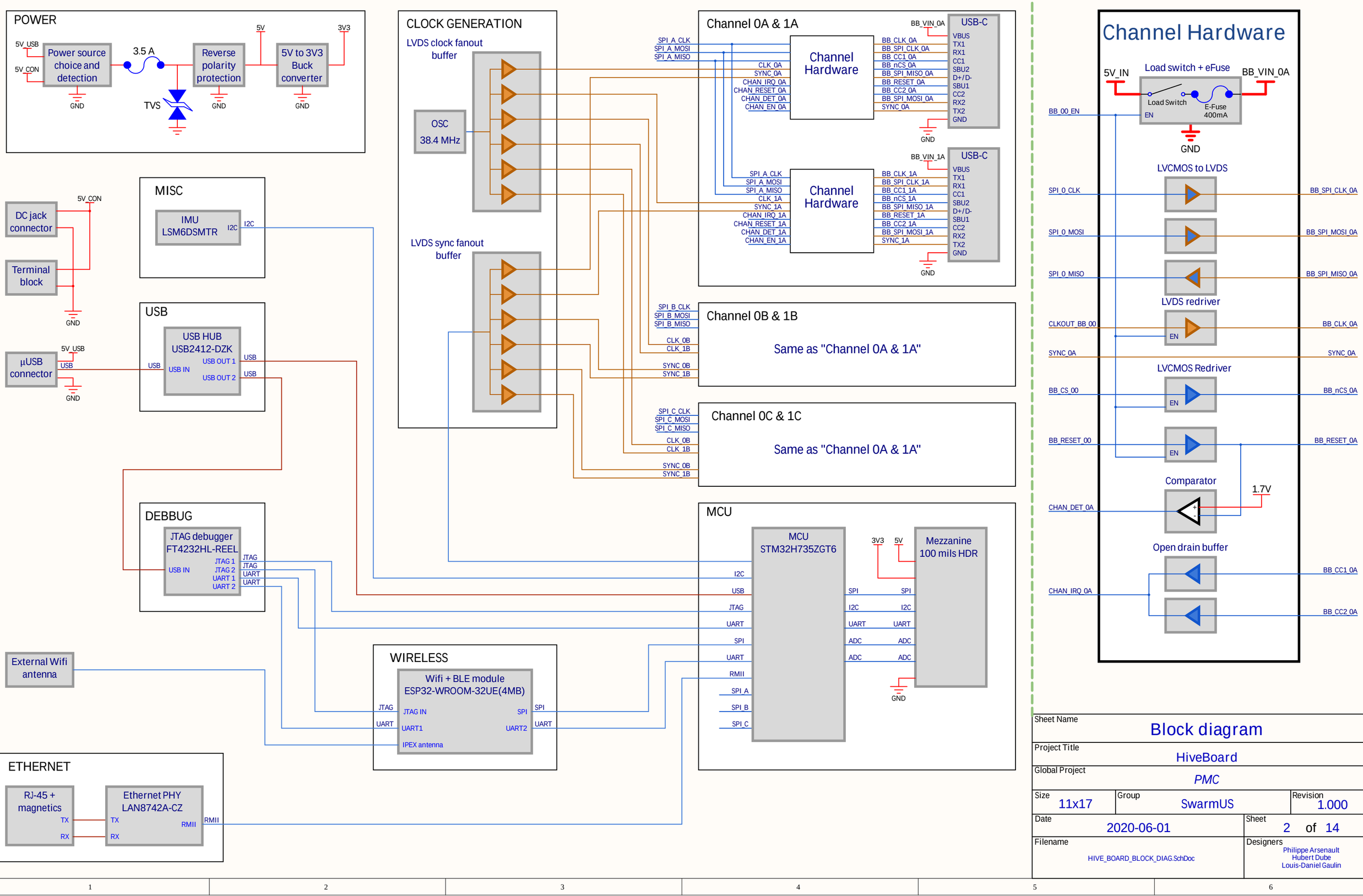
Mounting holes

MTH1 MTH2 MTH3 MTH4

Fiducials

FID1 FID2 FID3
FID 1MM FID 1MM FID 1MM

Project Title: HiveBoard		
Global Project: *PMC*		
Size: 11x17	Group: SwarmUS	Revision: 1.000
Date: 2020-06-01		Sheet: 1 of 14
Filename: HIVE_BOARD_TITLE.SchDoc		Designers: Philippe Arsenault, Hubert Dube, Louis-Daniel Gaulin

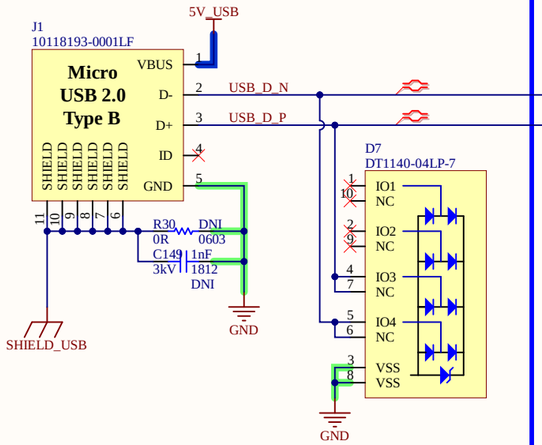


Sheet Name	Block diagram
Project Title	HiveBoard
Global Project	*PMC*
Size	11x17
Group	SwarmUS
Revision	1.000
Date	2020-06-01
Sheet	2 of 14
Filename	HIVE_BOARD_BLOCK_DIAG.SchDoc
Designers	Philippe Arsenault Hubert Dube Louis-Daniel Gaulin

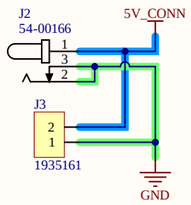
Change components:

Verify PSu wityh EPAD

USB protection and input



Power input DC jack+ terminal



PCB notes:
-Place protection diodes as close as possible to the connector
-Tracks must pass trough protection diode pads

Update block diagram

ETHERNET
HIVE_BOARD_ETHERNET.SchDoc

USB
HIVE_BOARD_USB.SchDoc

DEBUG
HIVE_BOARD_DEBUG.SchDoc

WIRELESS
HIVE_BOARD_WIRELESS.SchDoc

POWER
HIVE_BOARD_POWER.SchDoc

CLOCK GENERATION
HIVE_BOARD_CLOCK_GEN.SchDoc

MCU
HIVE_BOARD_MCU.SchDoc

CHAN NET CLASS

CHAN 0A + 1A
HIVE_BOARD_CHANNEL_HW.SchDoc

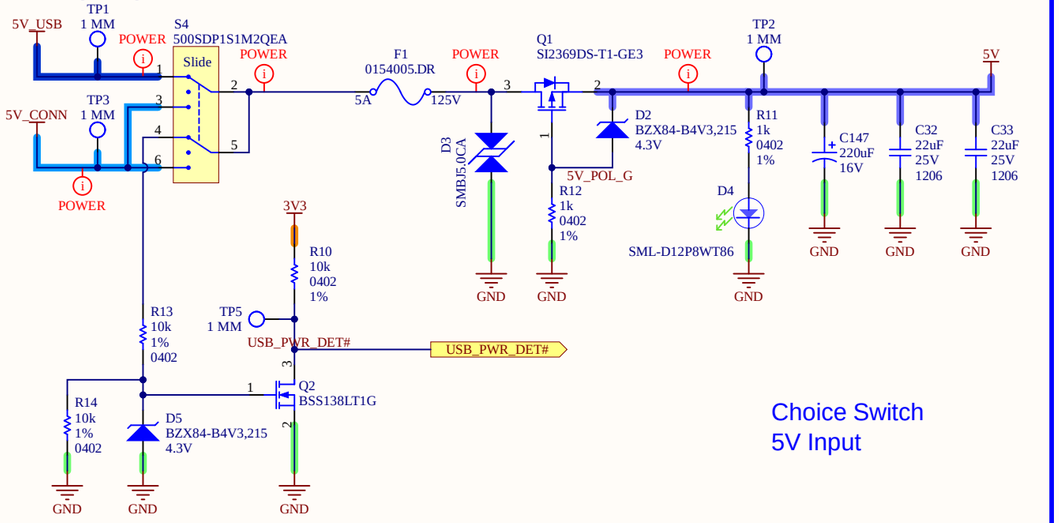
CHAN 0B + 1B
HIVE_BOARD_CHANNEL_HW.SchDoc

CHAN 0C + 1C
HIVE_BOARD_CHANNEL_HW.SchDoc

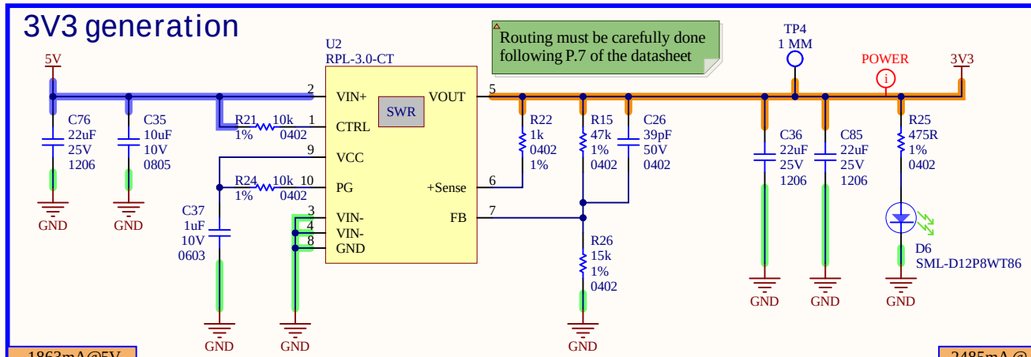
MISC
HIVE_BOARD_MISC.SchDoc

Sheet Name	Top
Project Title	HiveBoard
Global Project	*PMC*
Size: 11x17 / Group: SwarmUS / Revision: 1.000	
Date: 2020-06-01 / Sheet: 3 of 14	
Filename: HIVE_BOARD_TOP.SchDoc	Designers: Philippe Arsenault, Hubert Dube, Louis-Daniel Gaulin

5V input protection + choice

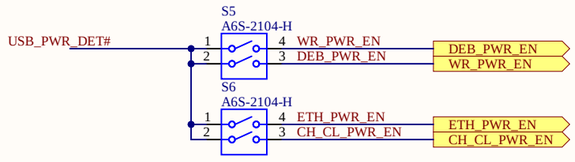


3V3 generation

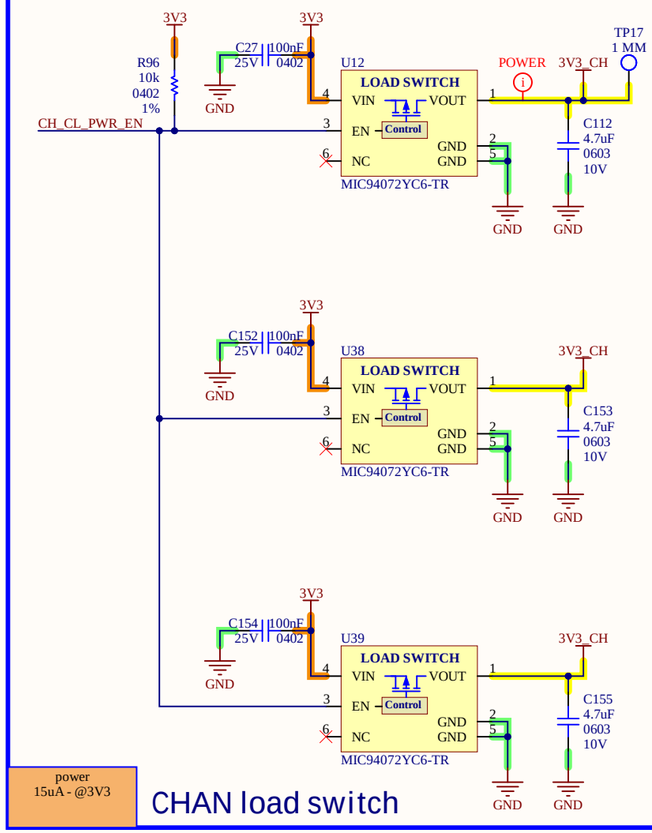


Sheet	Absolute maximum		Estimated - High Power		Estimated - Low Power	
	Current @ 5V	Current @ 3V3	Current @ 5V	Current @ 3V3	Current @ 5V	Current @ 3V3
MCU	-	620 mA	-	100 mA	-	100 mA
CLOCK_GEN	-	160mA + 126mA/3Ch	-	160mA + 126mA/3Ch	-	0 mA
CHANNEL_HW	400 mA/Ch	99 mA/Ch	400 mA/Ch	99 mA/Ch	-	0 mA
USB	-	62 mA	-	62 mA	-	54 mA
ETHERNET	-	117 mA	-	117 mA	-	0mA
DEBUG	-	153 mA	-	153 mA	-	0 mA
WIRELESS	-	394 mA	-	394 mA	-	394 mA
MISC	-	133 mA	-	133 mA	-	2 mA
Total - 3Ch	1200 mA	2359 mA	1200 mA	1839 mA	0 mA	549 mA
Total - 3 Ch @ 5V	2969 mA		2579 mA		402mA	
Total - 6 Ch	2400 mA	2485 mA	2400 mA	1965 mA	N/A	N/A
Total - 6 Ch @ 5V	4263 mA		3873 mA		N/A	

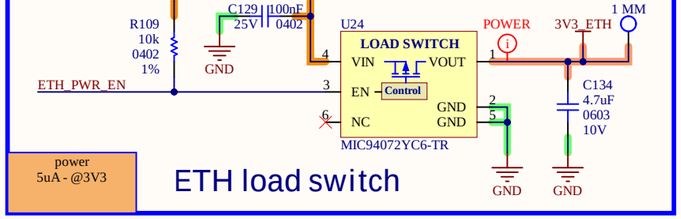
Load switch disable DIP



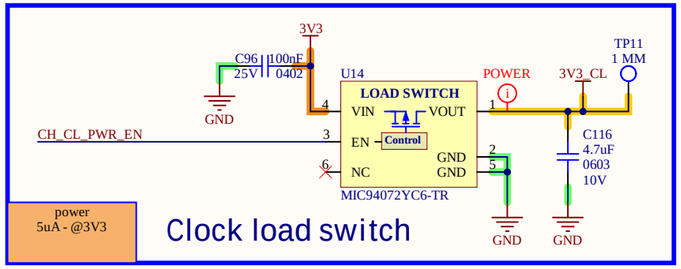
CHAN load switch



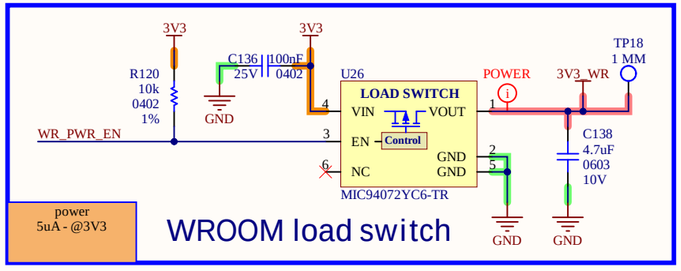
ETH load switch



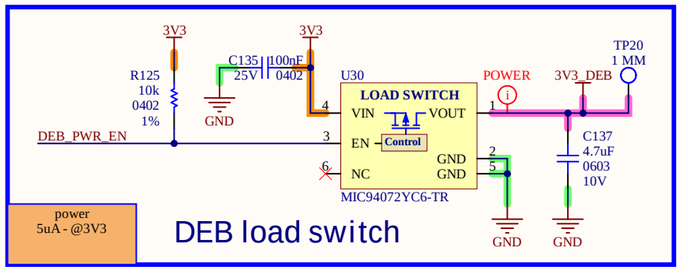
Clock load switch



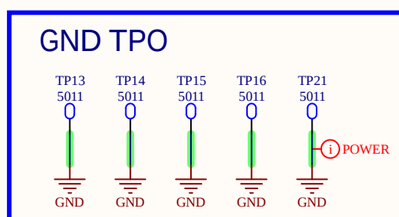
WROOM load switch



DEB load switch



GND TPO



Sheet Name	POWER
Project Title	HiveBoard
Global Project	PMC
Size	11x17
Group	SwarmUS
Revision PCB SCH	.
Date	2020-06-01
Sheet	4 of 14
Filename	HIVE_BOARD_POWER.SchDoc
Designers	Philippe Arsenault Hubert Dube Louis-Daniel Gaulin

PA & PB

U1B
STM32H735ZGT6

PA & PB BANK

PHY_nRST 37 PA0
PHY_MAC_CLK 38 PA1
PHY_MDIO 39 PA2
ETH_PWR_EN 40 PA3
CHAN_RESET_1C 43 PA4
CHAN_RESET_0C 44 PA5
CHAN_IRQ_1C 45 PA6
PHY_CRS 46 PA7
CHAN_EN_0B 97 PA8
USB_STM_VBUS 98 PA9
SYNC 99 PA10
USB_STM_D_N 100 PA11 USB_STM_D_N
USB_STM_D_P 101 PA12 USB_STM_D_P
102 PA13 - JTMS
STM_JTMS 107 PA14 - JTCK
STM_JTCK 108 PA15 - JTDI
STM_JTDI

PB0 49 MEZ_ADC1_N
PB1 50 MEZ_ADC1_P
PB2 51
PB3 - JTDC 130 SPI_nCS_0C
PB4 - JTRS 131 STM_JTDO
PB5 132 STM_NJTRST
PB6 133 WR_PWR_EN
PB7 134 I2C_MISC_SCL
PB8 136 I2C_MISC_SDA
PB9 137 VSPI_nCS0
PB10 66 R162 33R DEB_PWR_EN
PB11 67 1% 0402 SPI_CLK_C
PB12 72 R165 33R PHY_TXEN
PB13 73 R167 33R 1% 0402 PHY_TXD0
PB14 74 1% 0402 PHY_TXD1
PB15 75 R168 33R SPI_MISO_C
1% 0402 SPI_MOSI_C

PC & PD

U1C
STM32H735ZGT6

PC & PD Bank

MCU_LED_1 28
29
MCU_LED_0 30
MCU_LED_HB 31
47
PHY_MDC
PHY_RXD0 48
PHY_RXD1 93
CHAN_DET_1B 94
CHAN_DET_0B 95
CHAN_IRQ_0B 96
SPI_nCS_0B R163 33R 109
SPI_CLK_B 1% 0402 110
SPI_MISO_B R166 33R 111
SPI_MOSI_B 1% 0402 9
IMU_INT1
MCU_LED_B 10
MCU_LED_G 11

PC0 112 CHAN_RESET_1A
PC1 113 CHAN_RESET_0A
PC2_C 114 CHAN_EN_1A
PC3_C 115 CHAN_IRQ_1A
PC4 116 SPI_nCS_1A
PC5 117 CHAN_DET_1A
PC6 120 CHAN_DET_0A
PC7 121 R161 33R SPI_MOSI_A
PC8 76 1% 0402 STM_UTx
PC9 77 STM_URx
PC10 78 SPI_nCS_1C
PC11 81 CHAN_RESET_1B
PC12 82 CHAN_IRQ_1B
PC13 83 CHAN_RESET_0B
PC14 - OSC32_IN 84 CHAN_EN_1B
PC15 - OSC32_OUT 85 SPI_nCS_1B

PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PD8
PD9
PD10
PD11
PD12
PD13
PD14
PD15

Mezzanine connector

3V3 J8 PREC008DAAN-RC 5V
50_OHM_SE

MEZ_SPI_SCK 5 6 MEZ_UART_Rx
MEZ_SPI_MISO 7 8 MEZ_UART_Tx
MEZ_SPI_MOSI 9 10
11 12 MEZ_ADC1_P
MEZ_I2C_SCL 13 14 MEZ_ADC1_N
MEZ_I2C_SDA 15 16

50_OHM_SE
GND GND

MTH5 MTH6
GND GND

PE & PF

U1D
STM32H735ZGT6

PE & PF Bank

UART2_WROOM_Rx 138 PE0
UART2_WROOM_Tx 139 PE1
WROOM_GPIO0 1 PE2
WROOM_EN 2 PE3
IMU_INT2 3 PE4
IO_EXP_INT# 4 PE5
USB_PWR_DET# 5 PE6
MEZ_UART_Rx 57 PE7
MEZ_UART_Tx 58 PE8
59 PE9
CHAN_DET_1C 60 PE10
CHAN_DET_0C 61 PE11
CHAN_EN_0C PE12
MEZ_SPI_SCK R172 33R 62 PE13
MEZ_SPI_MISO 1% 0402 63 PE14
MEZ_SPI_MOSI R173 33R 64 PE15
1% 0402
CHAN_IRQ_0C 65

PF6 20 MCU_LED_R
PF7 21 R169 33R VSPI_CLK
PF8 22 1% 0402 VSPI_MISO/Q
PF9 23 R170 33R VSPI_MOSI/D
PF10 24 1% 0402 MCU_LED_2
PF11 52 CHAN_EN_1C
PF14 53 MEZ_I2C_SCL
PF15 54 MEZ_I2C_SDA

PG & PH

U1E
STM32H735ZGT6

PG & PH Bank

CH_CL_PWR_EN 86 PG6
CLK_OE_1# 87 PG7
CLK_OE_0# 88 PG8
SPI_MISO_A 122 PG9
CHAN_IRQ_0A 123 PG10
R171 33R 124 PG11
SPI_CLK_A 1% 0402 125 PG12
CHAN_EN_0A 126 PG13
SPI_nCS_0A 127 PG14
DEBUG_EN#

PH0-OSC_IN 25
PH0-OSC_OUT 26

50_OHM_SE
50_OHM_SE
R178 0R 3
0402
OUTPUT VDC 4
24MHz
2 GND EN 1 MCU_OSC_EN
X4
O 24,0-JO32-B-1V3-1-T1-LF
GND

3V3 3V3
C1 100nF 25V 0402
R64 10k 0402 1%
GND

VDD

3V3
C2 100nF 25V 0402
C7 100nF 25V 0402
C8 100nF 25V 0402
C9 100nF 25V 0402
C10 100nF 25V 0402
C12 100nF 25V 0402
C13 100nF 25V 0402
C14 100nF 25V 0402
C15 100nF 25V 0402
C16 100nF 25V 0402
C17 100nF 25V 0402
C18 100nF 25V 0402
C19 100nF 25V 0402
C11 4.7uF 25V 0603
GND

1x 100nF per pin + 1x 4.7uF on a pin
Where needed/have the space
DS p.92
Suggested placement is on the bottom if necessary

Decoupling

VDDA

3V3 L1 2k @ 100MHz 400 mA 0805 POW_MCU VDDA
C3 100nF 25V 0402
C6 1uF 10V 0603
GND

VDDLDO

POW_MCU VDDLDO
C20 4.7uF 25V 0603
C21 4.7uF 25V 0603
C22 4.7uF 25V 0603
C23 100nF 25V 0402
C24 100nF 25V 0402
C25 100nF 25V 0402
GND

1x 100nF + 1x 4.7uF per pin

VDDLDO

POW_MCU VCAP
C28 2.2uF 35V 0402
C31 2.2uF 35V 0402
C29 2.2uF 35V 0402
GND

1x 2.2uF per pin

Power inputs + reset

3V3 DNI R116 10k 0402 1% VDDA
R122 0402 10k 1%
GND

U1A
STM32H735ZGT6
Power Supply

BOOT0 135
VDDA 36
VDD 7
VDD 13
VDD 19
VDD 32
VDD 42
VDD 56
VDD 71
VDD 79
VDD 92
VDD 106
VDD 119
VDD 129
VDD 144
VBAT 8
VCAP 68
VCAP 103
VCAP 140
VDDLDO 70
VDDLDO 105
VDDLDO 143
VDD50USB 90
VDD33USB 91

RST 27 MCU_RST#
VSSA 34
VSS 6
VSS 12
VSS 18
VSS 33
VSS 41
VSS 55
VSS 69
VSS 80
VSS 89
VSS 104
VSS 118
VSS 128
VSS 141
VSSSMPS 14
VLXSMPS 15
VDDSMPS 16
VFBSMPS 17
VREF+ 35
PDR_ON 142

R8 1k 1% 0402
S3 435171014816
C4 1uF 10V 0603
R9 150R 1% 0402
GND

POW_MCU
C30 1uF 10V 0603
C5 100nF 25V 0402
VDDLDO
C123 4.7uF 25V 0603
R130 47R 1% 0402 VDDA
R175 10k 0402 1%
R176 10k 0402 1% DNI
3V3
GND

AN5419 is useful

abs. max: 600mA @ 3V3
typ : 100mA @ 3V3

The following signals can be moved to facilitate the routing:
- DW_RESET_XX
- DW_IRQ_XX
- DW_nCS_XX
- USER_GPIOX
- UART
- SPI ports
- WROOM EN

VDD
VDDSMPS
VLXSMPS
VFBSMPS
VSSSMPS
VCAP
VDDLDO
VSS
SMPS (off)
V reg (on)
VCORE
VDDLDO <= VDD
1. LDO Supply

Heatsink

HS1
ATS-CPX025025015-138-C2-R0
Heat sink
25x25x15mm
12.20°C/W @ 100LFM
Mouting holes must be added

MEC1 SMTSO-M3-2ET
MEC2 SMTSO-M3-2ET
GND

MCU LEDs

3V3 D1 EAST1616RGBA3
VDD
MCU_LED_B 475R R1 1% 0402 B
MCU_LED_G 475R R2 1% 0402 G
MCU_LED_R R3 1k 1% 0402 R
RGB state LED

LED 0
MCU_LED_0 SML-D12P8WT86 D22 475R R5 1% 0402 3V3

LED 1
MCU_LED_1 SML-D12P8WT86 D23 475R R23 1% 0402 3V3

LED 2
MCU_LED_2 SML-D12P8WT86 D24 475R R33 1% 0402 3V3

LED HB
MCU_LED_HB SML-D12P8WT86 D25 475R R129 1% 0402 3V3

Green LED = 2.75mA @1.97V
B = 2.7V @ 1mA
G = 2.8V @ 1mA
R = 1.7V @ 1.6mA
14.6mA @3V3

5V 3V3
D27 SMBJ5.0CA
D28 SMLVT3V3
GND GND

D26 DT1140-04LP-7
MEZ_SPI_SCK 1 10 IO1 NC
MEZ_SPI_MISO 2 9 IO2 NC
MEZ_SPI_MOSI 4 7 IO3 NC
5 6 IO4 NC
3 8 VSS VSS
GND

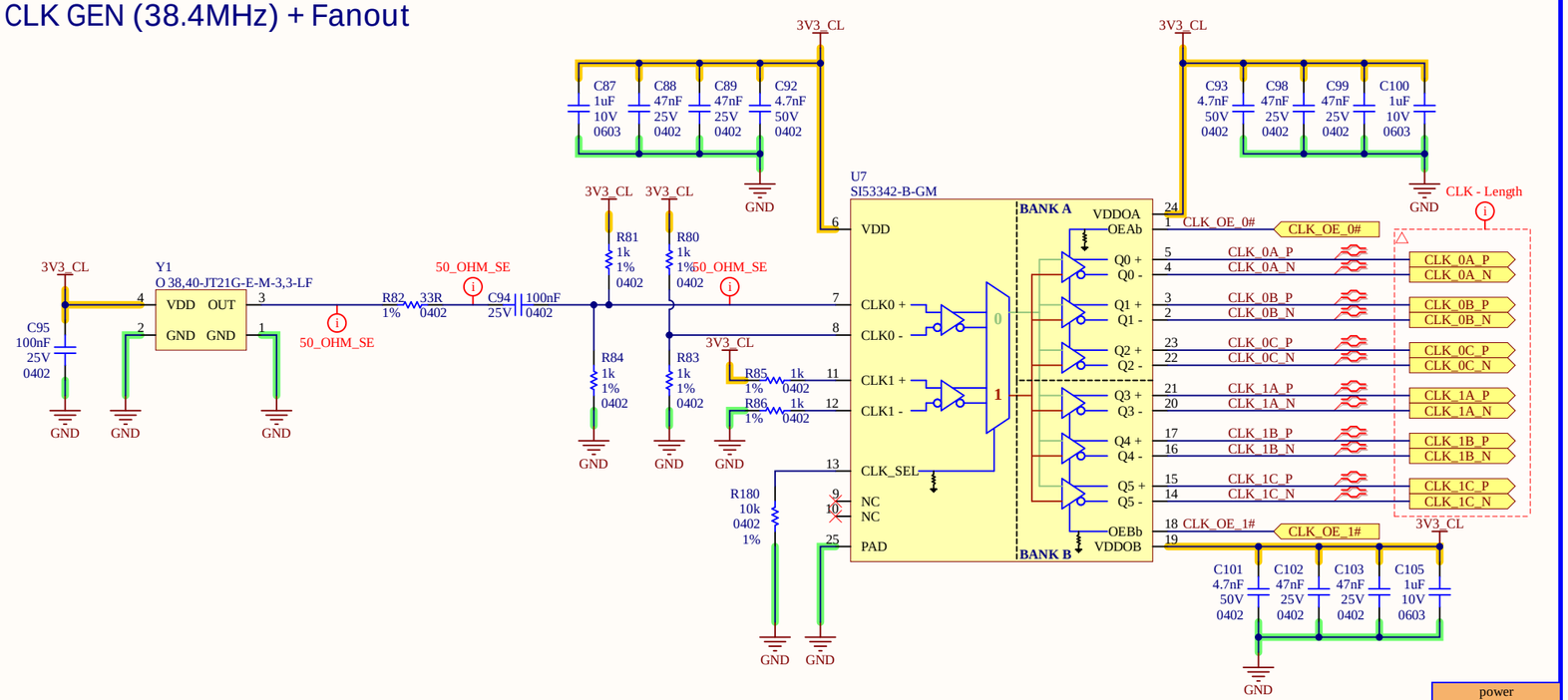
D29 DT1140-04LP-7
MEZ_UART_Rx 1 10 IO1 NC
MEZ_UART_Tx 2 9 IO2 NC
4 7 IO3 NC
5 6 IO4 NC
3 8 VSS VSS
GND

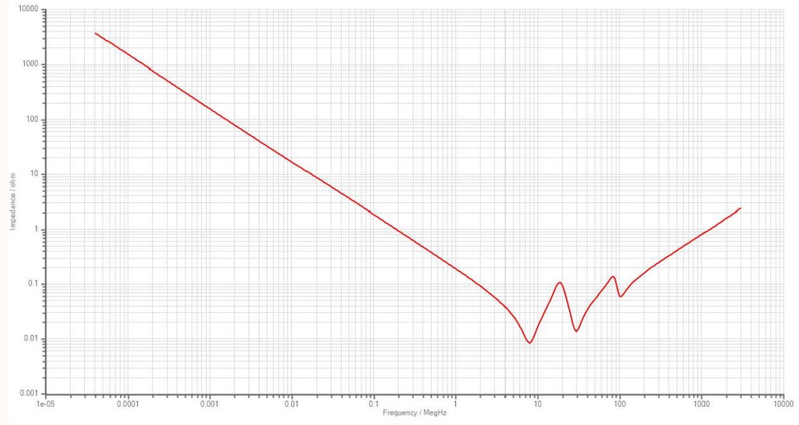
D30 DT1140-04LP-7
MEZ_ADC1_P 1 10 IO1 NC
MEZ_ADC1_N 2 9 IO2 NC
MEZ_I2C_SCL 4 7 IO3 NC
MEZ_I2C_SDA 5 6 IO4 NC
3 8 VSS VSS
GND

MCU NET CLASS

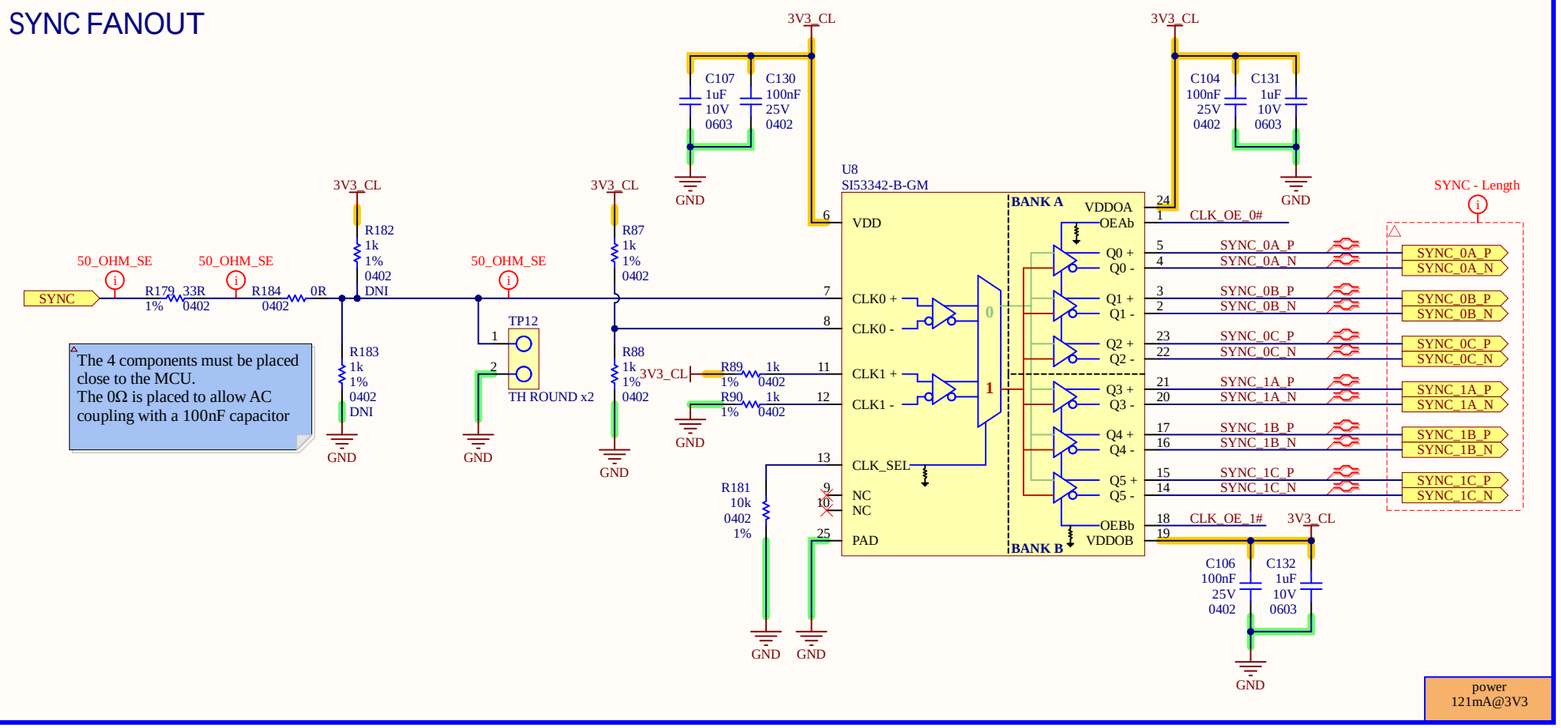
Sheet Name	MCU
Project Title	HiveBoard
Global Project	PMC
Size	11x17
Group	SwarmUS
Revision PCB SCH	.
Date	2020-06-01
Sheet	5 of 14
Filename	HIVE_BOARD_MCU.SchDoc
Designers	Philippe Arsenault Hubert Dube Louis-Daniel Gaulin

CLK GEN (38.4MHz) + Fanout



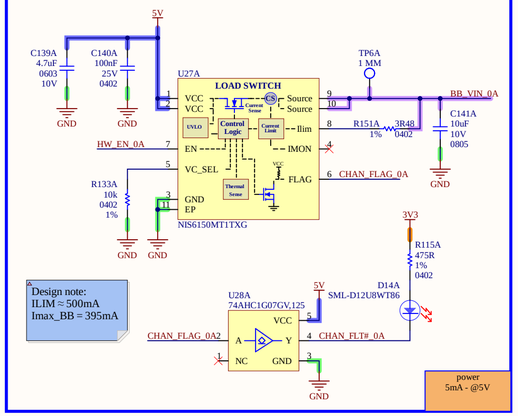


SYNC FANOUT

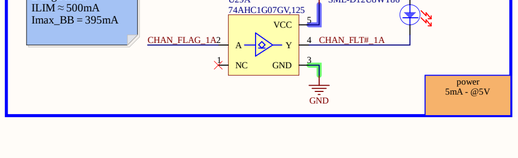


Sheet Name	CLOCK GEN & FANOUT
Project Title	HiveBoard
Global Project	*PMC*
Size: 11x17 / Group: SwarmUS / Revision PCB SCH	.
Date: 2020-06-01	Sheet: 6 of 14
Filename: HIVE_BOARD_CLOCK_GEN.SchDoc	Designers: Philippe Arsenault, Hubert Dube, Louis-Daniel Gaulin

Channel 0 BB Load Switch



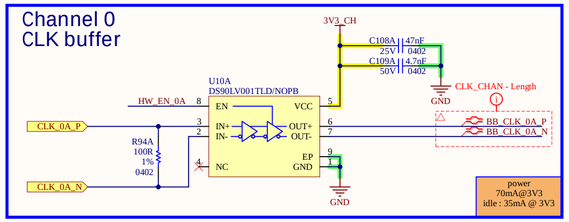
Channel 0 Enable and LED



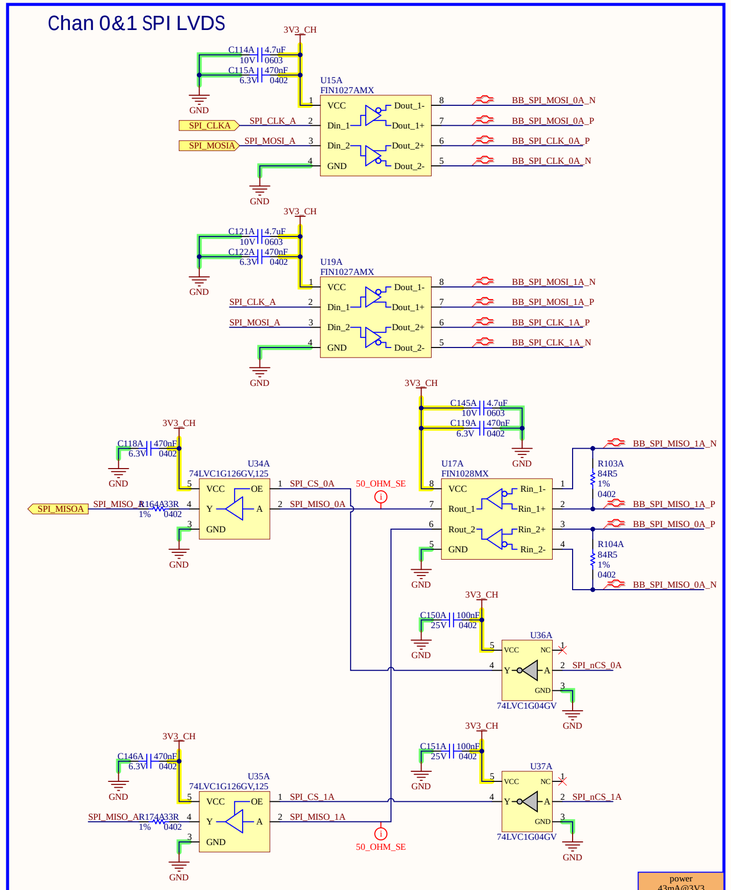
Channel 1 Enable and LED

Channel 1 BB Load Switch

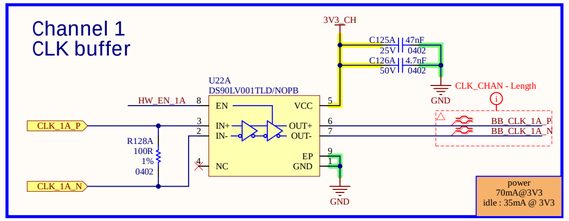
Channel 0 CLK buffer



Chan 0&1 SPI LVDS



Channel 1 CLK buffer

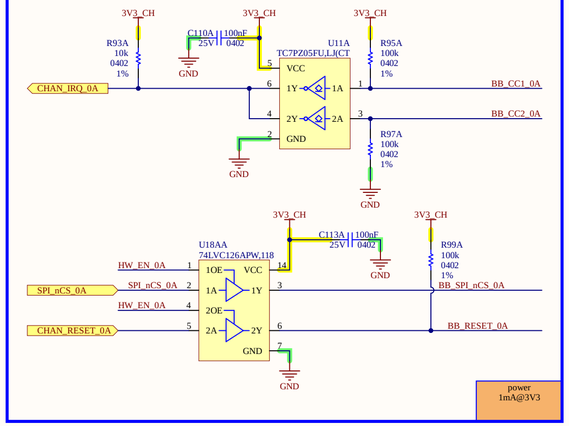


State	nCS_0	nCS_1	OE_0	OE_1	Y_0	Y_1
DW1000_0 COM.	0	1	1	0	MISO_0	3-state
DW1000_1 COM.	1	0	0	1	3-state	MISO_1
No COM.	1	1	0	0	3-state	3-state

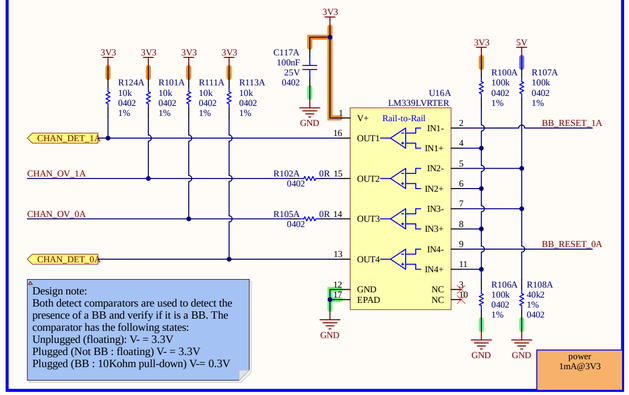
Design note:
The LVCMOS output of the LVDS receiver cannot be 3-stated. Therefore, 3-state buffers are used

nCS is kept low for the entire duration of the DW1000 message. The attached table shows the 3-state logic:

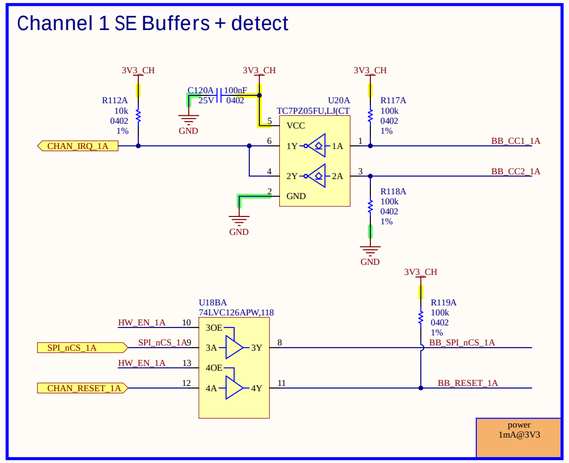
Channel 0 SE Buffers + detect



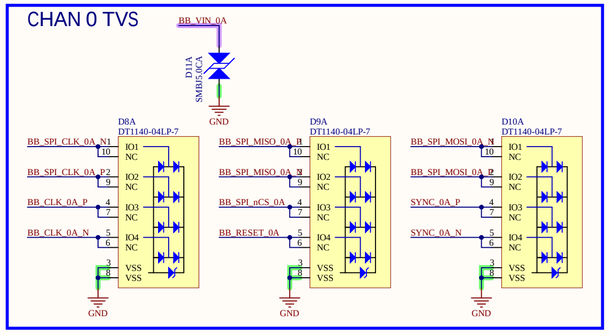
Channel 1+2 Det & OV



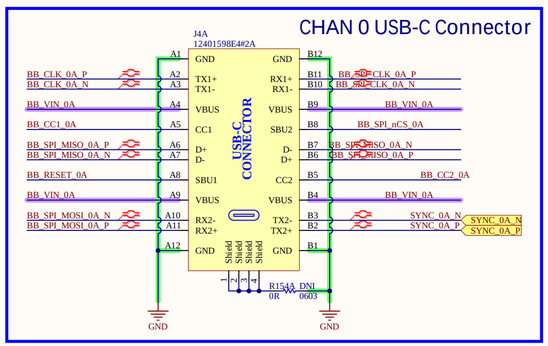
Channel 1 SE Buffers + detect



CHAN 0 TVS

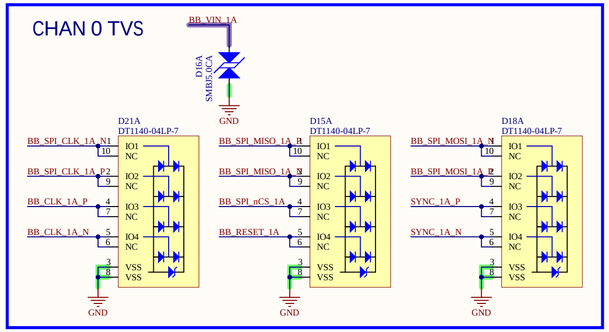


CHAN 0 USB-C Connector



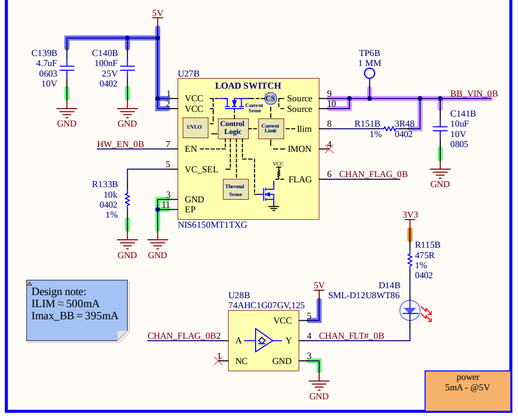
CHAN 1 USB-C Connector

CHAN 0 TVS

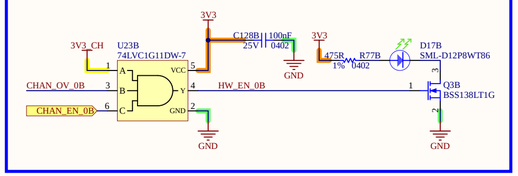


Sheet Name	CHANNEL HARDWARE & CONNECTOR
Project Title	HiveBoard
Global Project	*PMC*
Size: 11x17 / Group: SwarmUS / Revision: 1.000	
Date: 2020-06-01 / Sheet: 7.1 of 14	
Filename: HIVE_BOARD_CHANNEL_HWSchDoc	Designers: Philippe Arsenault, Hubert Dube, Louis-Daniel Gaulin

Channel 0 BB Load Switch

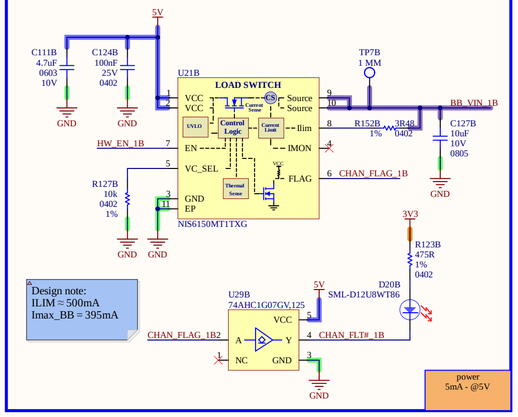


Channel 0 Enable and LED

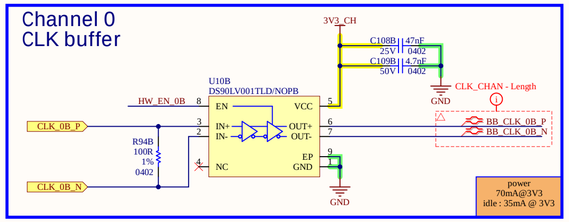


Channel 1 Enable and LED

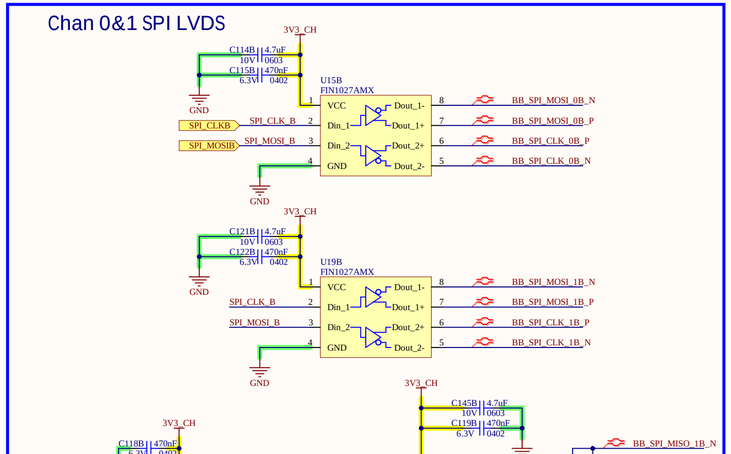
Channel 1 BB Load Switch



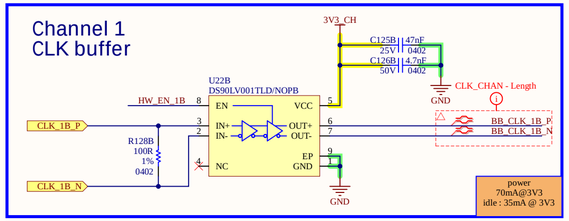
Channel 0 CLK buffer



Chan 0&1 SPI LVDS



Channel 1 CLK buffer

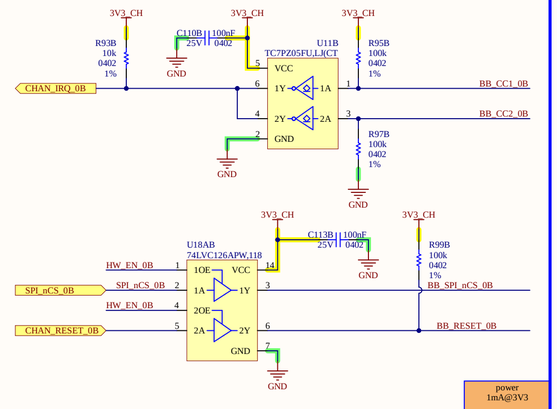


State	nCS_0	nCS_1	OE_0	OE_1	Y_0	Y_1
DW1000_0 COM.	0	1	1	0	MISO_0	3-state
DW1000_1 COM.	1	0	0	1	3-state	MISO_1
No COM.	1	1	0	0	3-state	3-state

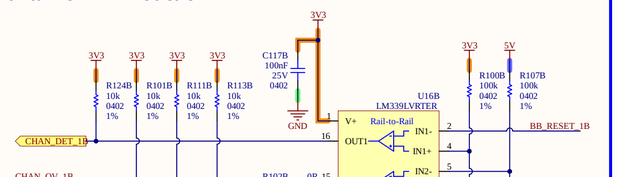
Design note:
The LVCMOS output of the LVDS receiver cannot be 3-stated. Therefore, 3-state buffers are used

nCS is kept low for the entire duration of the DW1000 message. The attached table shows the 3-state logic:

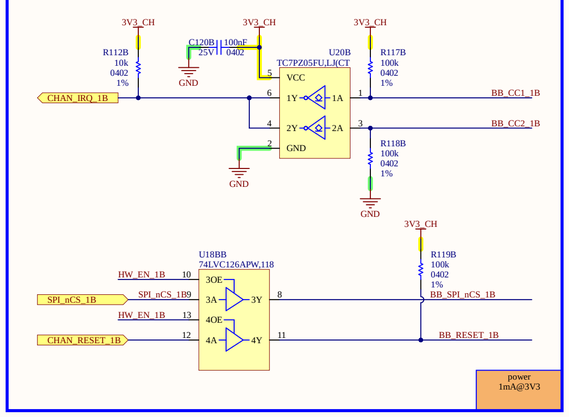
Channel 0 SE Buffers + detect



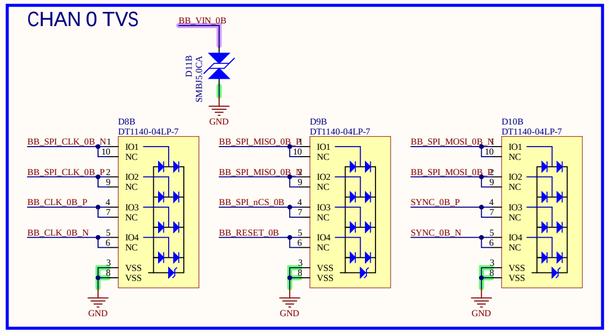
Channel 1+2 Det & OV



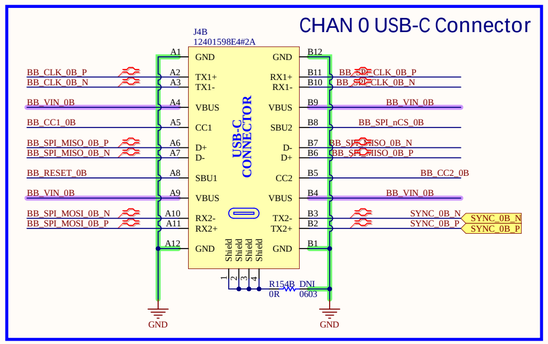
Channel 1 SE Buffers + detect



CHAN 0 TVS

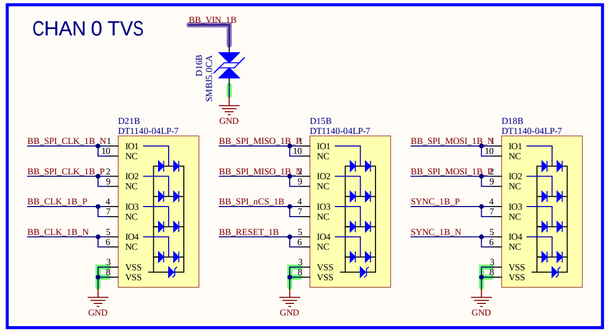


CHAN 0 USB-C Connector



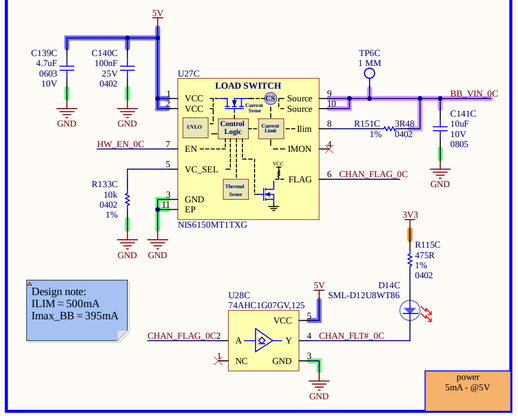
CHAN 1 USB-C Connector

CHAN 0 TVS

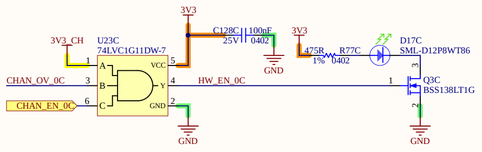


Sheet Name	CHANNEL HARDWARE & CONNECTOR
Project Title	HiveBoard
Global Project	*PMC*
Size: 11x17 / Group: SwarmUS / Revision: 1.000	
Date: 2020-06-01 / Sheet: 7.2 of 14	
Filename: HIVE_BOARD_CHANNEL_HWSchDoc	Designers: Philippe Arsenault, Hubert Dube, Louis-Daniel Gaulin

Channel 0 BB Load Switch

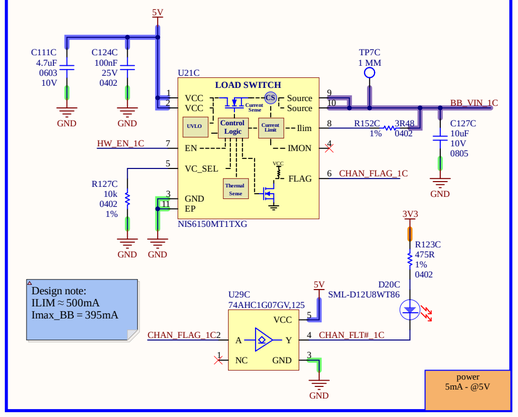


Channel 0 Enable and LED

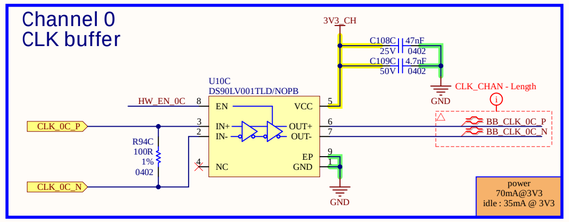


Channel 1 Enable and LED

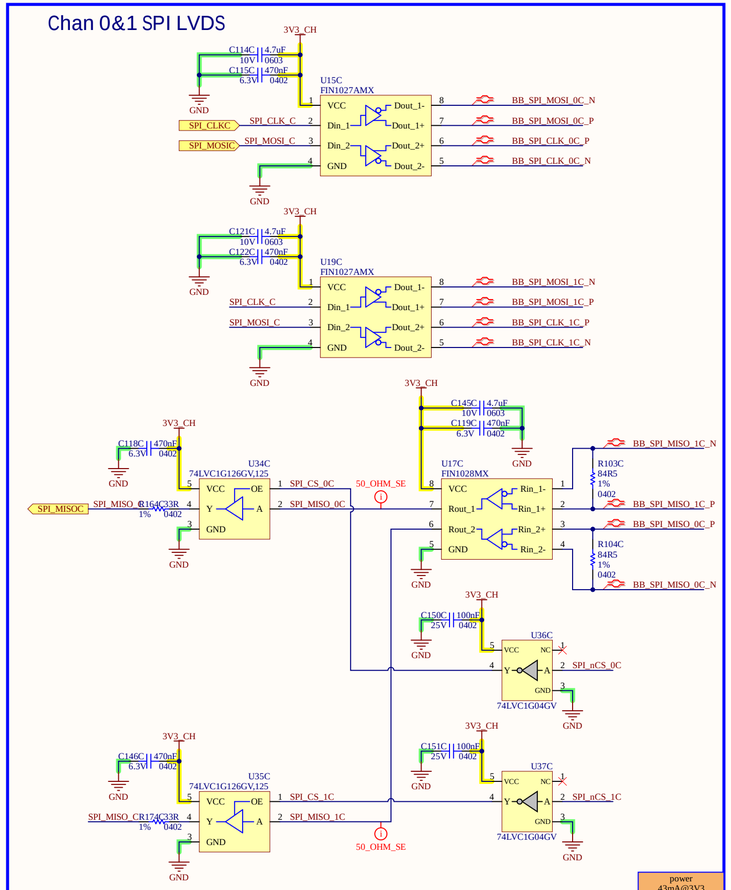
Channel 1 BB Load Switch



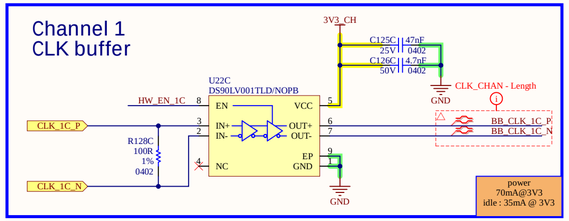
Channel 0 CLK buffer



Chan 0&1 SPI LVDS



Channel 1 CLK buffer



State	nCS_0	nCS_1	OE_0	OE_1	Y_0	Y_1
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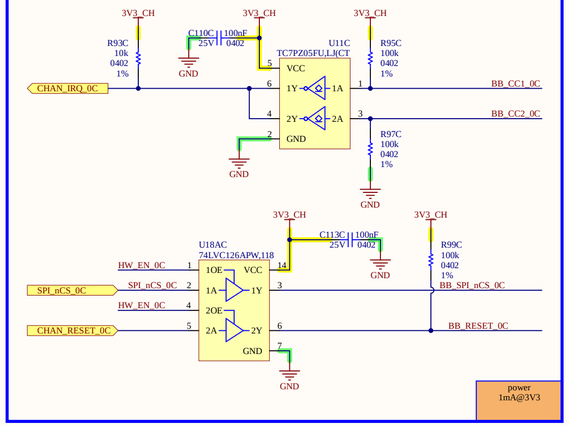
DW1000_1 COM.	1	0	0	1	3-state	MISO_1
No COM.	1	1	0	0	3-state	3-state

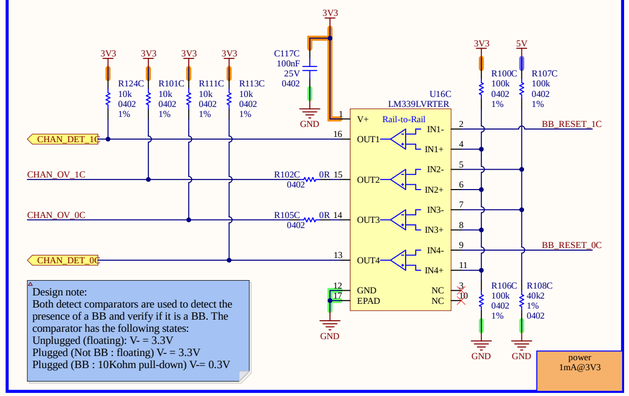
Design note:
The LVCMOS output of the LVDS receiver cannot be 3-stated. Therefore, 3-state buffers are used

nCS is kept low for the entire duration of the DW1000 message. The attached table shows the 3-state logic:

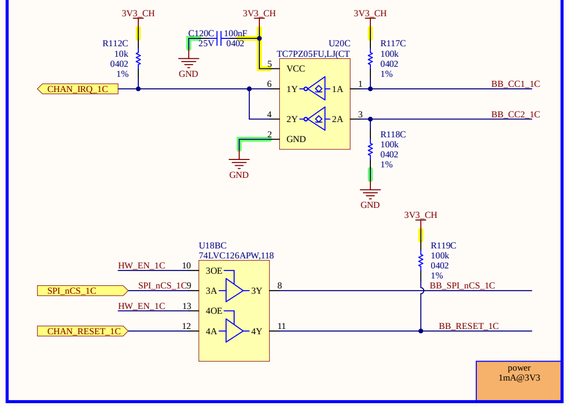
Channel 0 SE Buffers + detect



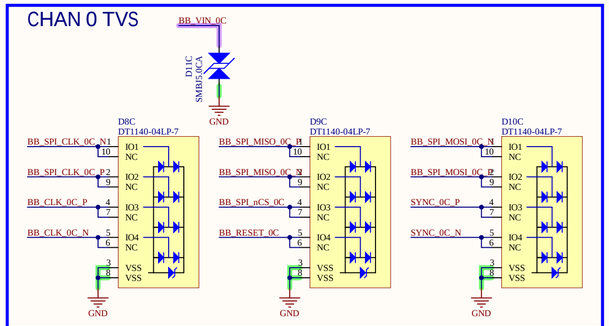
Channel 1+2 Det & OV



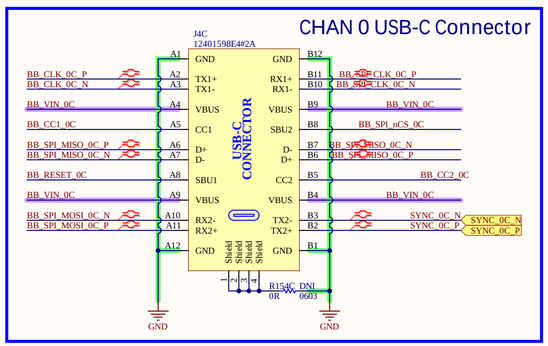
Channel 1 SE Buffers + detect



CHAN 0 TVS

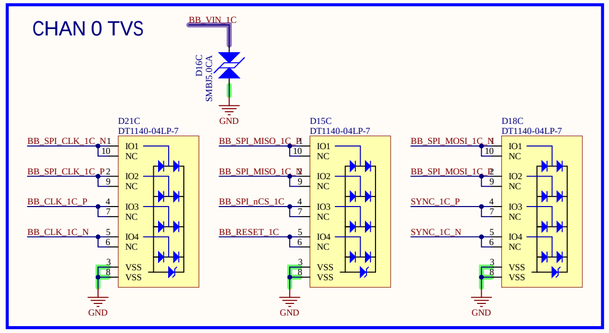


CHAN 0 USB-C Connector



CHAN 1 USB-C Connector

CHAN 0 TVS

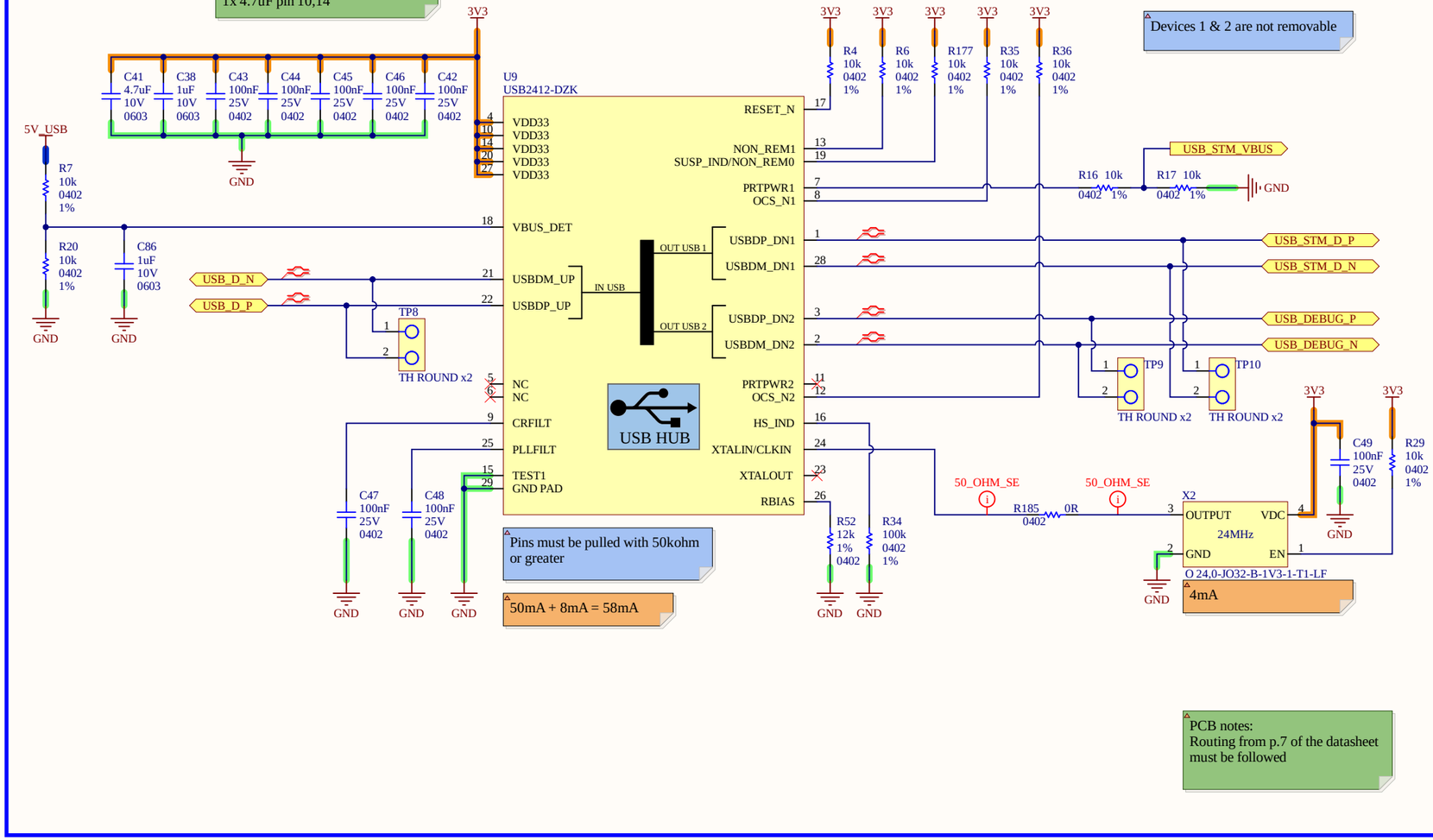


Sheet Name	CHANNEL HARDWARE & CONNECTOR
Project Title	HiveBoard
Global Project	*PMC*
Size: 11x17 / Group: SwarmUS / Revision: 1.000	
Date: 2020-06-01 / Sheet: 7.3 of 14	
Filename: HIVE_BOARD_CHANNEL_HWSchDoc	Designers: Philippe Arsenault, Hubert Dube, Louis-Daniel Gaulin

USB Hub

PCB notes:
1x 100nF per pin
1x 1uF pin 4,20,27
1x 4.7uF pin 10,14

Devices 1 & 2 are not removable



Pins must be pulled with 50kohm or greater

50mA + 8mA = 58mA

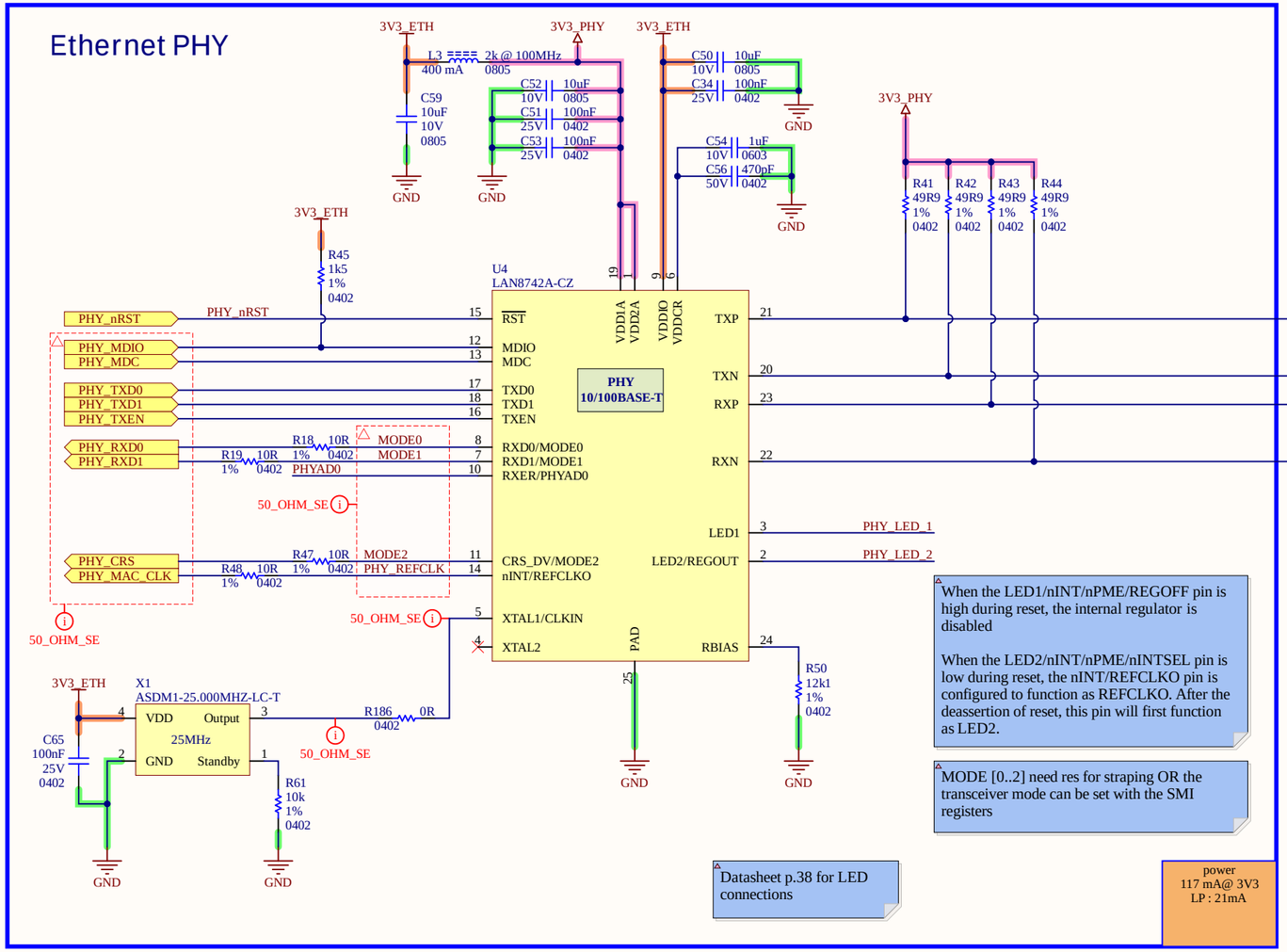
4mA

power
MAX : 62mA@3V3
LP : 54mA@3V3

PCB notes:
Routing from p.7 of the datasheet must be followed

Sheet Name	USB Hub
Project Title	HiveBoard
Global Project	*PMC*
Size: 11x17 / Group: SwarmUS / Revision PCB SCH: .	
Date: 2020-06-01	Sheet: 8 of 14
Filename: HIVE_BOARD_USB.SchDoc	Designers: Philippe Arsenault, Hubert Dube, Louis-Daniel Gaulin

Ethernet PHY



When the LED1/nINT/nPME/REGOFF pin is high during reset, the internal regulator is disabled

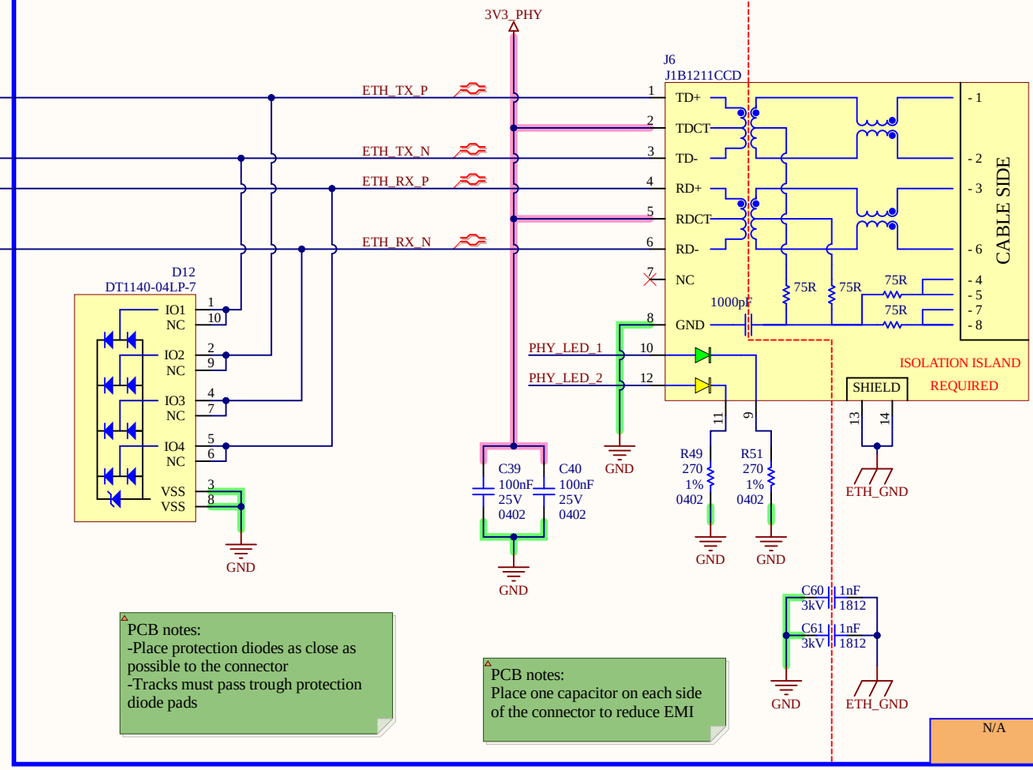
When the LED2/nINT/nPME/nINTSEL pin is low during reset, the nINT/REFCLKO pin is configured to function as REFCLKO. After the deassertion of reset, this pin will first function as LED2.

MODE [0..2] need res for straping OR the transceiver mode can be set with the SMI registers

Datasheet p.38 for LED connections

power
117 mA@ 3V3
LP : 21mA

RJ45 magnetics + protections



PCB notes:
- Create isolation island in the middle of the connector to protect against ESD
- Keep a distance of at least 1.5mm between isolated components and copper

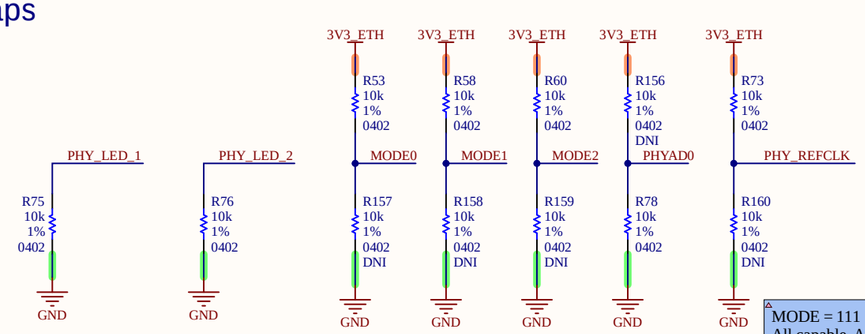
PCB notes:
-Place protection diodes as close as possible to the connector
-Tracks must pass trough protection diode pads

PCB notes:
Place one capacitor on each side of the connector to reduce EMI

N/A

RMII CLOCK frequency is 50MHz.
13ieme harmonique is 650MHz.
Wavelength is 46cm
IF MAC CLK is less than 11cm : not considered a transmission line

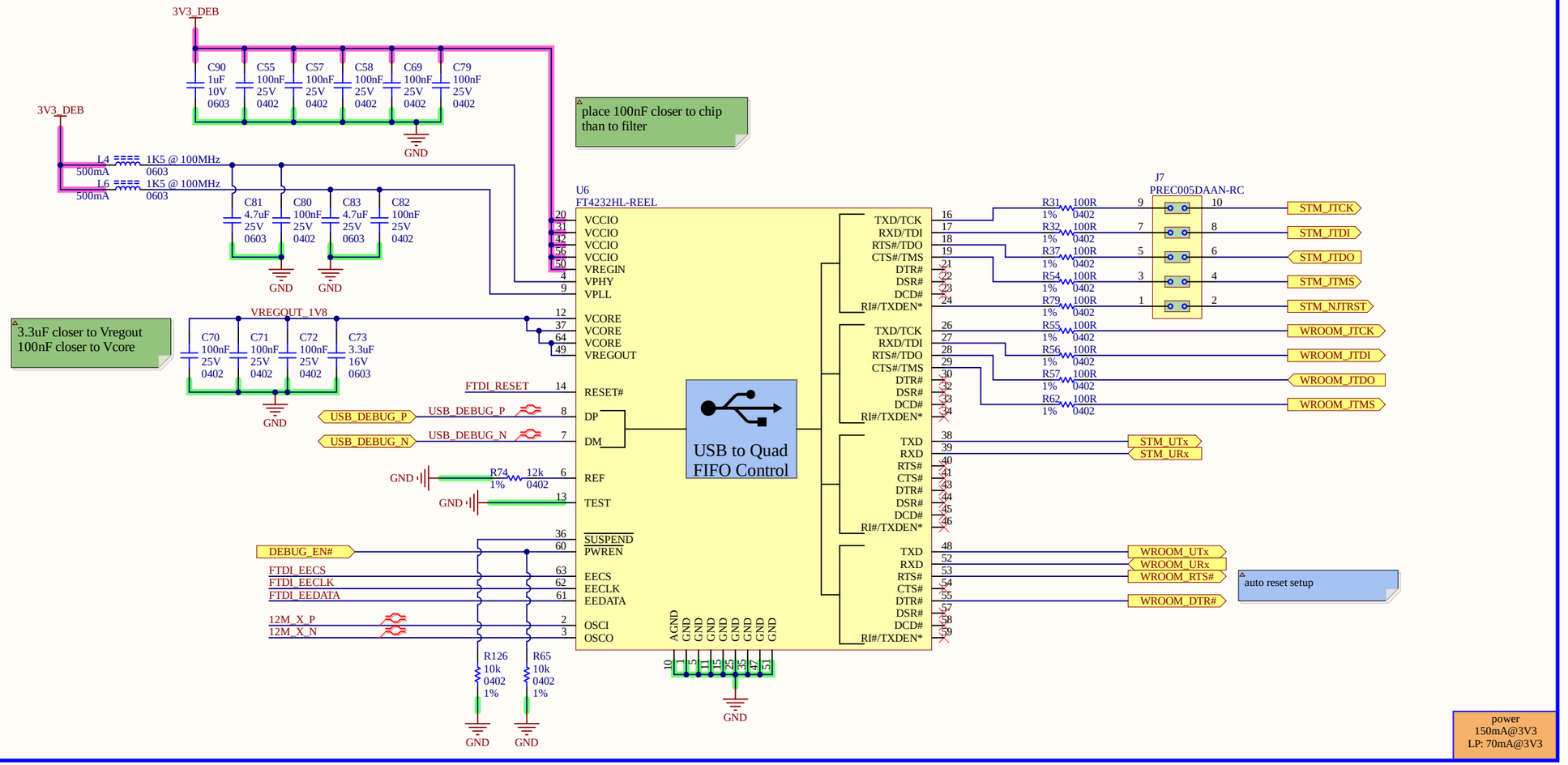
Straps



MODE = 111
All capable. Auto-negotiation enabled

Sheet Name	ETHERNET
Project Title	HiveBoard
Global Project	*PMC*
Size: 11x17 / Group: SwarmUS / Revision PCB SCH: .	
Date: 2020-06-01	Sheet: 9 of 14
Filename: HIVE_BOARD_ETHERNET.SchDoc	Designers: Philippe Arsenault, Hubert Dube, Louis-Daniel Gaulin

FTDI Debug Chip



J10 SNT-100-BK-T-H

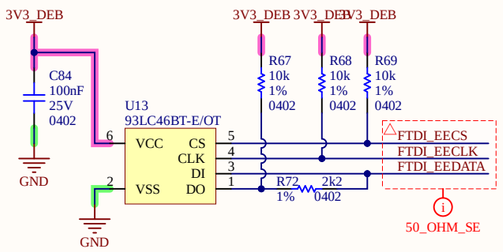
J13 SNT-100-BK-T-H

J15 SNT-100-BK-T-H

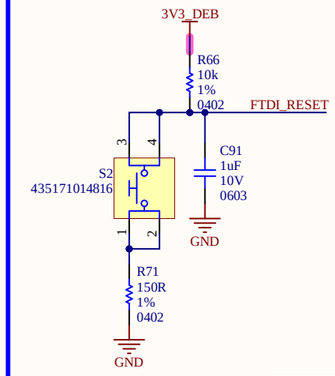
J17 SNT-100-BK-T-H

J12 SNT-100-BK-T-H

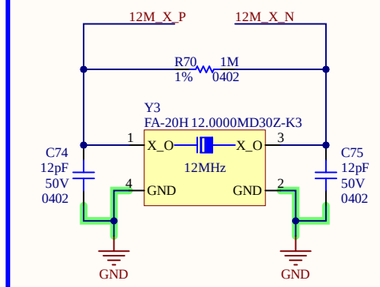
EEPROM



Reset BTN

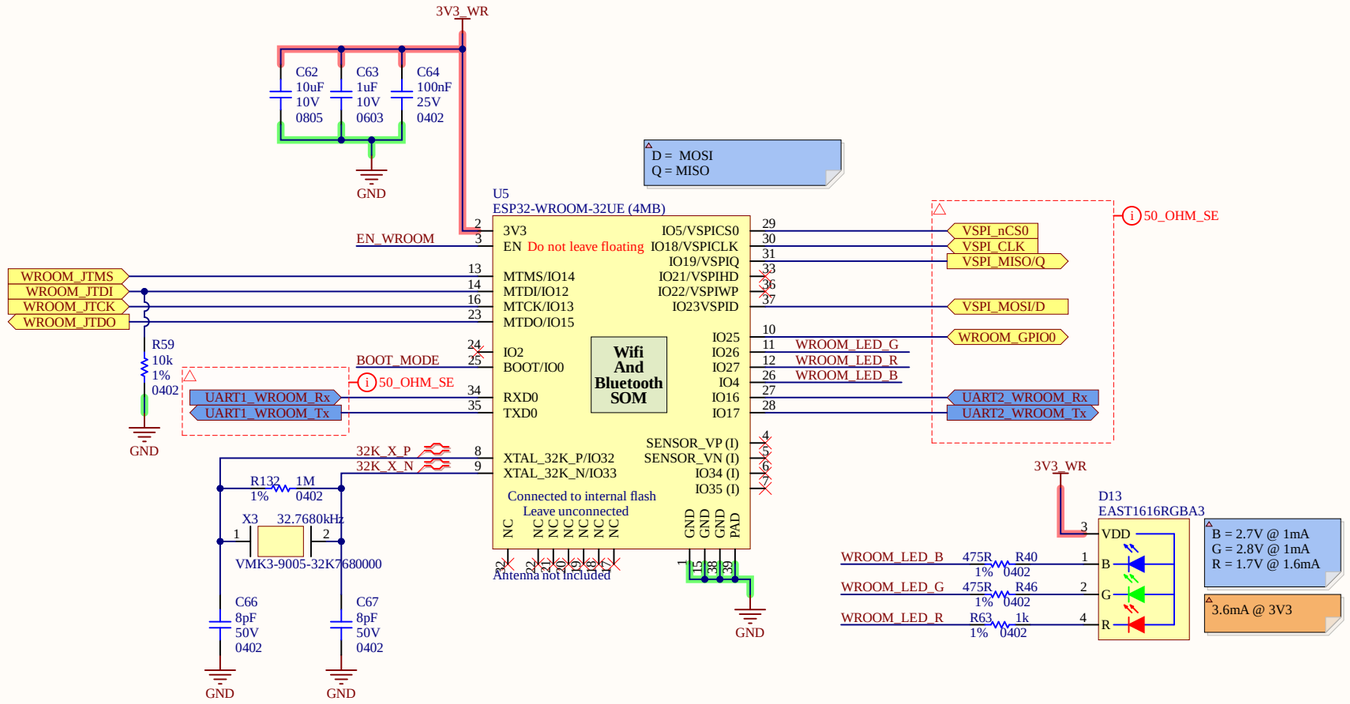


Crystal

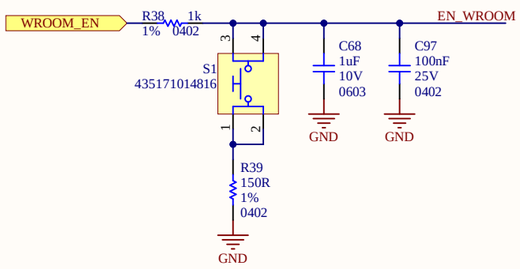


Sheet Name	DEBUG
Project Title	HiveBoard
Global Project	*PMC*
Size	11x17
Group	SwarmUS
Revision PCB SCH	.
Date	2020-06-01
Sheet	10 of 14
Filename	HIVE_BOARD_DEBUG.SchDoc
Designers	Philippe Arsenault Hubert Dube Louis-Daniel Gaulin

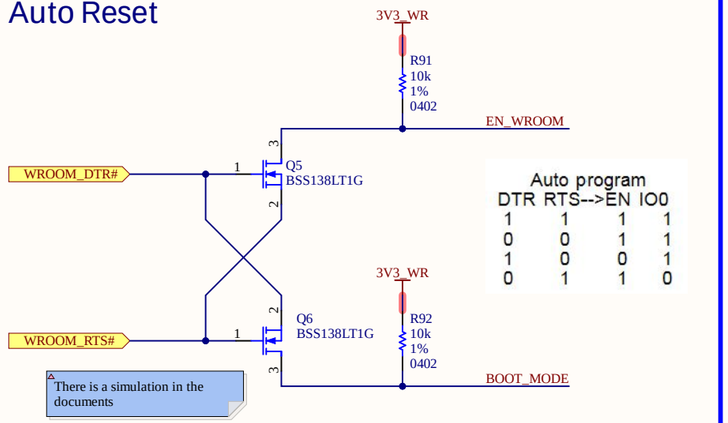
WROOM



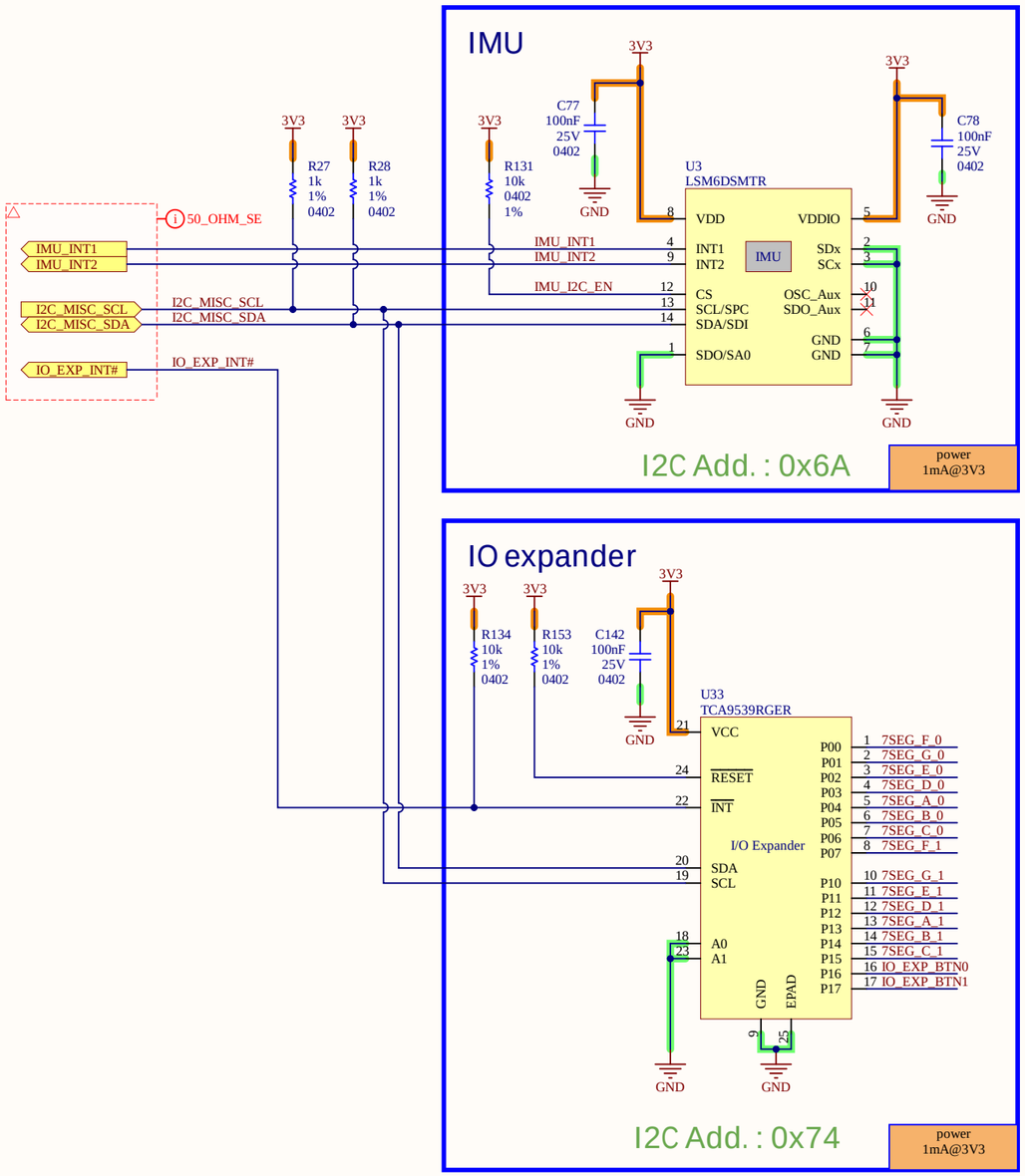
Reset BTN



Auto Reset



Sheet Name	WIRELESS	
Project Title	HiveBoard	
Global Project	*PMC*	
Size: 11x17	Group: SwarmUS	Revision PCB SCH: .
Date: 2020-06-01	Sheet: 11 of 14	
Filename: HIVE_BOARD_WIRELESS.SchDoc	Designers: Philippe Arsenault, Hubert Dube, Louis-Daniel Gaulin	



Sheet Name	MISC
Project Title	HiveBoard
Global Project	*PMC*
Size	11x17
Group	SwarmUS
Revision PCB SCH	.
Date	2020-06-01
Sheet	12 of 14
Filename	HIVE_BOARD_MISC.SchDoc
Designers	Philippe Arsenault Hubert Dube Louis-Daniel Gaulin