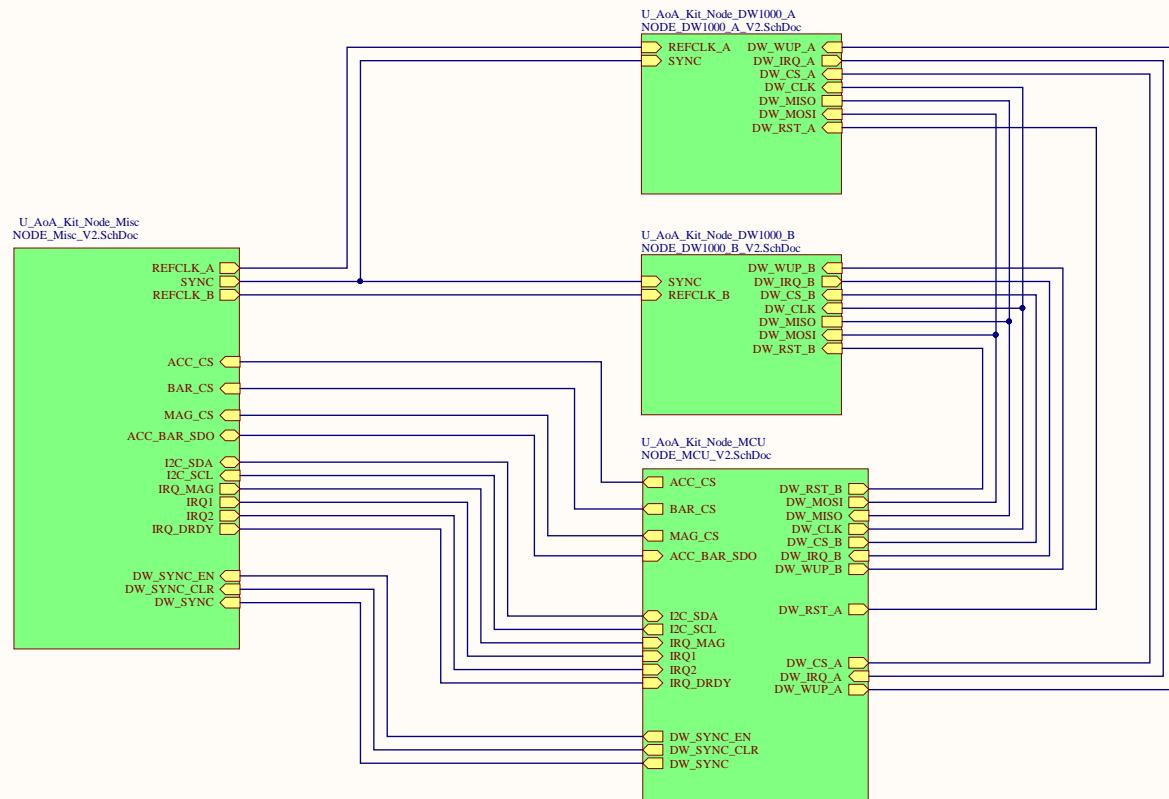
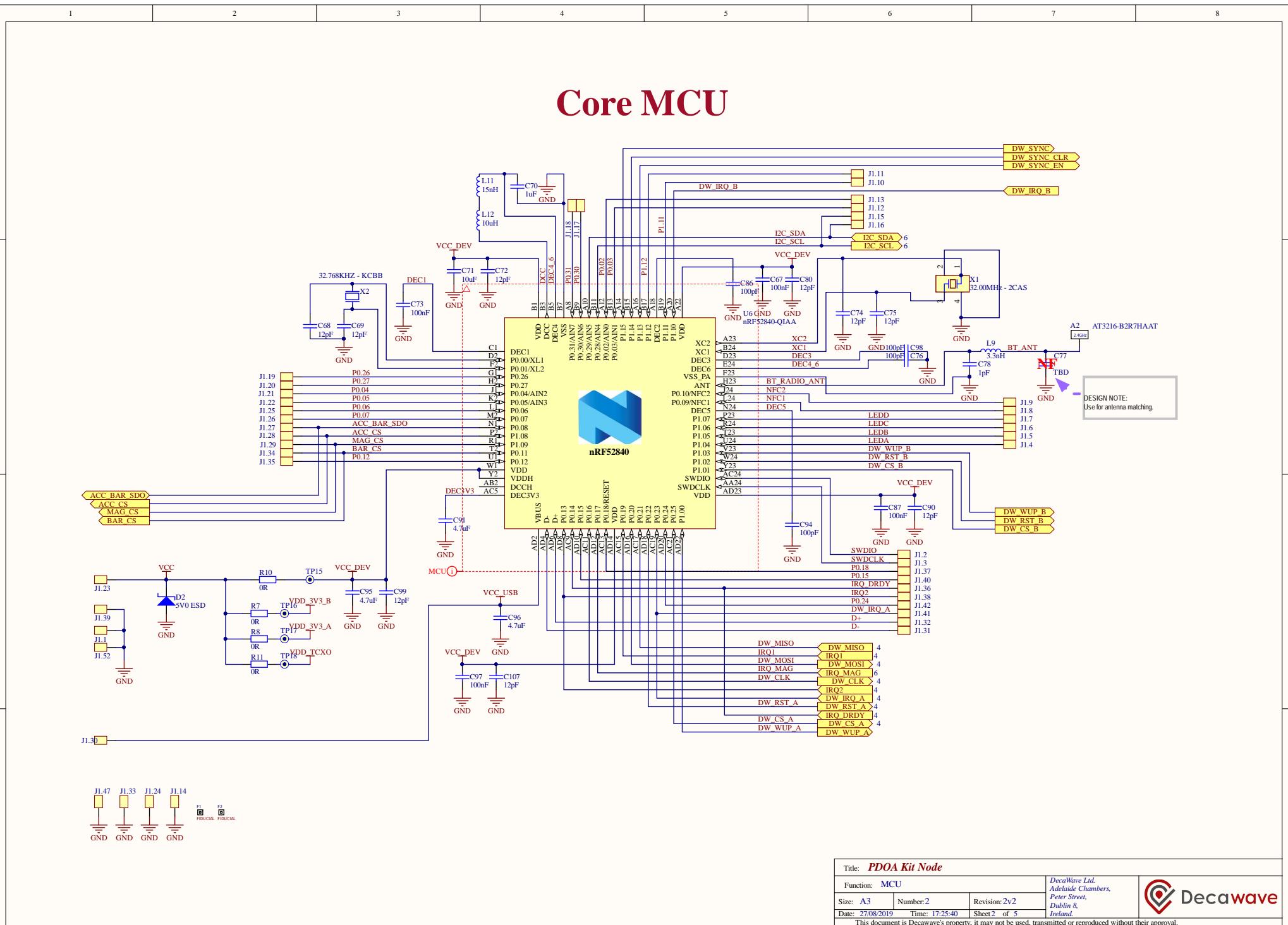
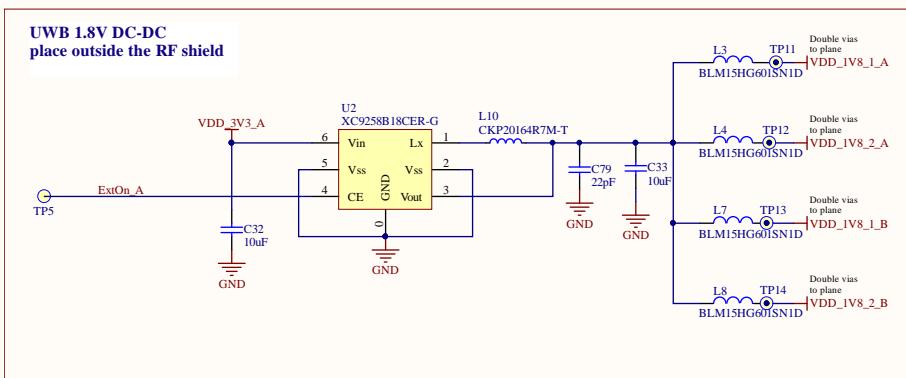
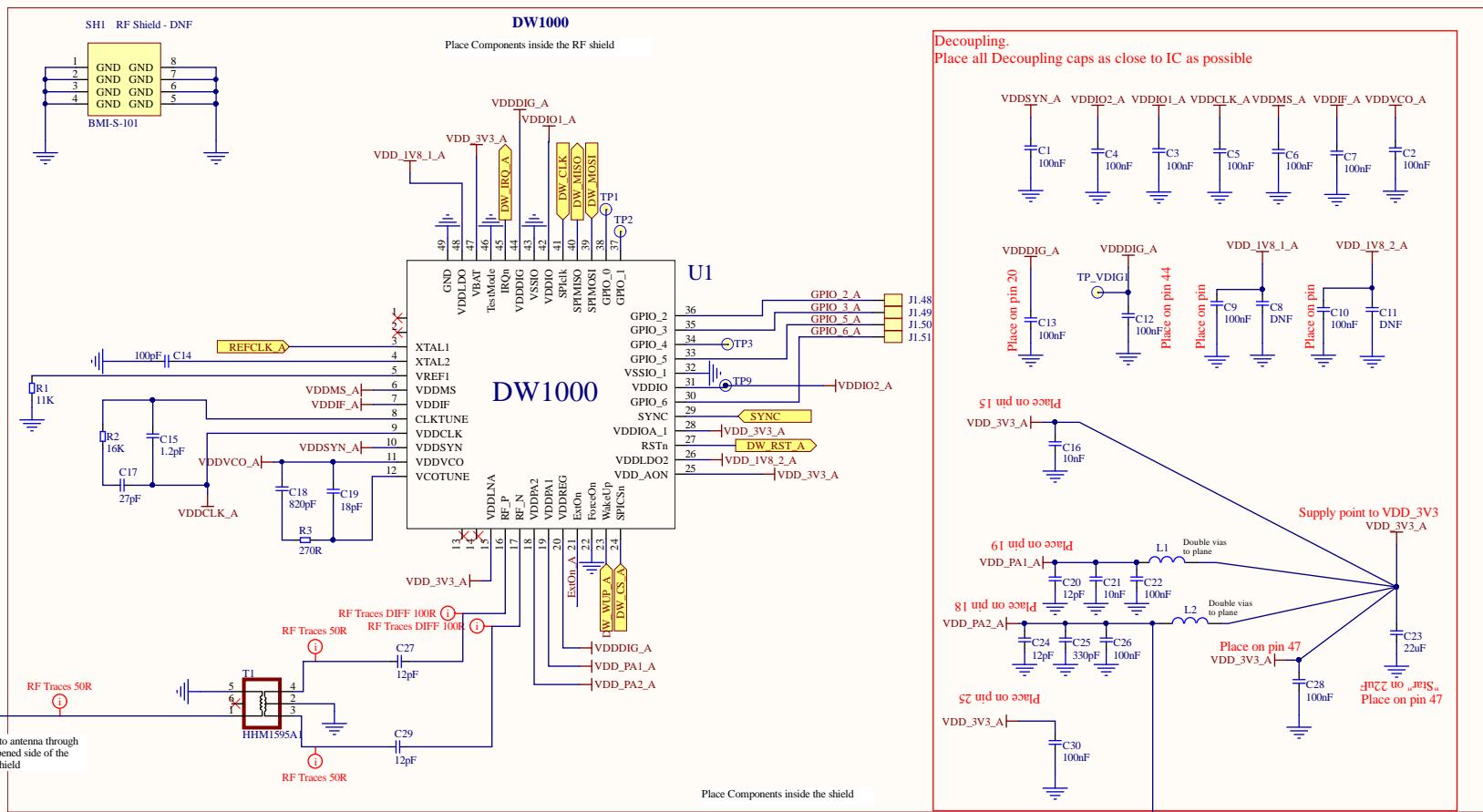


Castellation		
J1.1	GND	GND
SWDIO	GPIO_6_A	J1.52
SWDCLK	GPIO_5_A	
LEDA	GPIO_3_A	
LEDB	GPIO_2_A	
LEDC	GND	
LEDD	GPIO_6_B	
NFC1	GPIO_5_B	
NFC2	GPIO_3_B	
P1.11	GPIO_2_B	
P1.12	P0.24	
P0.03	DW_IRQ_A	
P0.02	P0.15	
GND	GND	
I2C_SCL	IRQ2	
I2C_SDA	P0.18	
P0.30	IRQ_DRDY	
P0.31	BAR_SDO	
P0.26	BAR_CS	
P0.27	GND	
P0.04	D+	
P0.05	D-	
VCC	VCC_USB	
GND	MAG_CS	
P0.06	ACC_CS	
J1.27	P0.07	ACC_SDO J1.28
Castellated pitch : 1.0mm		

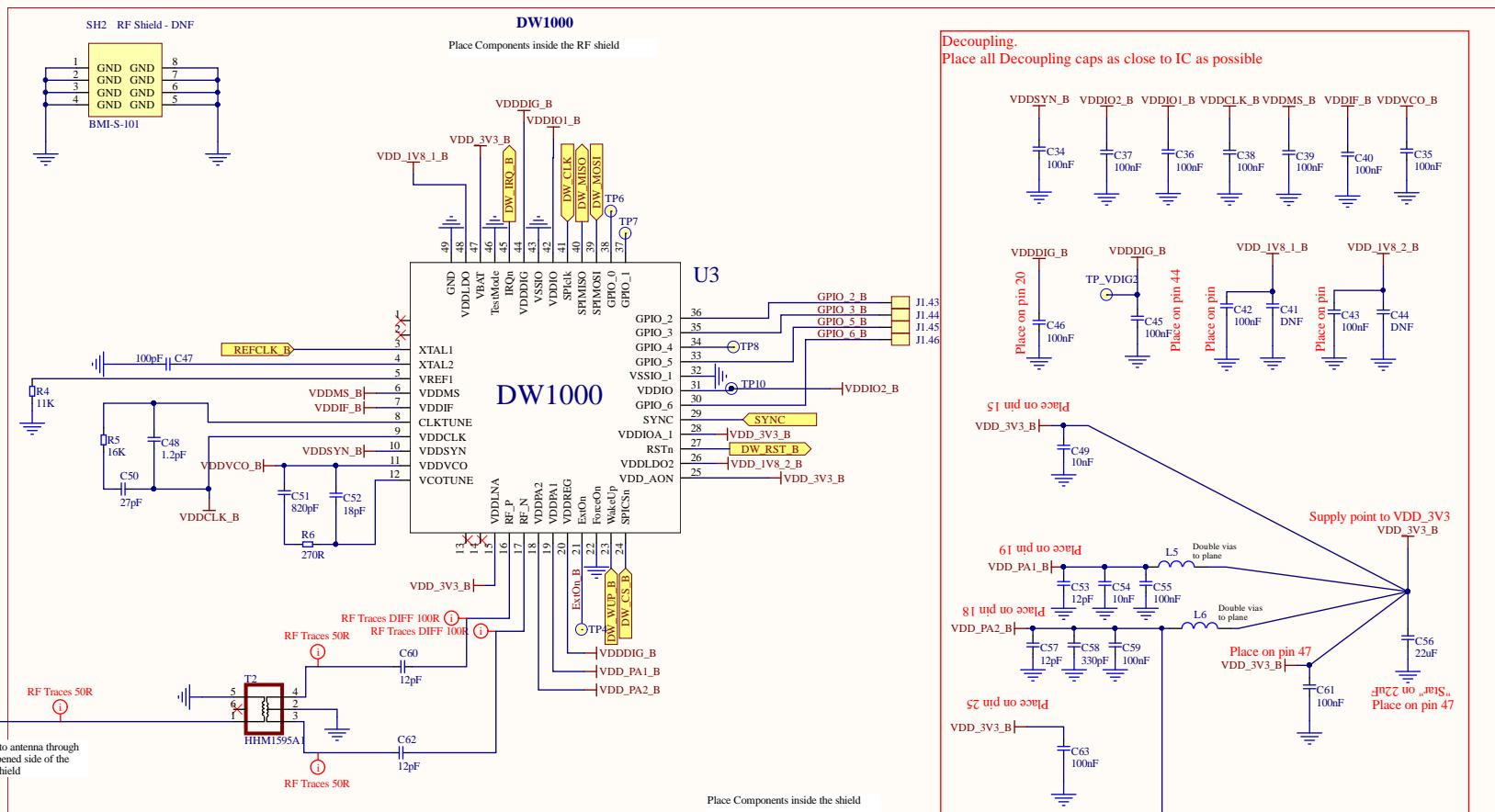






This can be placed outside the shield

Title:	PDOA Kit Node		
Function:	DW1002 A	DecaWave Ltd, Adelaide Chambers, Peter Street, Dublin 8, Ireland.	 Decawave
Size:	A3	Number:	3
Revision:	2v2	Date:	27/08/2019
Time:	17:25:40	Sheet:	3 of 5



This can be placed outside the shield

Title: PDOA Kit Node	
Function: DW1000 B	<i>DecaWave Ltd, Adelaide Chambers, Peter Street, Dublin 8, Ireland.</i>
Size: A3	Number: 4 Revision: 2v2
Date: 27/08/2019	Time: 17:25:41 Sheet 4 of 5
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1

2

3

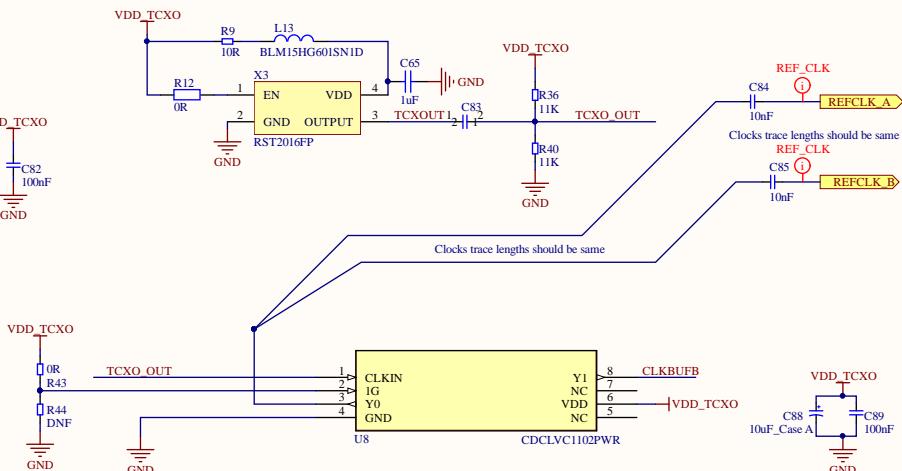
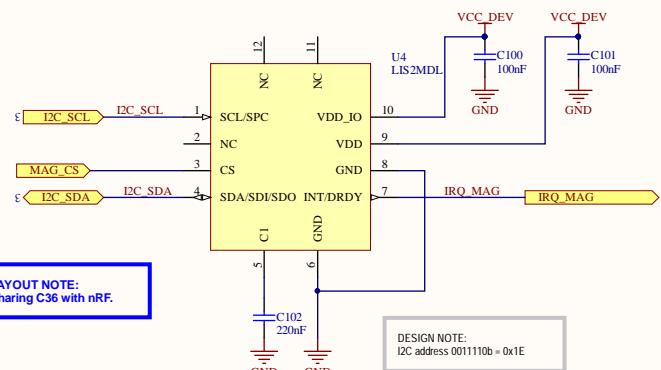
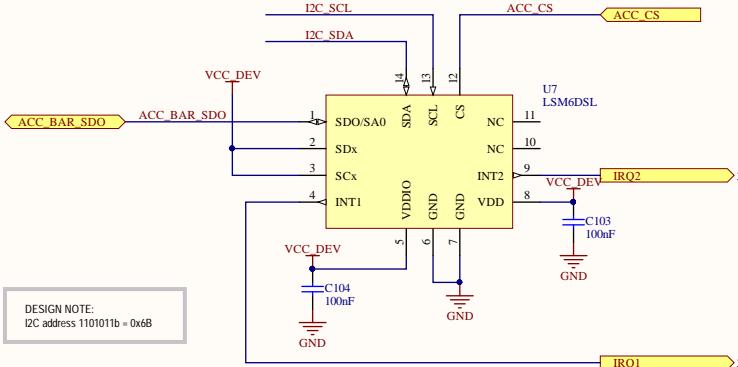
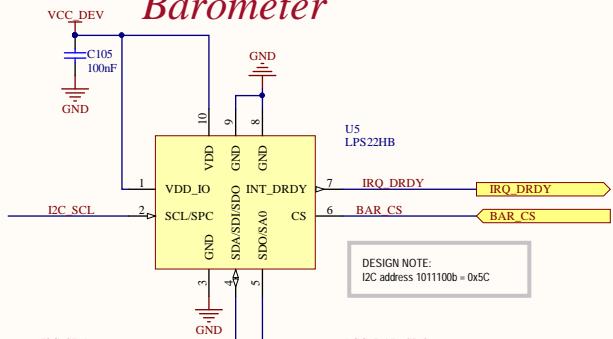
4

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8

CLOCK GENERATION**3-Axes Magnetometer****6-Axes Accelerometer and Gyroscope****Barometer****Title: PDOA Kit Node**

Function: Miscellaneous

Size: A3 Number:5

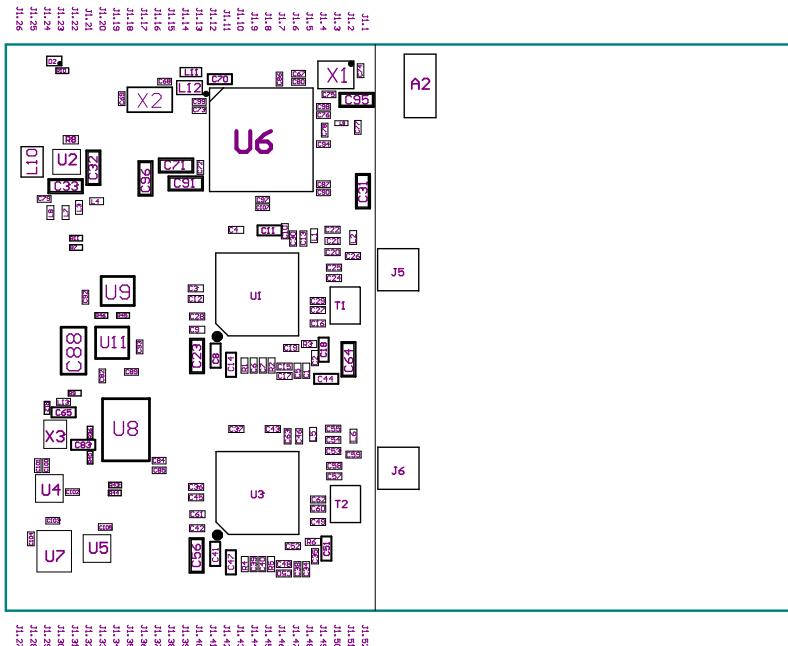
Date: 27/08/2019 Time: 17:25:41

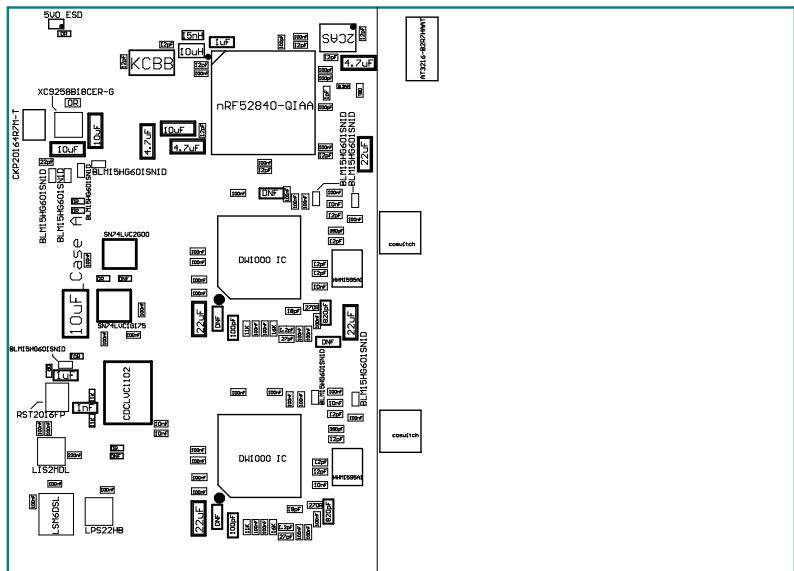
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Adelaide Chambers,
Peter Street,
Dublin 8,
Ireland.

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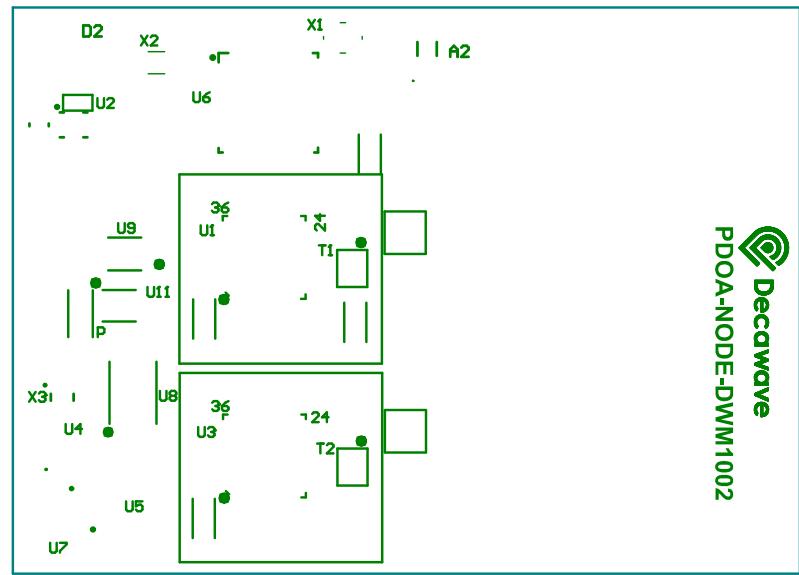
**TOP DESIGNATOR
TOP ASSEMBLY**





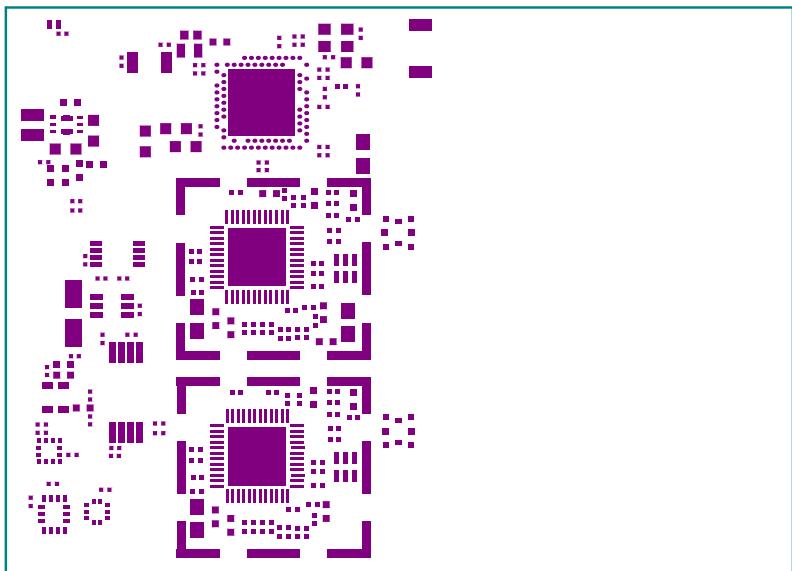
27/08/2019

TOP COMMENT
TOP ASSEMBLY



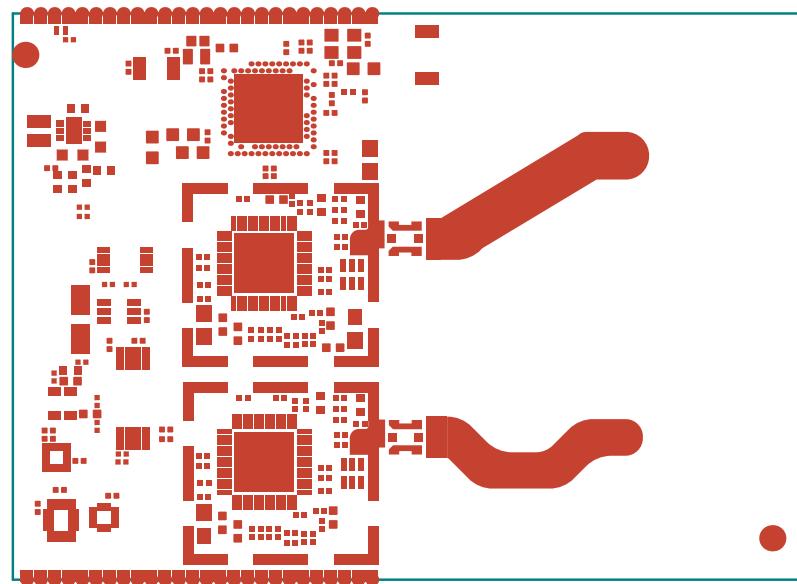
 Decawave
PDOA-NODE-DWM1002

27/08/2019



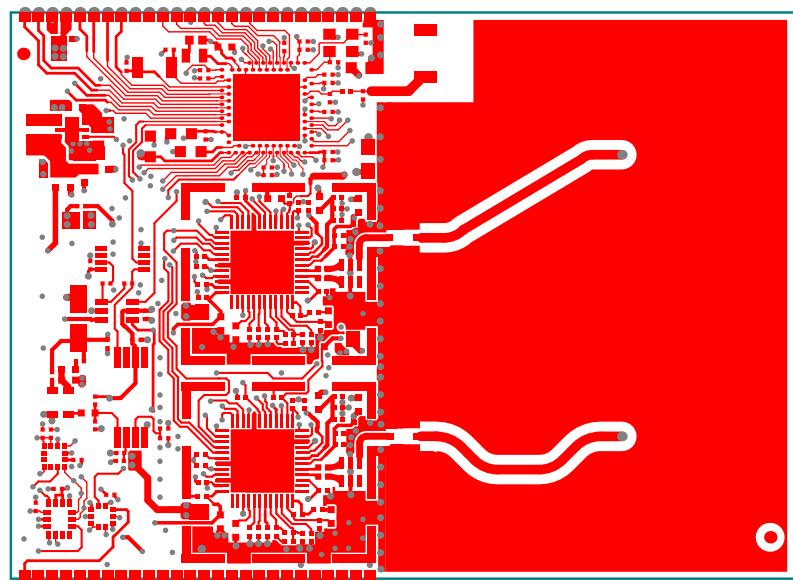
27/08/2019

SOLDERPASTE TOP



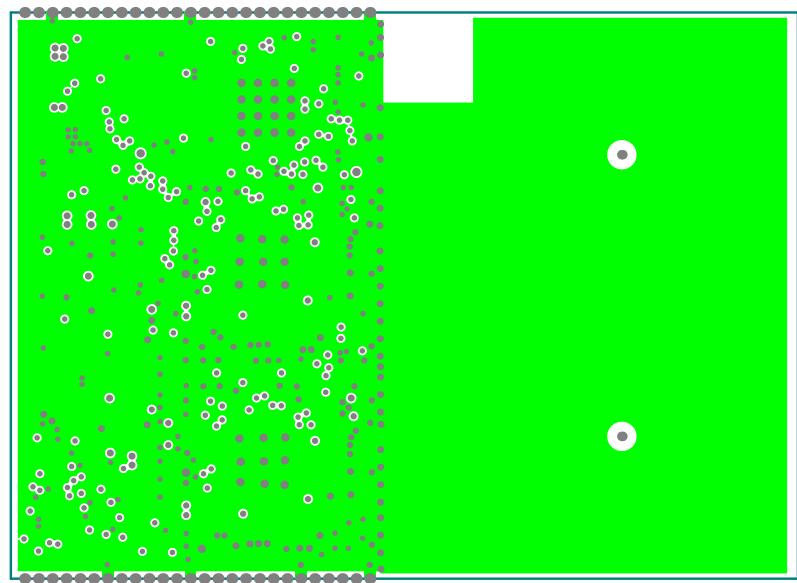
27/08/2019

TOP MASK



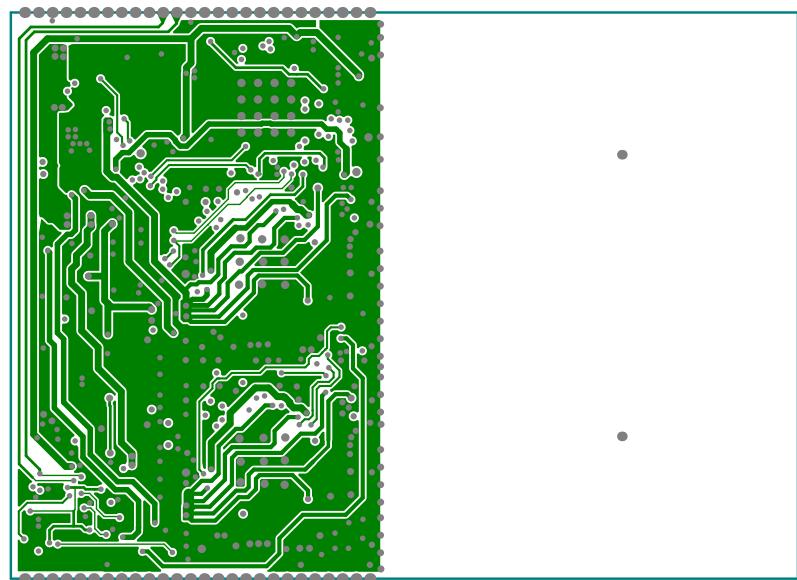
27/08/2019

LAYER-01_TOP



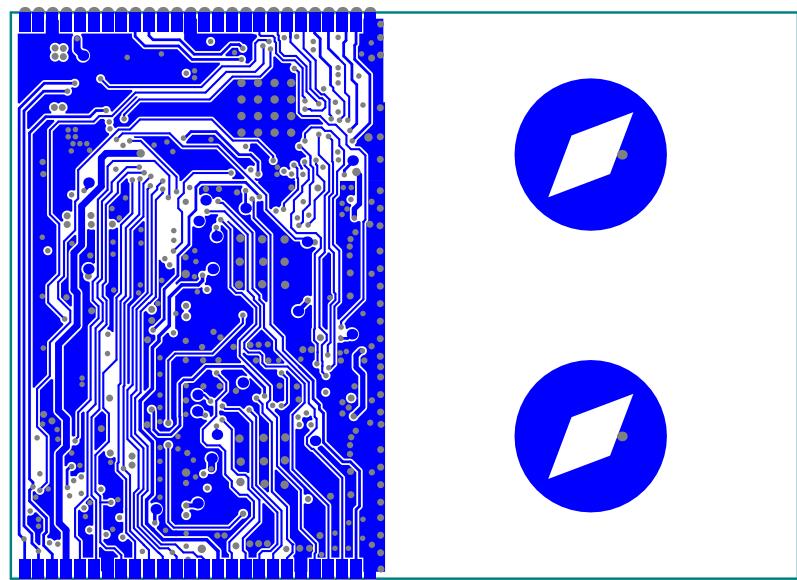
27/08/2019

LAYER-02_GROUND PLANE



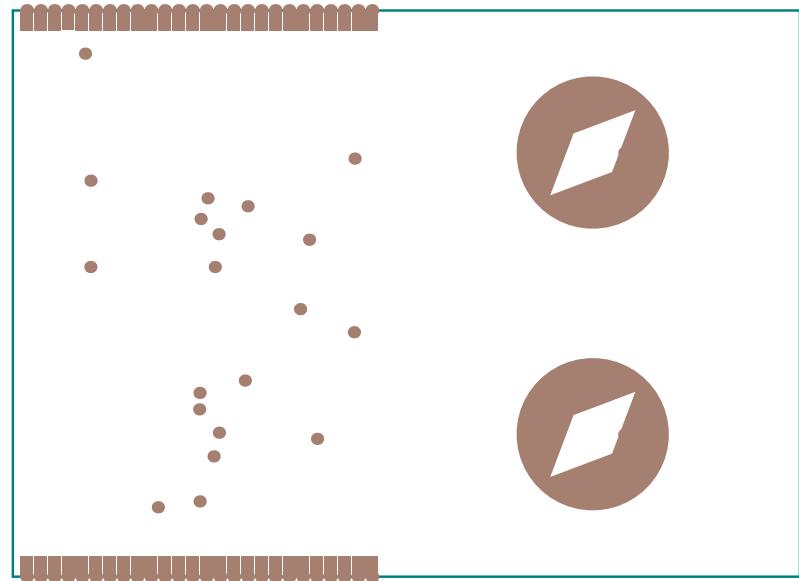
27/08/2019

LAYER-03_POWER/SIG



27/08/2019

LAYER-04_BOTTOM

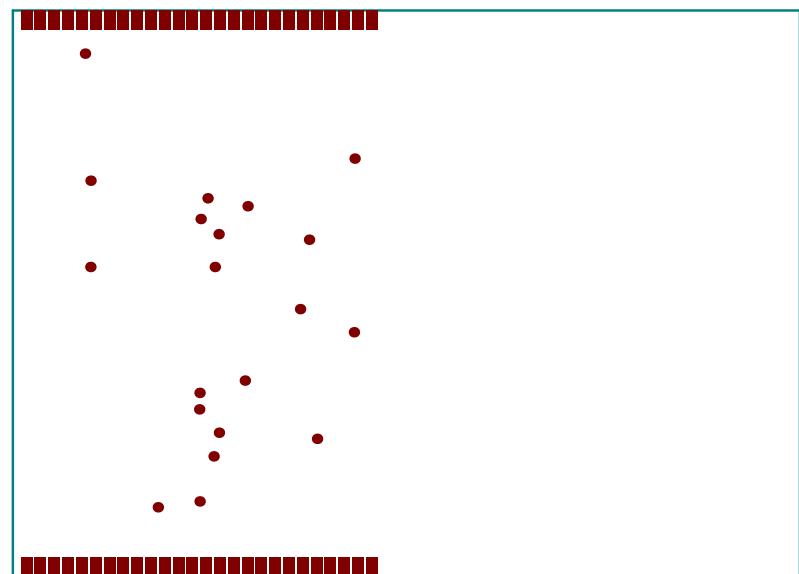


27/08/2019

BOTTOM MASK

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27/08/2019

SOLDERPASTE BOTTOM

150

27/08/2019

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Hole Length
+	261	7.87mil (0.200mm)	PTH	Round	TOP LAYER - BOTTOM LAYER	Via	-
X	143	10.00mil (0.254mm)	PTH	Round	TOP LAYER - BOTTOM LAYER	Via	-
X	40	12.00mil (0.305mm)	PTH	Round	TOP LAYER - BOTTOM LAYER	Via	-
□	52	19.69mil (0.500mm)	PTH	Round	TOP LAYER - BOTTOM LAYER	Pad	-
▽	2	20.00mil (0.508mm)	PTH	Round	TOP LAYER - BOTTOM LAYER	Pad	-
498 Total							

Via specifications

Layer specifications

TOP_LAYER	Positive layer
L02_GND	Positive layer
L03_PHR/SIG	Positive layer
L04_BOTTOM	Positive layer

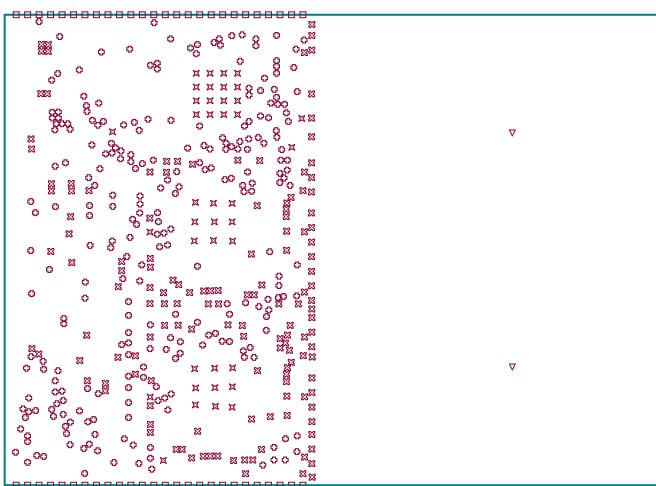


THROUGH HOLE VIA: 10/10 Mil's

DESIGN FEATURES:
MINIMUM CONDUCTOR WIDTH 6 MILS
MINIMUM AIRCAMP 5 MILS

IMPEDANCE SPECIFICATION REFER STACKUP PDF
PCB MATERIAL AND STACKUP REFER AOA-KIT-NODE_STACKP.PDF

DESIGN HAS CASTELLATIONS (HALF HOLE EDGE PLATING)
Impedance control board, test coupon to be provided along with PCB



27/08/2019