

BeeBoard

PMC

SwarmUS

Revision 1.000

Date : 2021-03-18

TOP
BEE_BOARD_TOP.SchDoc



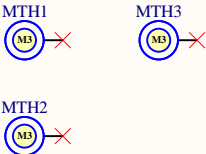
TOP
BEE_BOARD_BLOCK_DIAG.SchDoc



The following components were changed:

BSS138LT1G → BVSS138LT1G

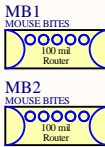
Mounting holes



Fiducials



Mouse bites



Revision history

Section name

power

Power notes

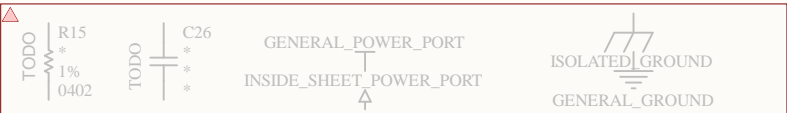
Usage notes

Questions / TODO

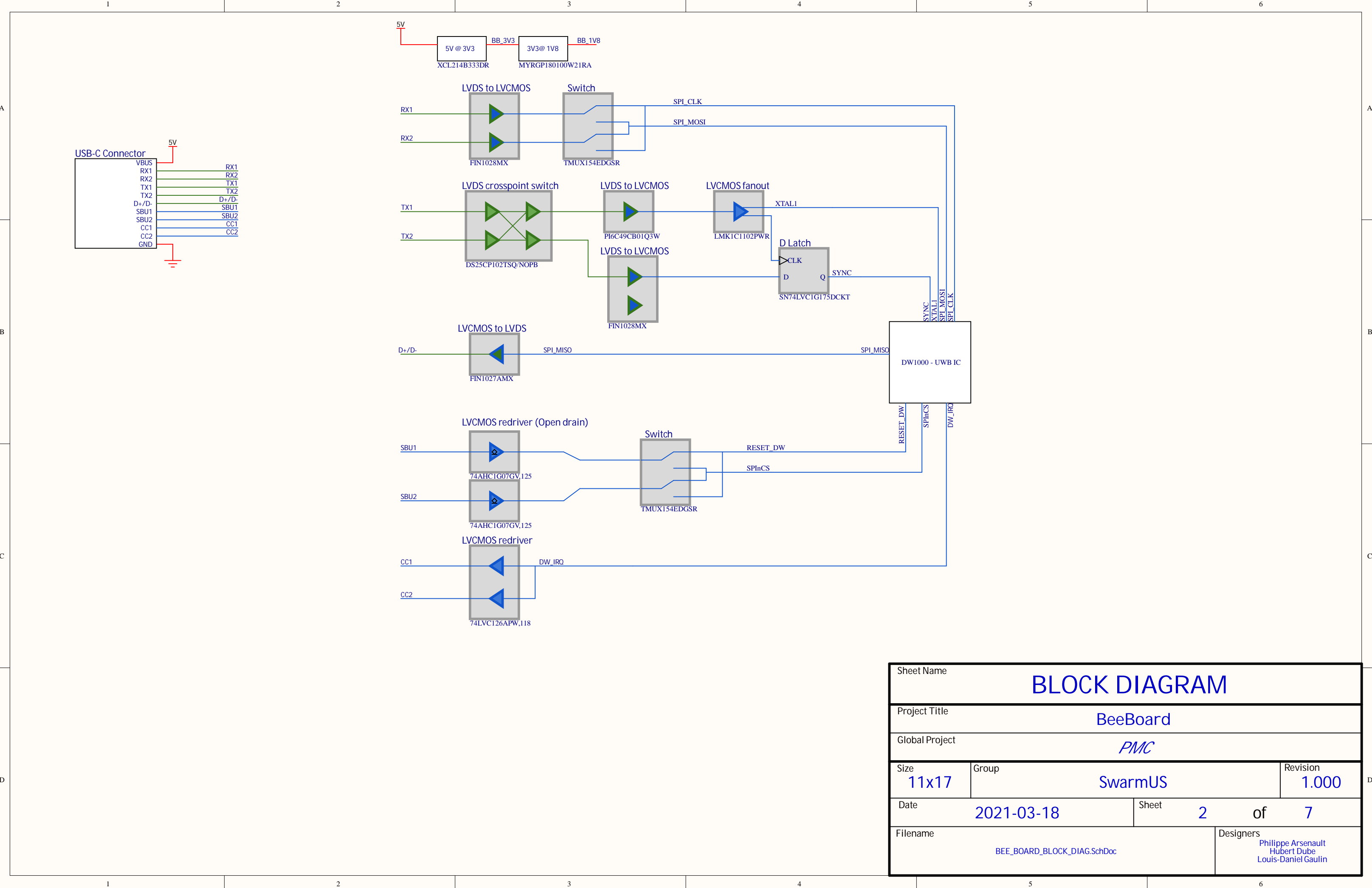
Routing notes

Package size conversion

Metric	Imperial
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

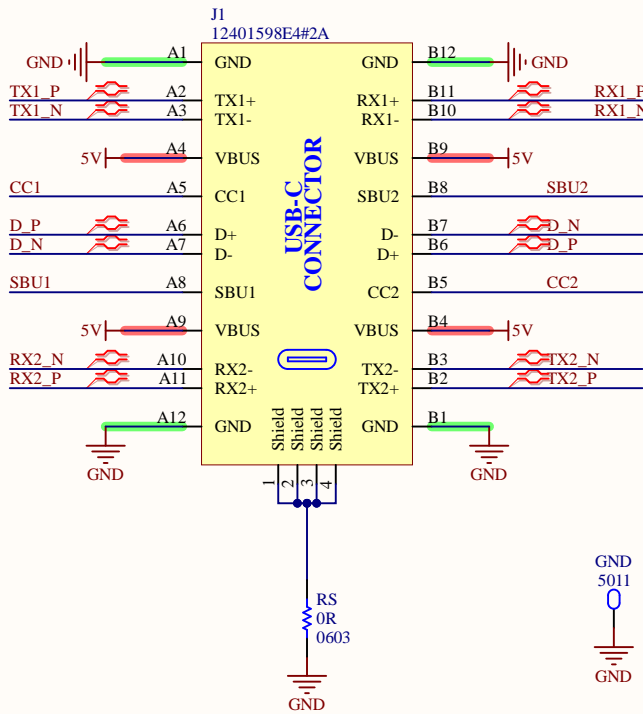


Project Title			BeeBoard		
Global Project			PMC		
Size	11x17	Group	SwarmUS	Revision	1.000
Date	2021-03-18			Sheet	1 of 7
Filename	BEE_BOARD_TITLE.SchDoc			Designers	Philippe Arsenault Hubert Dube Louis-Daniel Gaulin

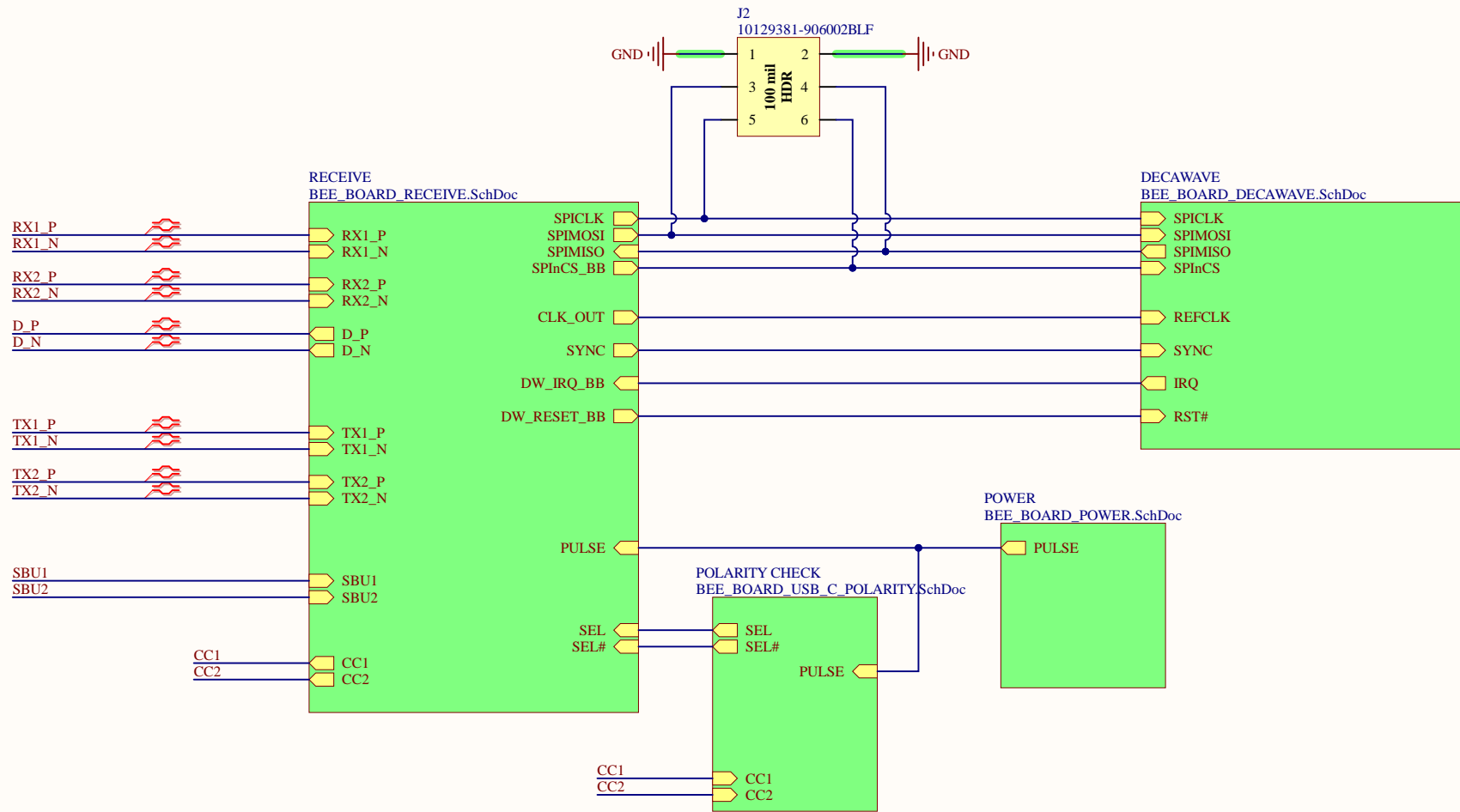


Sheet Name			BLOCK DIAGRAM		
Project Title			BeeBoard		
Global Project			PMC		
Size	Group			Revision	
11x17	SwarmUS			1.000	
Date		2021-03-18		Sheet	2 of 7
Filename				Designers	
BEE_BOARD_BLOCK_DIAG.SchDoc				Philippe Arsenaault Hubert Dube Louis-Daniel Gaulin	

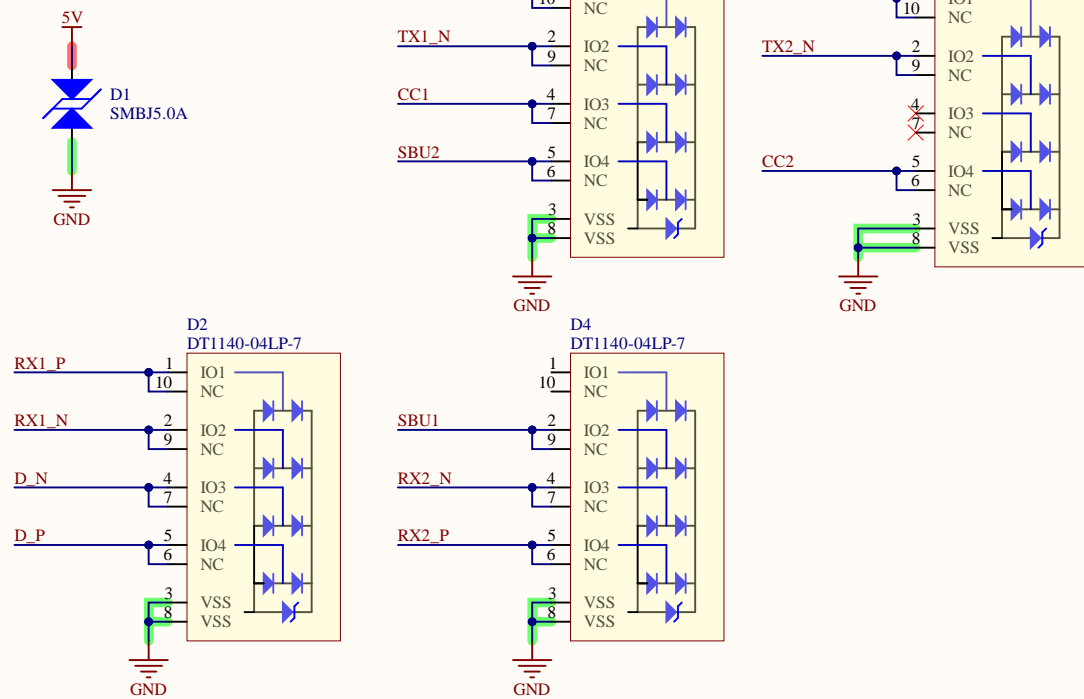
DP diff pair are 85 ohm



On flat cable (no twisting) :
RX1 : SPI CLK
RX2: SPI_MOSI
TX1 : CLK_38.4MHz
TX2 : SYNC
D+/D- : MISO
SBU1 : DW_RESET
SBU2 : SPI_nCS
CC1 : outputs IRQ
CC2 : NC



TVS Protection



Sheet Name			Top		
Project Title			BeeBoard		
Global Project			PMC		
Size	11x17	Group	SwarmUS	Revision	1.000
Date	2021-03-18			Sheet	3 of 7
Filename	BEE_BOARD_TOP.SchDoc			Designers	Philippe Arsenault Hubert Dube Louis-Daniel Gaulin

3V3 Generation

The diagram illustrates a 3V3 voltage regulation circuit. The input is a 5V rail, which is connected to the VIN pin (pin 1) of the XCL214B333DR converter (U1). A 402R resistor (R1) and a 22uF capacitor (C1) are connected between the 5V input and ground. A 4.7uF capacitor (C3) is connected between the 5V input and ground. A 100k resistor (R43) is connected between the VIN pin and the CE pin (pin 6). The CE pin is also connected to ground. The PGND (pin 7) and AGND (pin 5) pins are connected to ground. The VOUT pin (pin 4) is connected to the L2 pin (pin 9). The L2 pin is connected to the Lx pin (pin 3) and the L1 pin (pin 8). The Lx pin is connected to ground. The L1 pin is connected to ground. The NC pin (pin 2) is connected to ground. The output of the converter is connected to a 3V3 rail, which is connected to a 475R resistor (R2) and a 10uF capacitor (C5). The 3V3 rail is also connected to a 3V3 output terminal. A diode (D7) is connected between the 3V3 rail and ground.

380mA@5V
MAX

EFFICENCY = 90%+ @250mA

517mA@3V3
MAX

PCB Note:
Routing must be
carefully done following
P.11 of the datasheet

1V8 Generation

The diagram shows a buck converter circuit for generating 1V8 from a 3V3 input. The input is connected to the VIN pin (pin 6) of the U3 converter (MYRGP180100W21RA). A 4.7uF 25V capacitor (C7) is connected between VIN and GND. The CE pin (pin 4) is connected to GND. The AGND and PGND pins (pins 2 and 3) are connected to GND. The VOUT pin (pin 3) is connected to the L2 pin (pin 8). The Lx pin (pin 1) is connected to the L1 pin (pin 7). The EPAD pin (pin 9) is connected to GND. The output of the converter is connected to a 10uF 16V capacitor (C8) and a 10k resistor (R3) in parallel, which is then connected to the gate of a MOSFET (Q1, BSS138LT1G). The MOSFET's source is connected to GND and its drain is connected to the 1V8 output. A 1M resistor (R4) is connected between the 3V3 input and the 1V8 output. A diode (D8, SML-D12P8WT86) is connected in parallel with the MOSFET's drain and source. The 1V8 output is also connected to a 1M resistor (R4) and a 475R resistor (R4) in series, which is then connected to the 3V3 input.

138mA@3V3
MAX

EFFICENCY = 90%+ @180mA

228mA@1V8
MAX

Close to DW

Pulse generator

435171014816

S1

3V3

R40 100k 1% 0402

C2 1uF 10V 0603

GND

C4 1uF 10V 0603

GND

U2 TPS3808G33DRVR

1 VDD

2 SENSE

3 CT

4 MR

5 GND

6 RESET

7 EP

R42 100k 1% 0402

C6 100nF 25V 0402

GND

PULSE

Reset Logic Timer

4V ref

Design Note:

$$T(s) = \frac{CT(nf)}{175} + 0.5 \cdot 10^{-3}$$

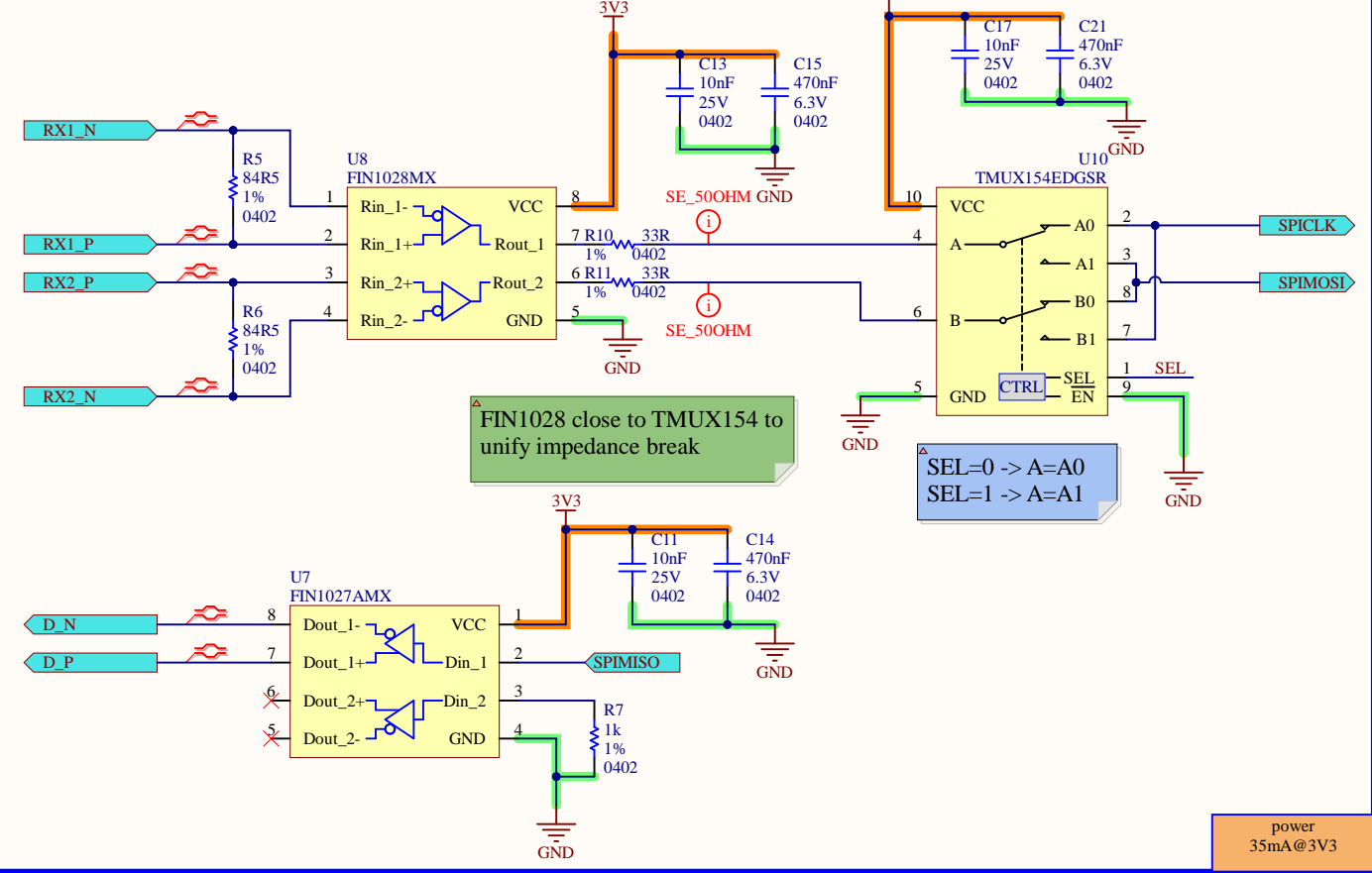
0.572s @ 100nF

5mA@3V3
MAX

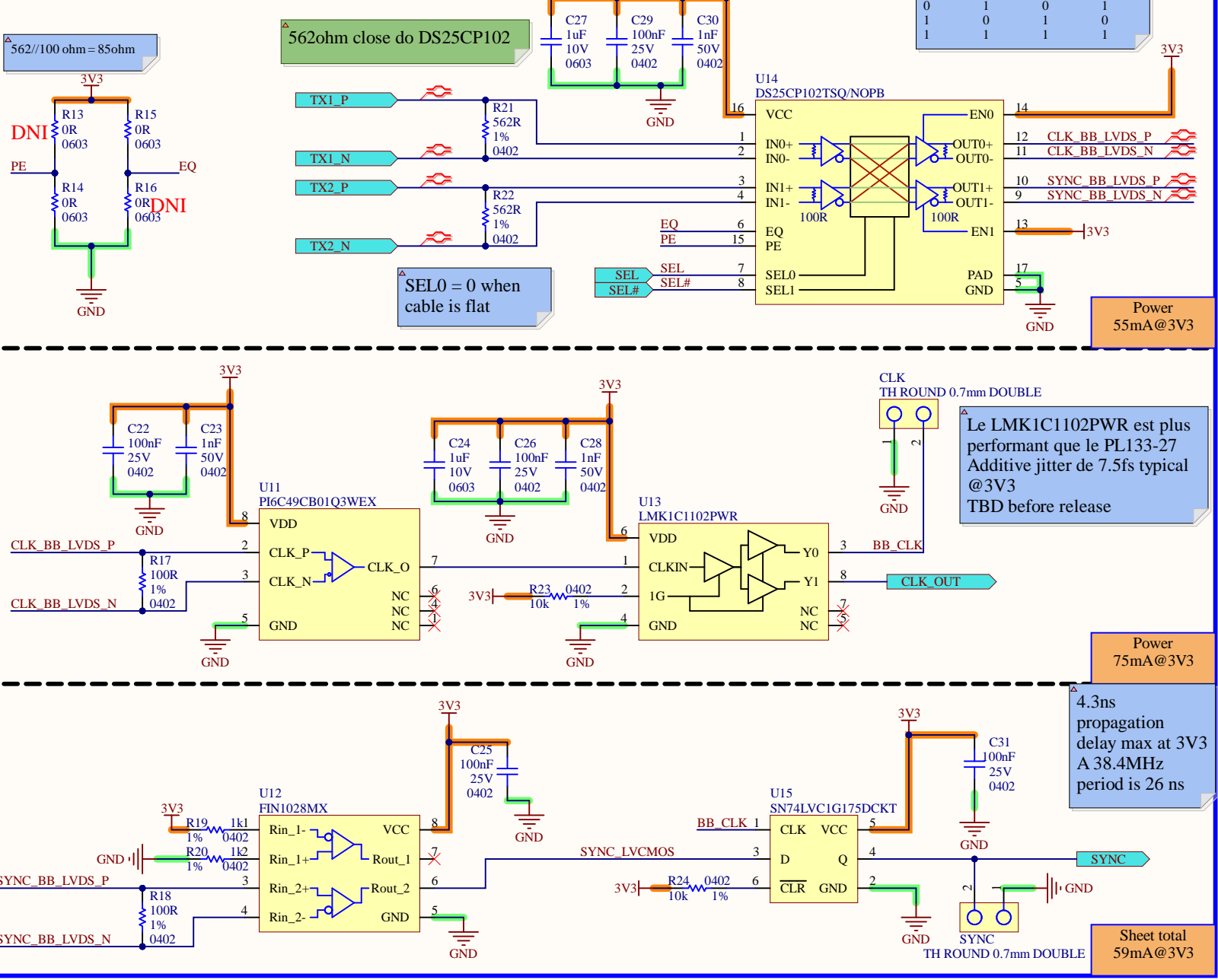
5mA@3V3
MAX

Sheet Name				POWER			
Project Title				BeeBoard			
Global Project				PMC			
Size		Group			Revision		
11x17		SwarmUS			1.000		
Date			2021-03-18		Sheet		4 of 7
Filename					Designers		
BEE_BOARD_POWER.SchDoc					Philippe Arsenault Hubert Dube Louis-Daniel Gaulin		

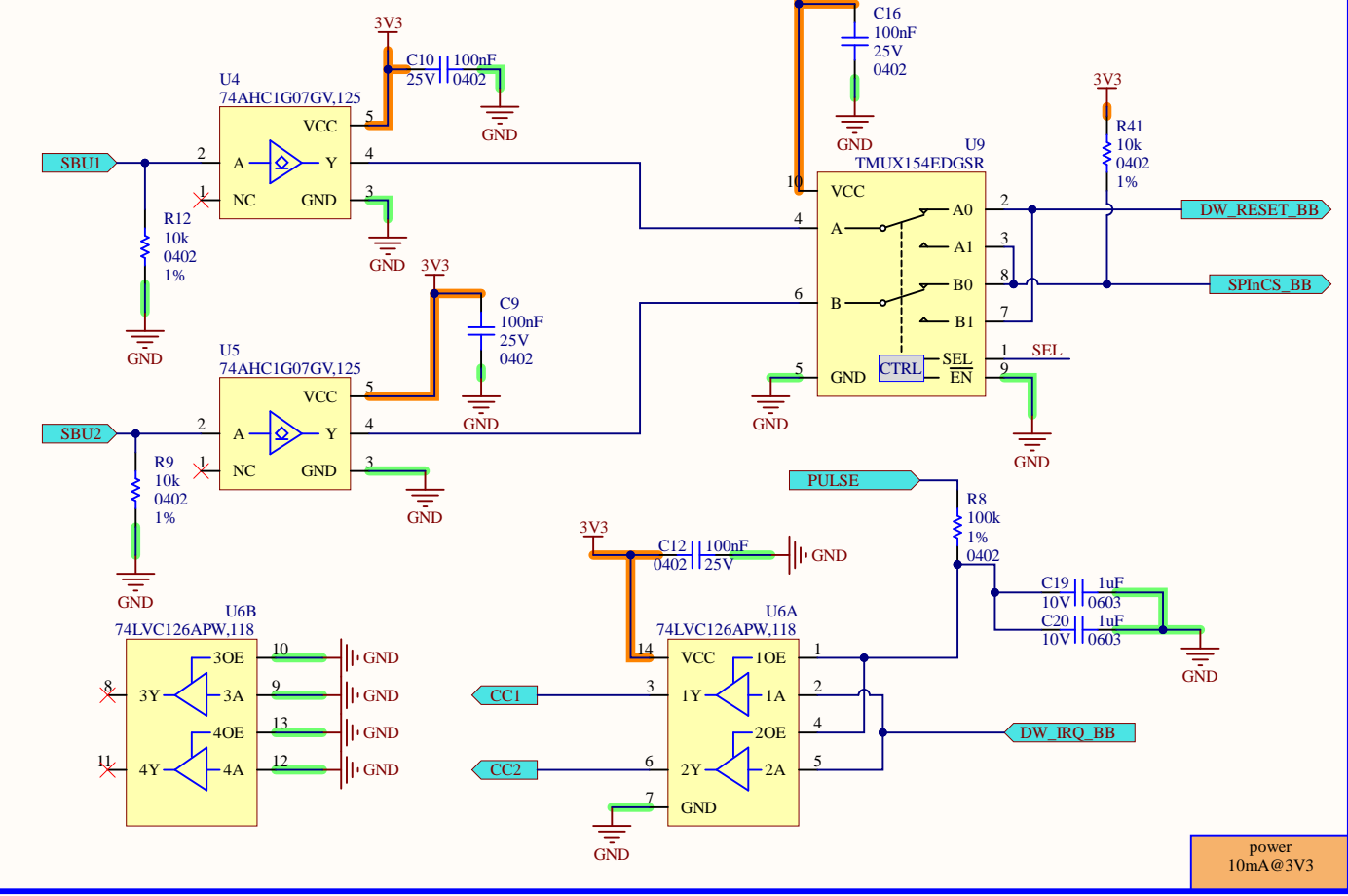
SPI LVDS/LVCMOS



38.4MHz CLK LVDS to LVCMOS & SYNC



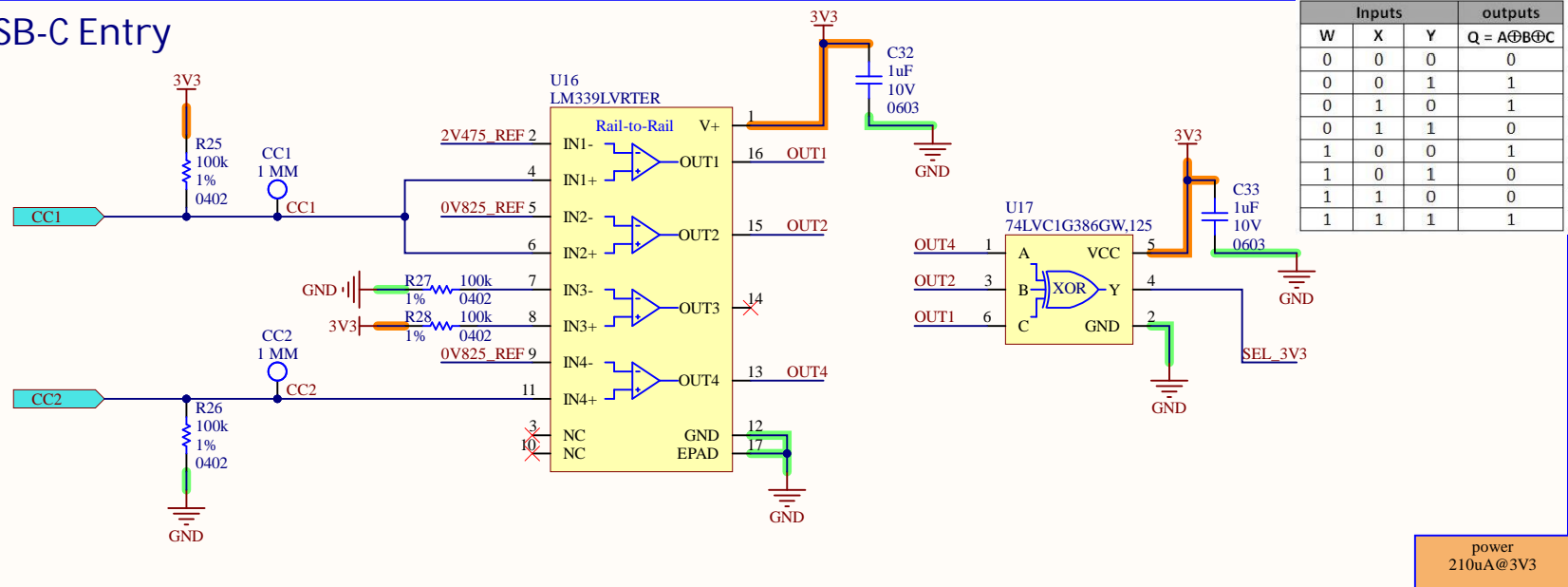
Channel 0 SE buffers



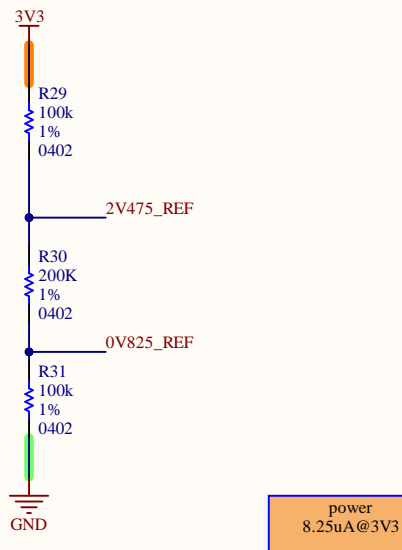
RC = 0.2
VIH is 2V
OE = 2V after DW_RESET = 3V3
for 180ms

Sheet Name		Receive modules	
Project Title		BeeBoard	
Global Project		PMC	
Size	Group	Revision	
11x17	SwarmUS	1.000	
Date	2021-03-18	Sheet	5 of 7
Filename		Designers	
BEE_BOARD_RECEIVE.SchDoc		Philippe Arsenault Hubert Dube Louis-Daniel Gaulin	

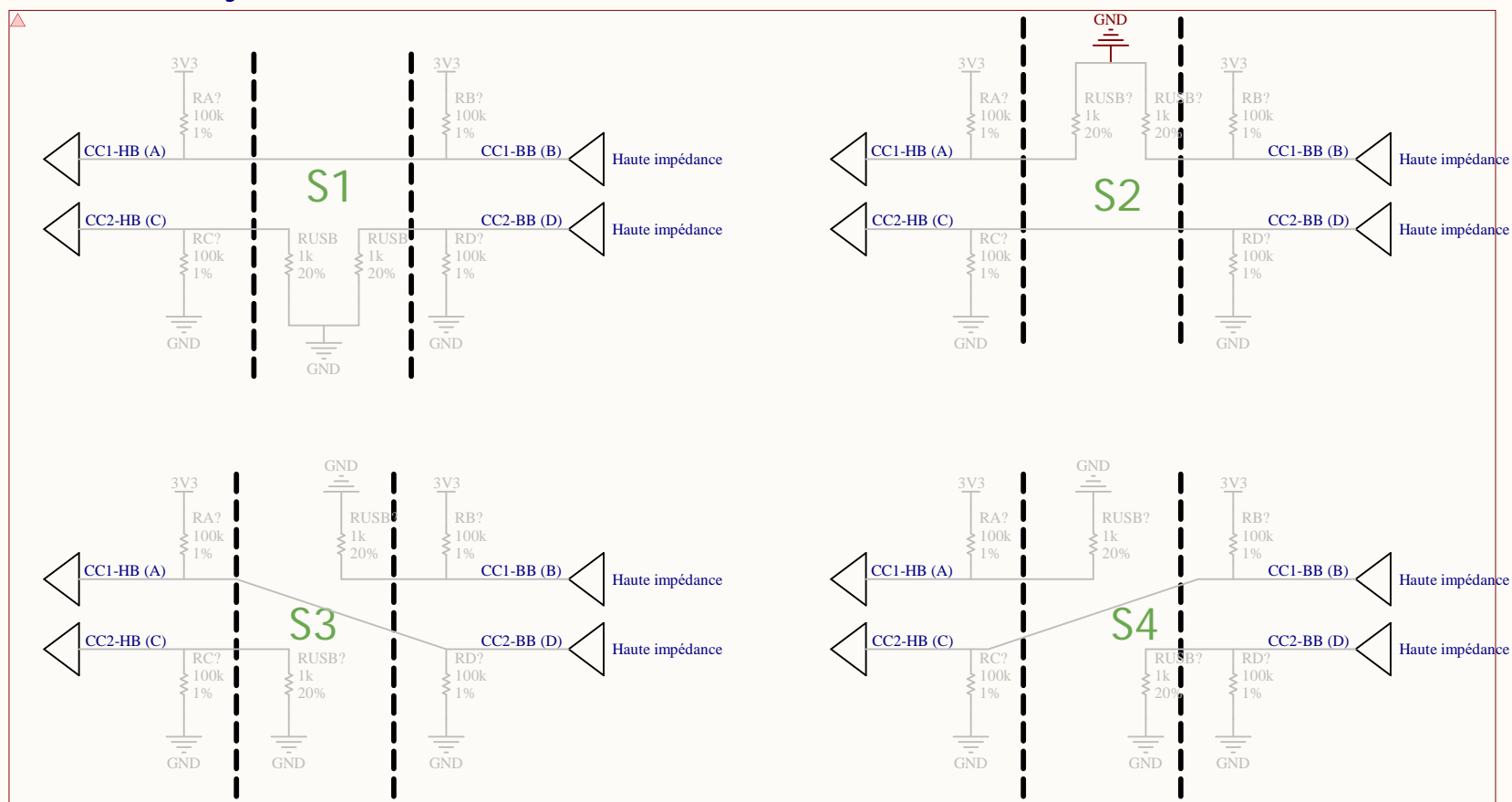
USB-C Entry



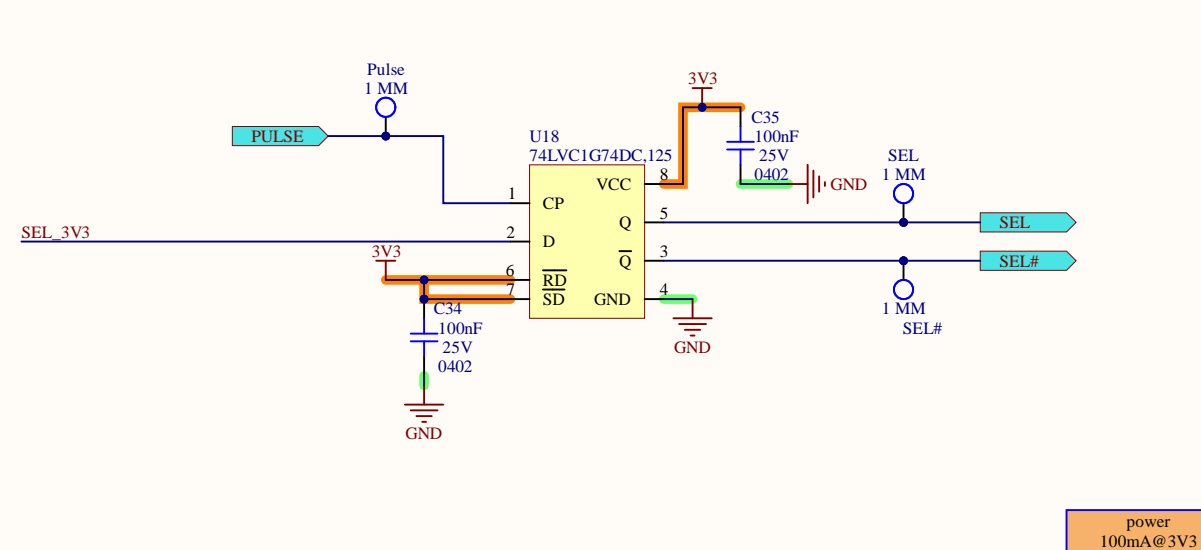
Resistor comparative



USB-C Polarity Check REFERENCE FIGURES



Selection fanout



Sheet Name

USB Polarity Check

Project Title

BeeBoard

Global Project

PMC

Size

11x17

Group

SwarmUS

Revision

1.000

Date

2021-03-18

Sheet

6

of

7

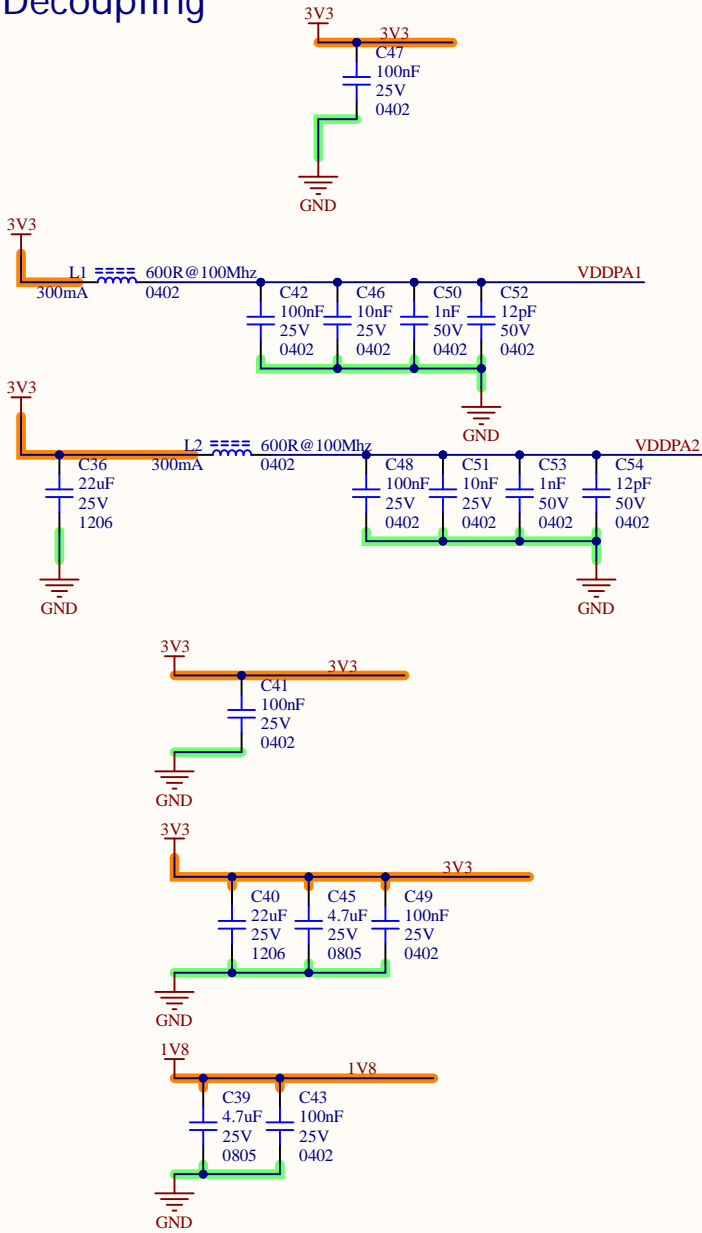
Filename

BEE_BOARD_USB_C_POLARITY.SchDoc

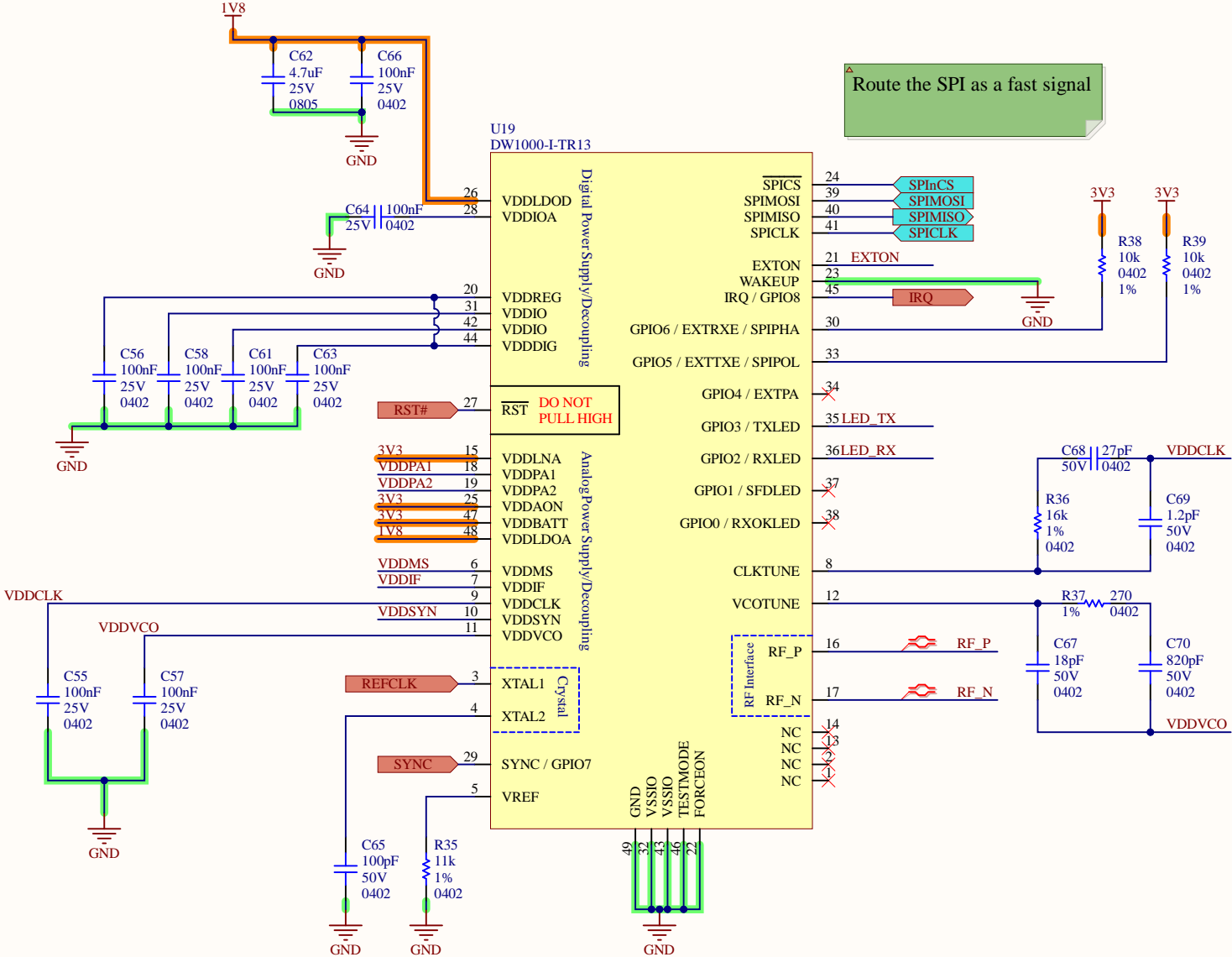
Designers

Philippe Arsenault
Hubert Dube
Louis-Daniel Gaulin

Decoupling



Decawave

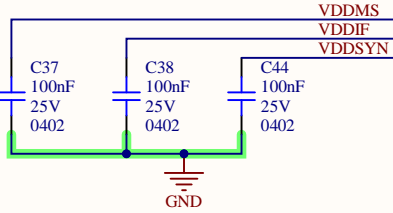


Route the SPI as a fast signal

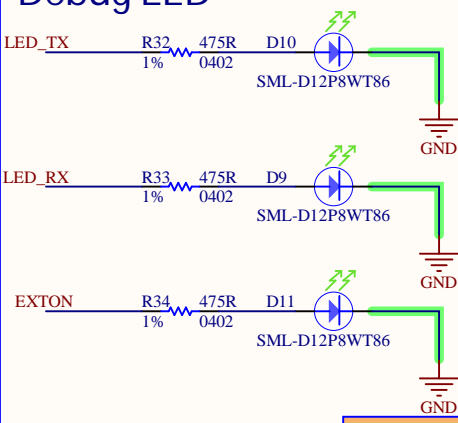
R38/R39 are there to supply a less resistance path for the 3v3 internal pull-up

power
30mA@3V3
210mA@1V8

Off-chip capacitance

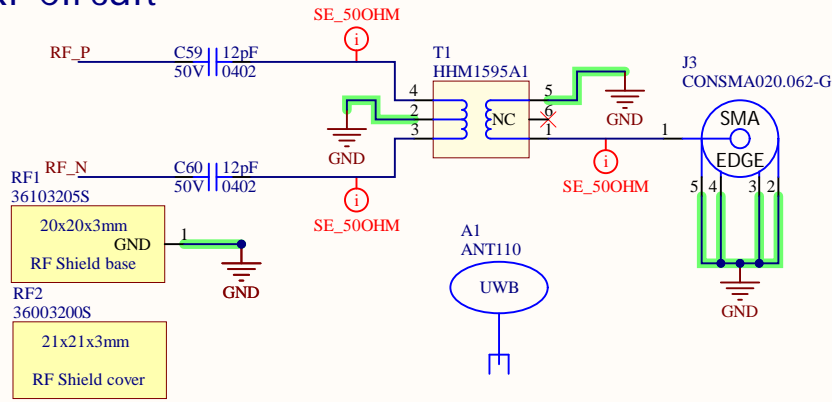


Debug LED



power
9mA@3V3

RF Circuit



Sheet Name			DECAWAVE		
Project Title			BeeBoard		
Global Project			PMC		
Size	Group			Revision	
11x17	SwarmUS			1.000	
Date		2021-03-18		Sheet	7 of 7
Filename				Designers	
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Sheet total
39mA@3V3
210mA@1V8