**SOC Design of Nand gate**

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1.Design a SOC design of Nand gate (universal gate).

Block Diagram

SW0

RTL of AND gate

AXI GPIO

ARM processor (ZYNQ processing unit)

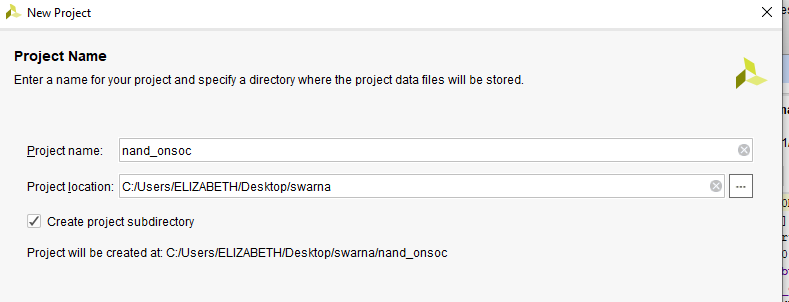
SW1

Implemented on FPGA

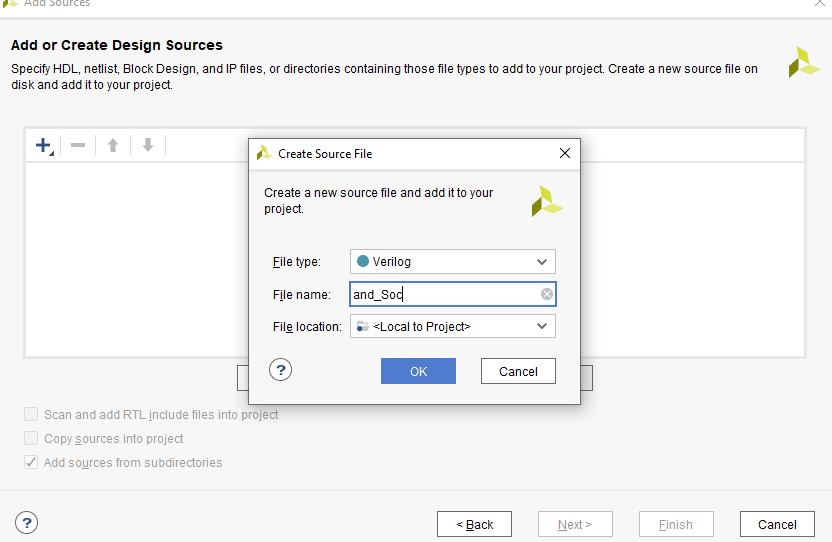
AXI GPIO

🡪Not gate implemented in software which is an ARM processor

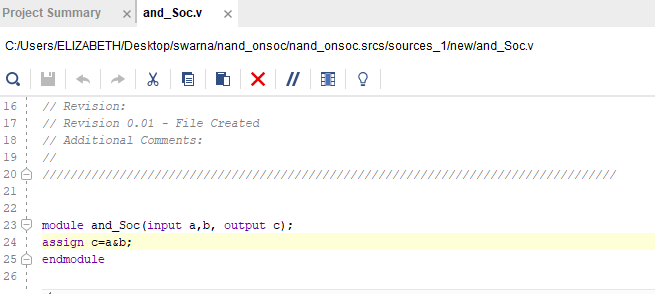
**Step-1**: Create a new project, give name of the project click ok.



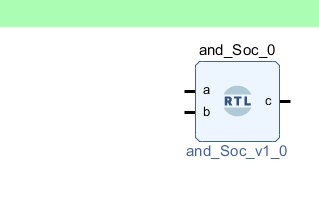
**Step-2**: Right click on design sources go to add sources, give a file name.



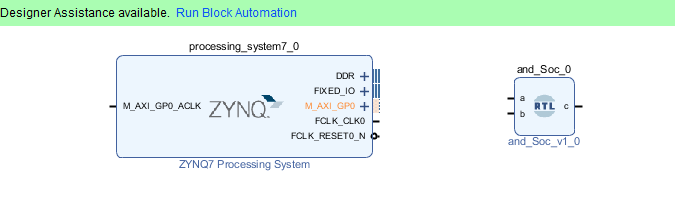
**Step-3:** write a Verilog code for “and” gate because “nand” is a not of and gate so we will design the not gate on ARM processor.



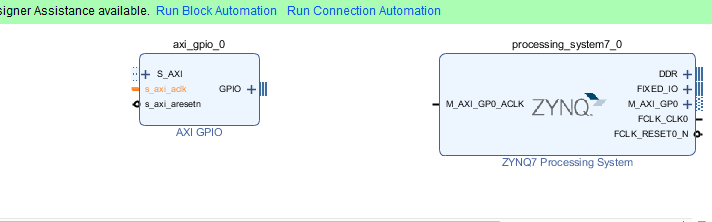
**Step-4**: save the code and in IP integrator create a block design add RTL of and gate.



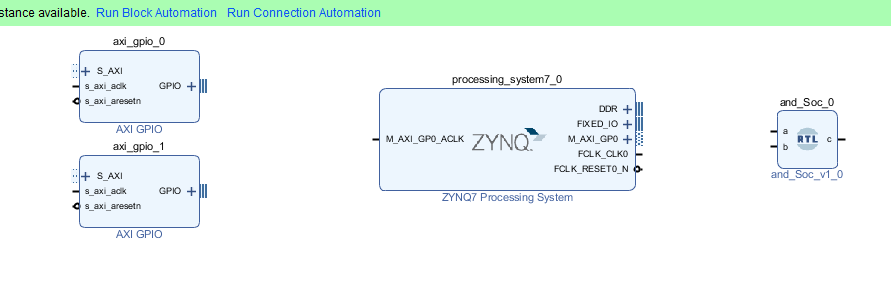
**Step-5**: Right click on workspace select Add IP, add the ZYNQ processing system.



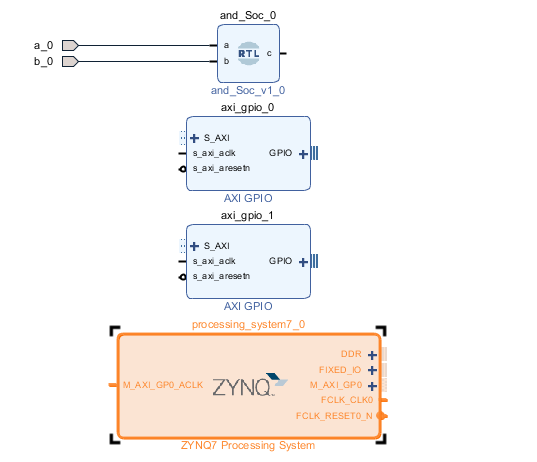
**Step-6:** Right click on workspace select Add IP, add the AXI GPIO for input purpose.



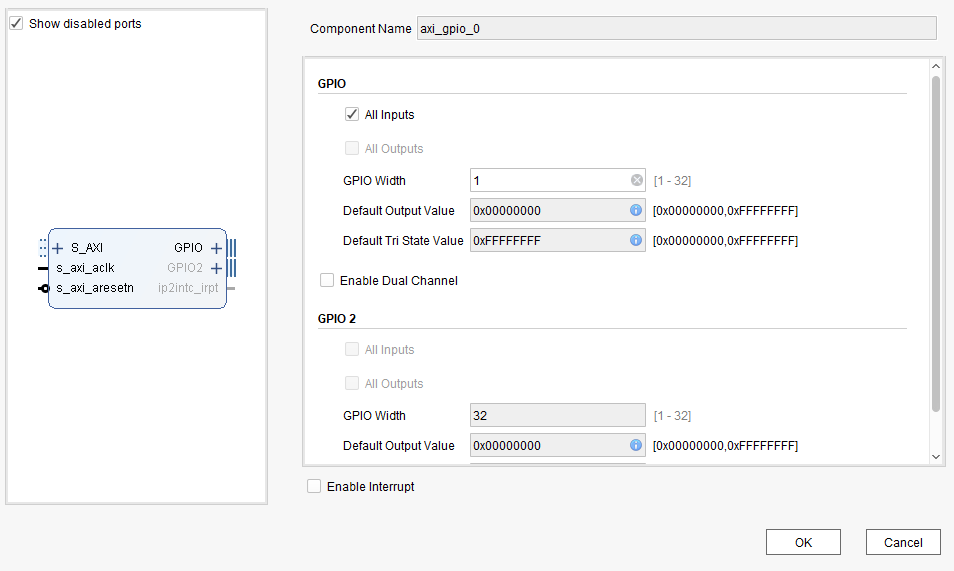
**Step-7:** Right click on workspace select Add IP, add the AXI GPIO for output purpose.



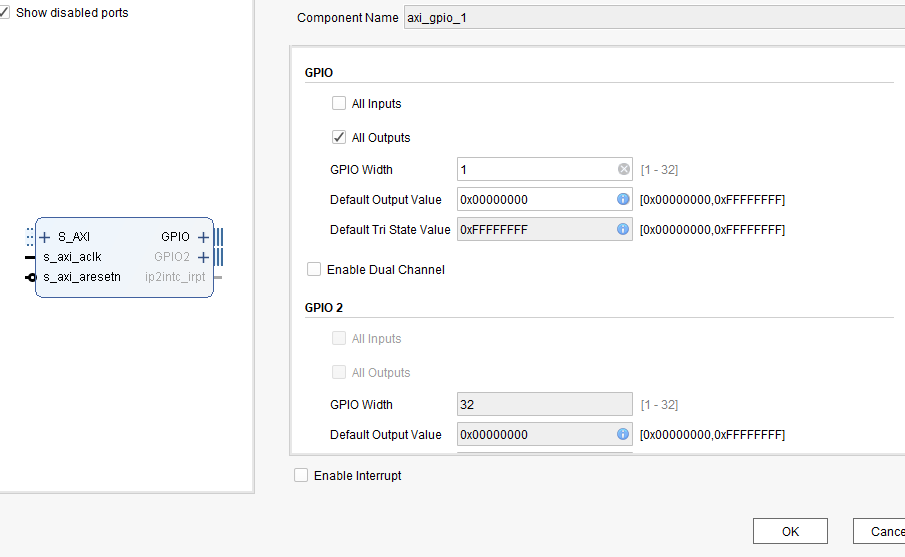
**Step-8:** Make input a and b as external.



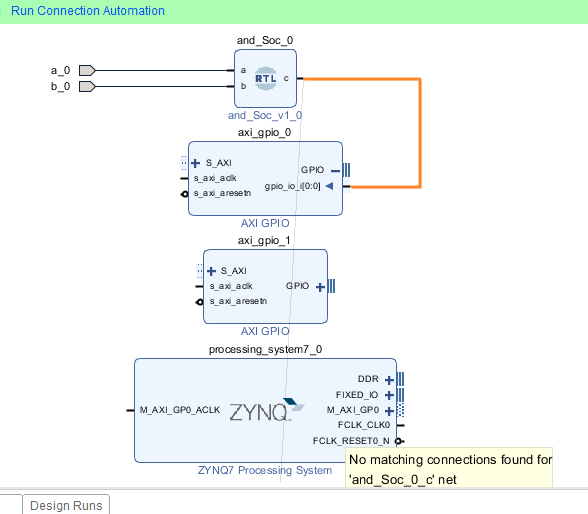
**Step-9:** Double click on AXI GPIO, select all inputs, give width =1 click ok.



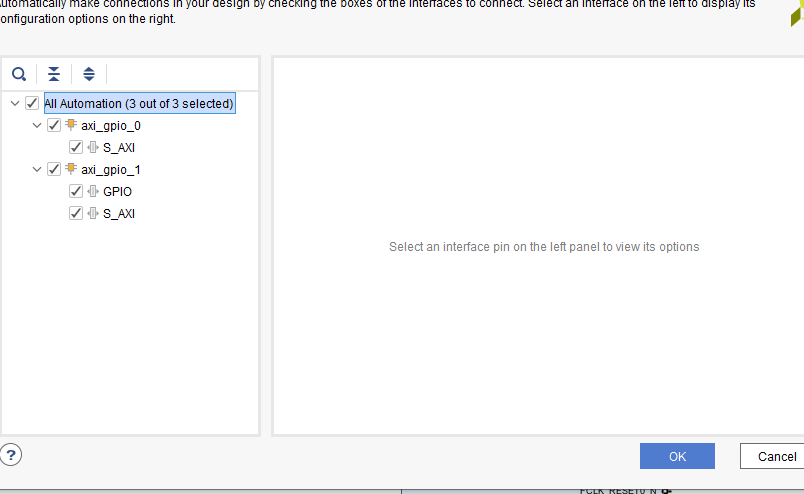
**Step-10:** Double click on second AXI GPIO, select all outputs, give width =1 click ok.



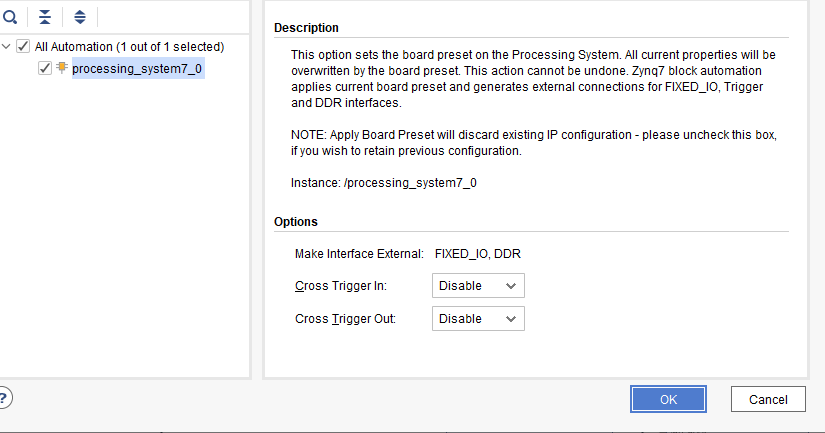
**Step-11:** Run connection automation.



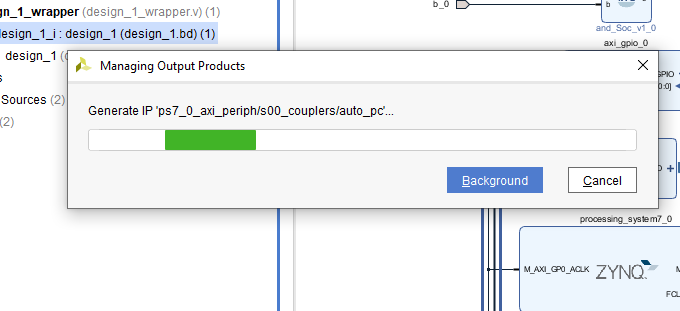
**Step-12:** select all automation click ok.



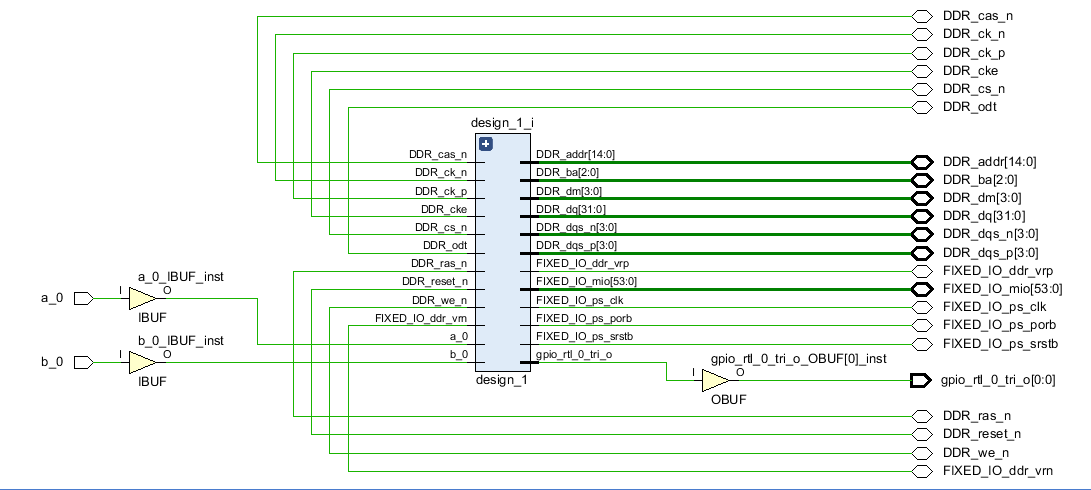
**Step-13:** Run block automation, select all automation, clock ok.



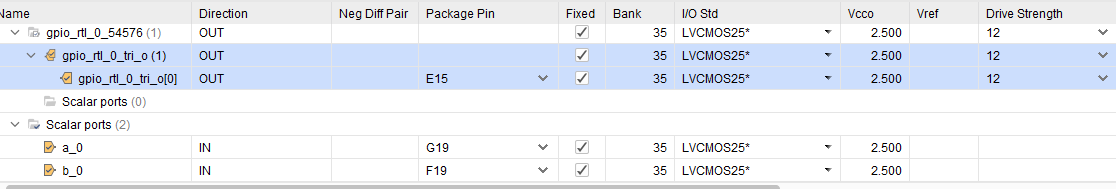
**Step-14:** validate the design, create HDL wrapper, Generate output products.



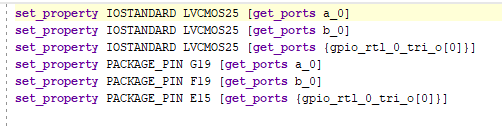
**Step-15:** Run synthesis, Run implementation, open implementation Design.



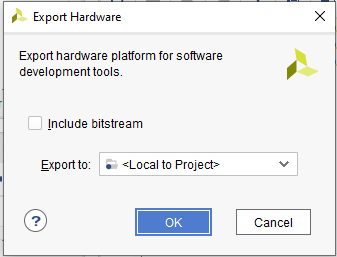
**Step-16:** Give pin planning.



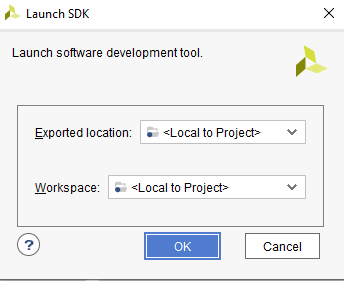
**Step-17:** Save the pin planning open constraints file then save it, generate bit stream.



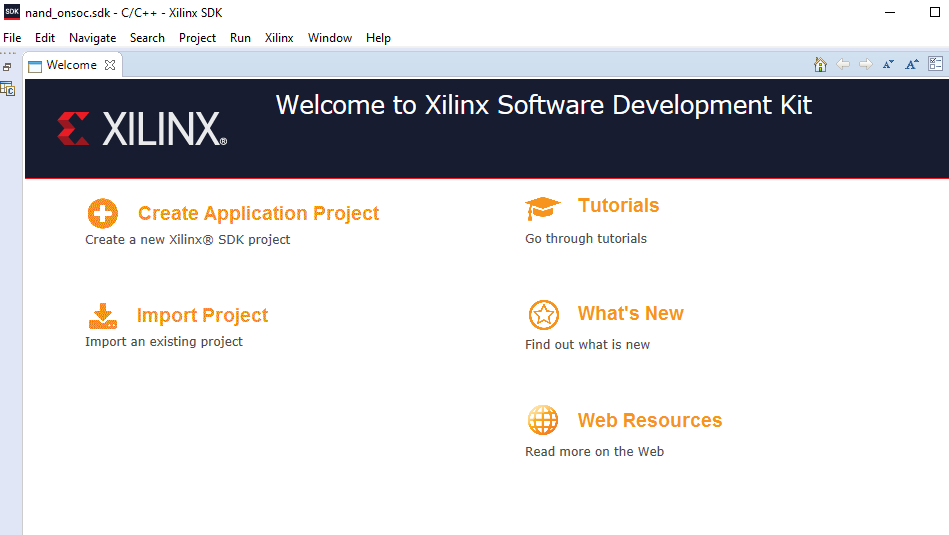
**Step-18:** Right click on file select export hardware click it ok.



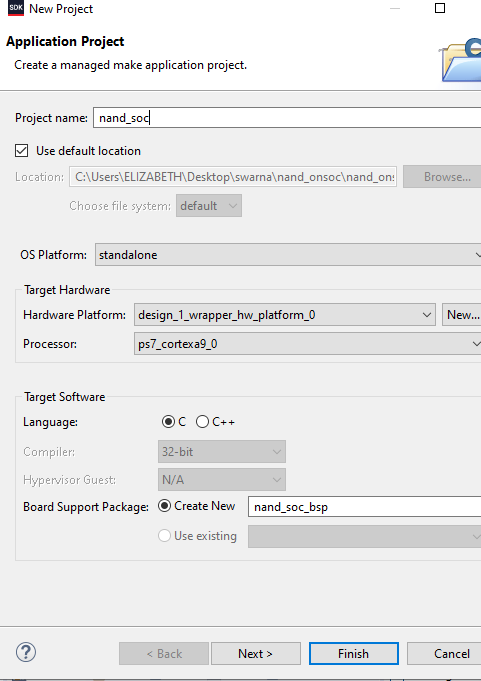
**Step-19:** Right click on file select Launch SDK give location and workspace click it ok.



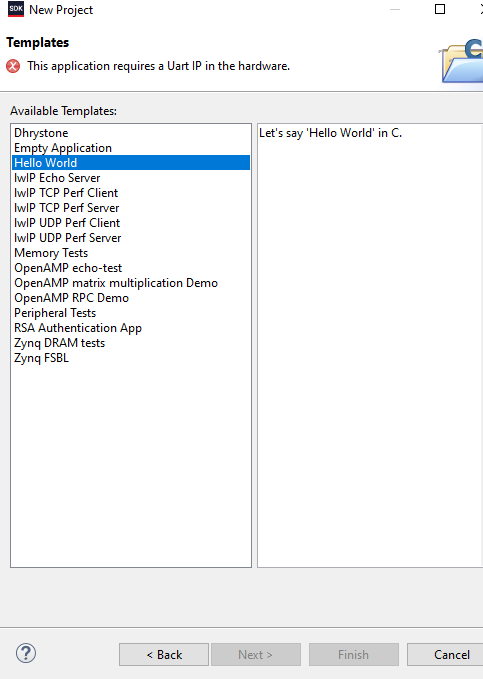
**Step-20:** Now Xilinx SDK file will open, Right click on file select new select application file.



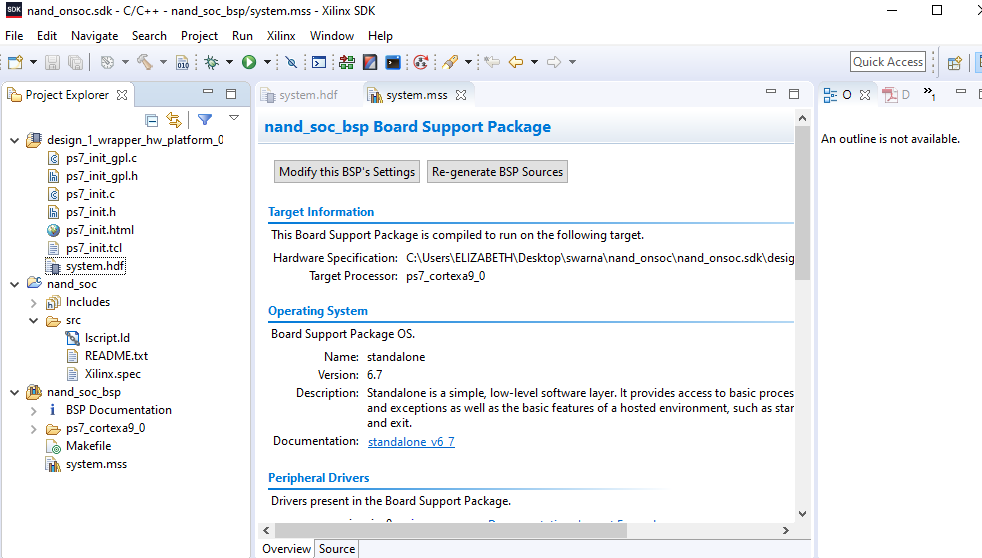
**Step-21:** Here we are designing not gate so give a project name and click it next.



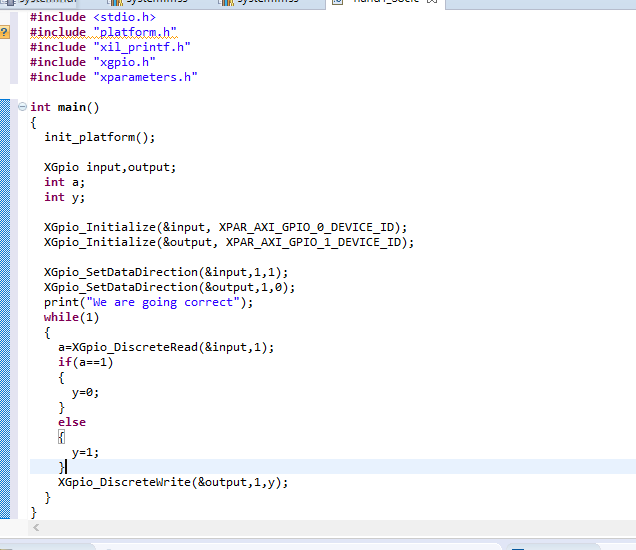
**Step-22:** select hello world click finish.



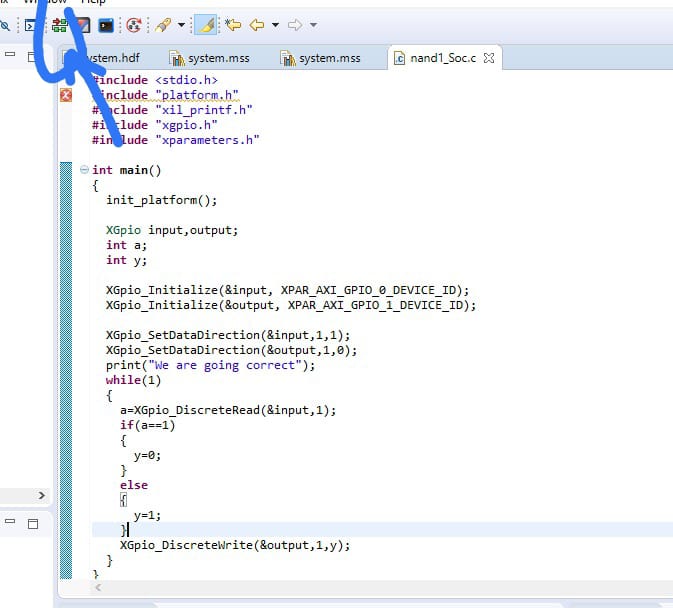
**Step-23:** Right click on src file, select new file, click finish.



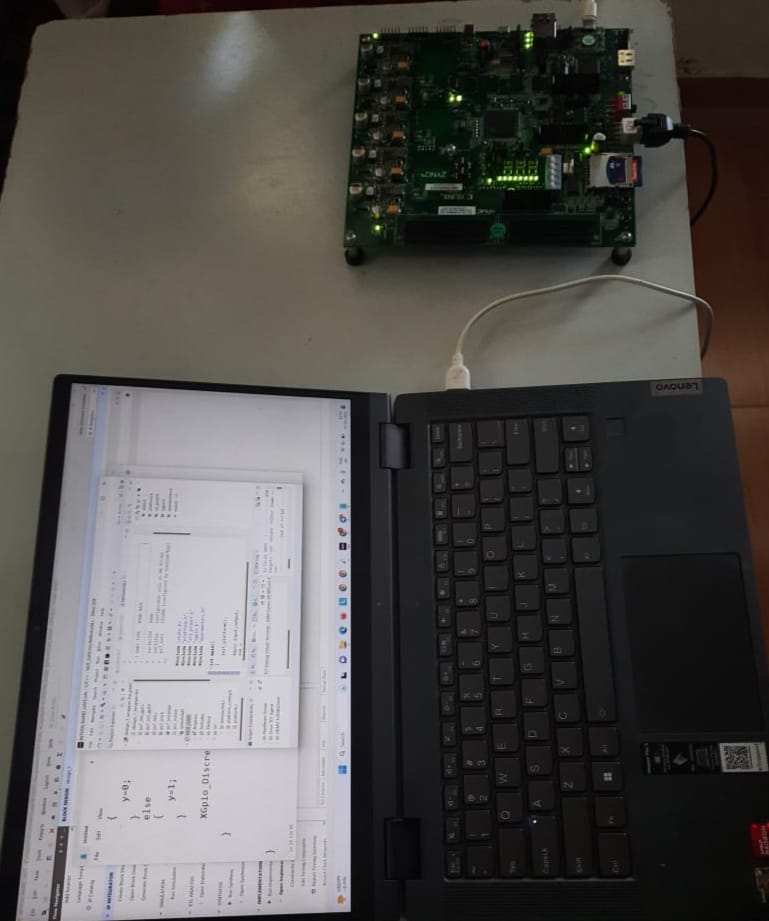
**Step-24:** Now write a not gate code in C programming language.



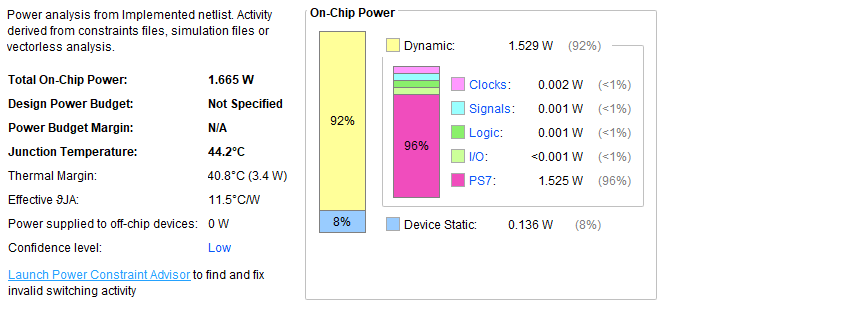
**Step-25:** save it and click program on FPGA now onwards connect a hardware to system.



**Step-26:** Check the output of nand gate on hardware.



**Step-27:** Click on report power for power analysis.



**Step-28:** Click on report utilization for summary of design.

