

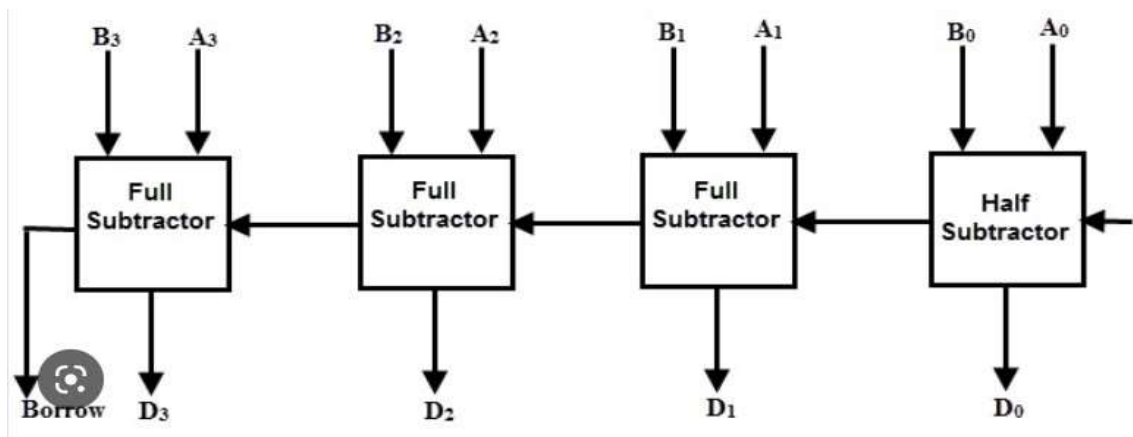
# EXPERIMENT-4

## *4Bit Subtractor*

**Objective:** Verification of 4bit Subtractor by using EDA playground

**Theory:** A 4bit binary subtractor is a combinational logic gates

**Block Diagram:** -



**Implementation:** -

```
module tb_subtractor_pavan;
    reg [3:0] a,b;
    reg c;
    wire [3:0] diff;
    wire out;
    b_subtractor_pavan a1(a,b,c,diff,count);
    initial begin
        $dumpfile("dump.vcd");
        $dumpvars;
        #100 $finish;
    end
    initial
        begin
            a=4'b0000; b=4'b0000; c=1'b0;
            $monitor("a=%0000b b=%0000b c=%0000b diff=%0000b count=%0000b",a,b,c,diff,count);
            #5 a=4'b0001; b=4'b0001; c=1'b0;
            #5 a=4'b0010; b=4'b0010; c=1'b0;
            #5 a=4'b0011; b=4'b0011; c=1'b0;
            #5 a=4'b0100; b=4'b0100; c=1'b0;
            #5 a=4'b0101; b=4'b0101; c=1'b0;
            #5 a=4'b0110; b=4'b0110; c=1'b0;
        end
endmodule

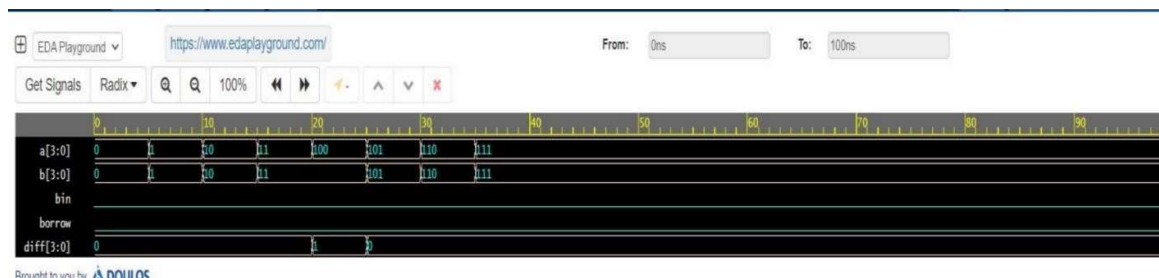
module b_subtractor_pavan(a,b,c,diff,count);
    input [3:0] a,b;
    input c;
    output [3:0] diff;
    output count;
    wire c0,c1,c2;
    full_subtractor_pavan fa1(a[0], ~b[0], 1, diff[0], c0);
    full_subtractor_pavan fa2(a[1], ~b[1], c0, diff[1], c1);
    full_subtractor_pavan fa3(a[2], ~b[2], c1, diff[2], c2);
    full_subtractor_pavan fa4(a[3], ~b[3], c2, diff[3], count);
endmodule

module full_subtractor_pavan(a,b,c,diff,borrow);
    input a,b,c;
    output diff,borrow;
    assign diff=(a/b)/c;
    assign borrow=((a&b) | (b&c) | (a&c));
endmodule
```

## Output: -

```
● Log  Share
[2023-03-07 11:26:57 EST] [verilog] --wall' design.sv testbench.sv && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
a=0000 b=0000 c=0 diff=0000 cout=1
a=0001 b=0001 c=0 diff=0000 cout=1
a=0010 b=0010 c=0 diff=0000 cout=1
a=0011 b=0011 c=0 diff=0000 cout=1
a=0100 b=0011 c=0 diff=0001 cout=1
a=0101 b=0101 c=0 diff=0000 cout=1
a=0110 b=0110 c=0 diff=0000 cout=1
a=0111 b=0111 c=0 diff=0000 cout=1
Finding VCD file...
./dump.vcd
[2023-03-07 11:26:57 EST] Opening EPWave...
Done
```

## Waveform: -



## Observations:

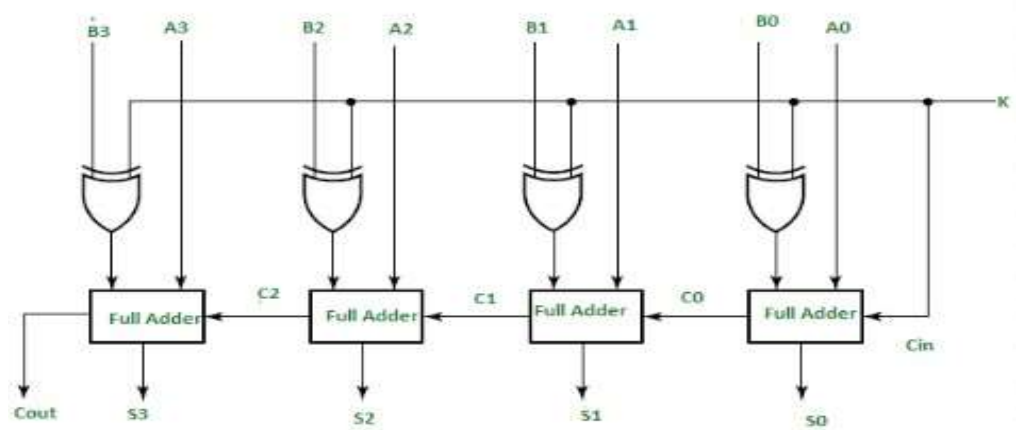
Finally we verified 4-bit subtractor by Verilog code by using EDA play ground

## 4Bit addder

**Objective:** Verification of 4bit Adder by using EDA playground

**Theory:** A 4bit binary adder is a combinational logic gates

## Block Diagram: -



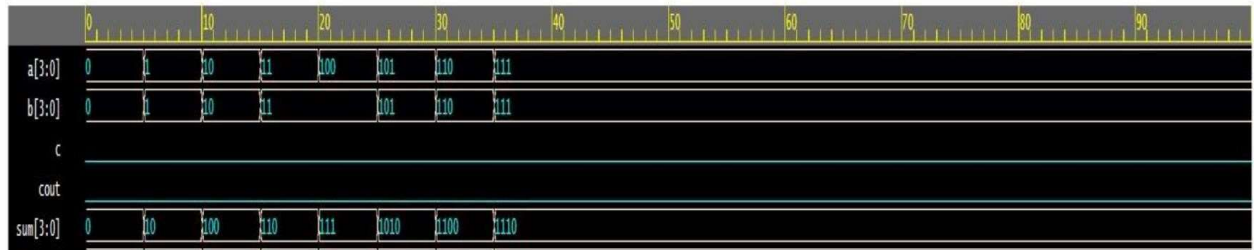
## Implementation: -

```
EDA playground
Run Save EDA Playground now has increased capacity. Usage restrictions have been lifted. Sorry for the inconvenience.
Playgrounds Profile
Brought to you by DOULOS
Languages & Libraries
Testbench + Design
SystemVerilog/Verilog
UVM / OVM
None
Other Libraries
None
OVL 2.8.1
SVUnit 2.11
Enable TL-Verilog
Enable Easier UVM
Enable VUnit
Tools & Simulators
Icarus Verilog 0.9.7
testbench.sv
design.sv
module tb_add_pavan;
reg [3:0] a,b;
reg c;
wire [3:0] sum;
b_subtractor_pavan a1(a,b,c,diff,count);
initial begin
  $dumpfile("dump.vcd");
  $dumpvars;
  #100 $finish;
end
initial
begin
  a=a'b'0000; b=b'b'0000; c=c'1'b0;
  $monitor("a=%0000b b=%0000b c=%0000b diff=%0000b count=%0000b",a,b,c,diff,count);
  #5 a=a'b'0001; b=b'b'0001; c=c'1'b0;
  #5 a=a'b'0010; b=b'b'0010; c=c'1'b0;
  #5 a=a'b'0011; b=b'b'0011; c=c'1'b0;
  #5 a=a'b'0100; b=b'b'0100; c=c'1'b0;
  #5 a=a'b'0101; b=b'b'0101; c=c'1'b0;
  #5 a=a'b'0110; b=b'b'0110; c=c'1'b0;
end
module b_subtractor_pavan(a,b,cin,sum,count);
input [3:0] a,b;
input cin;
output [3:0] sum;
output cout;
wire c0,c1,c2;
full_subtractor_pavan fa1(a[0], ~b[0], 1, diff[0], c0);
full_subtractor_pavan fa1(a[1], ~b[1], c0, diff[1], c1);
full_subtractor_pavan fa1(a[2], ~b[2], c1, diff[2], c2);
full_subtractor_pavan fa1(a[3], ~b[3], c2, diff[3], cout);
endmodule
module full_subtractor_pavan(a,b,c,sum,carry);
input a,b,c;
output sum,carry;
assign diff=(a^b)^c;
assign carry=((a&b)|(b&c)|(a&c));
endmodule
```

## Output:

```
Log Share
[2023-03-07 10:36:33 EST] iverilog '-wall' design.sv testbench.sv && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
a=0000 b=0000 c=0 sum=0000 cout=1
a=0001 b=0001 c=0 sum=0000 cout=1
a=0010 b=0010 c=0 sum=0000 cout=1
a=0011 b=0011 c=0 sum=0000 cout=1
a=0100 b=0011 c=0 sum=0001 cout=1
a=0101 b=0101 c=0 sum=0000 cout=1
a=1101 b=0100 c=0 sum=1001 cout=1
a=1100 b=0011 c=0 sum=1001 cout=1
Finding VCD file...
./dump.vcd
[2023-03-07 10:36:33 EST] Opening EPWave...
Done
```

## Waveform: -



## Observations:

Finally we verified 4-bit Adder by Verilog code by using EDA play ground