DIGITAL LOGIC DESIGN LAB

REPORT

ECE 1003 L 21-22

WIN 2022-23

DECLARATION BY THE

CANDIDATE

I, SWARNLATA, solemnly declare that the project report is based on my own work carried out during the course of our study under the supervision of Chafle pratiksha vasantrao. I assert the statements made and conclusions drawn are an outcome of my research work.

I further certify that

I. The work contained in the report is original and has been done by me under the general supervision of my supervisor.
II. The work has not been submitted to any other Institution for any other degree/diploma/certificate in this university or any other University of India or abroad.
III. I have followed the guidelines provided by the university in writing the report.

Name: SWARNLATA

Roll No.: 22BCE8591

Experiment List

Sr. No	Experiment Name
1	DESIGN AND VERIFICATION OF VARIOUS LOGIC GATES
2	
3	
4	
5	
6	
7	
8	
9	

Experiment 1

OR GATE:

Objective: Verification of OR gate..

Theory:. TO evaluate or gate using eda playground Y=(A.B)The OR Gate may have two or more inputs and only output. The output assumes the logic 1 state, even if one of its inputs is at logic 1 state. Its output assumes logic 0 state, only when each of its input logic 0 state.

Block Diagram: -

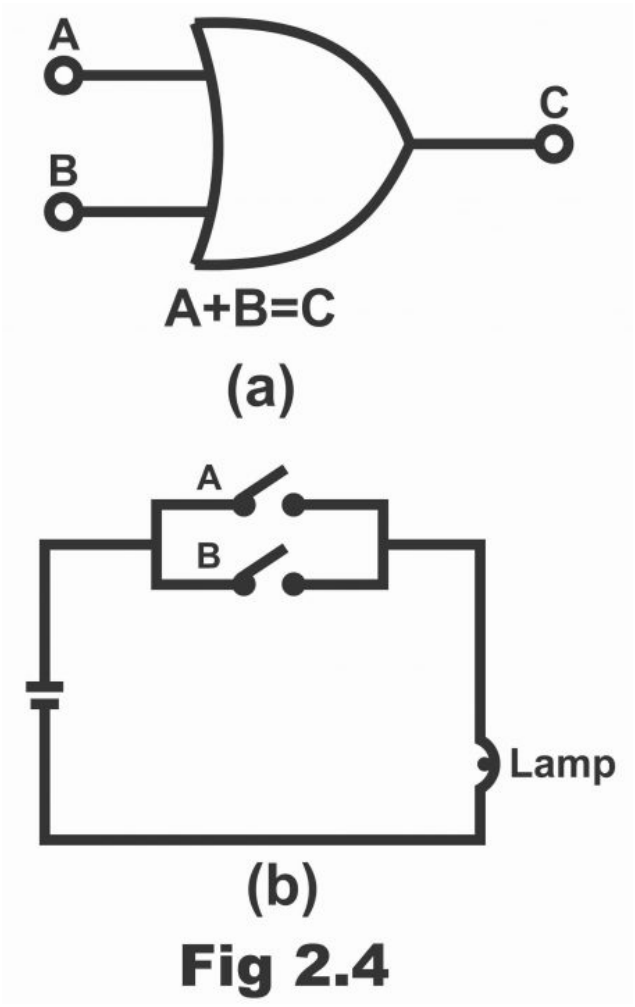
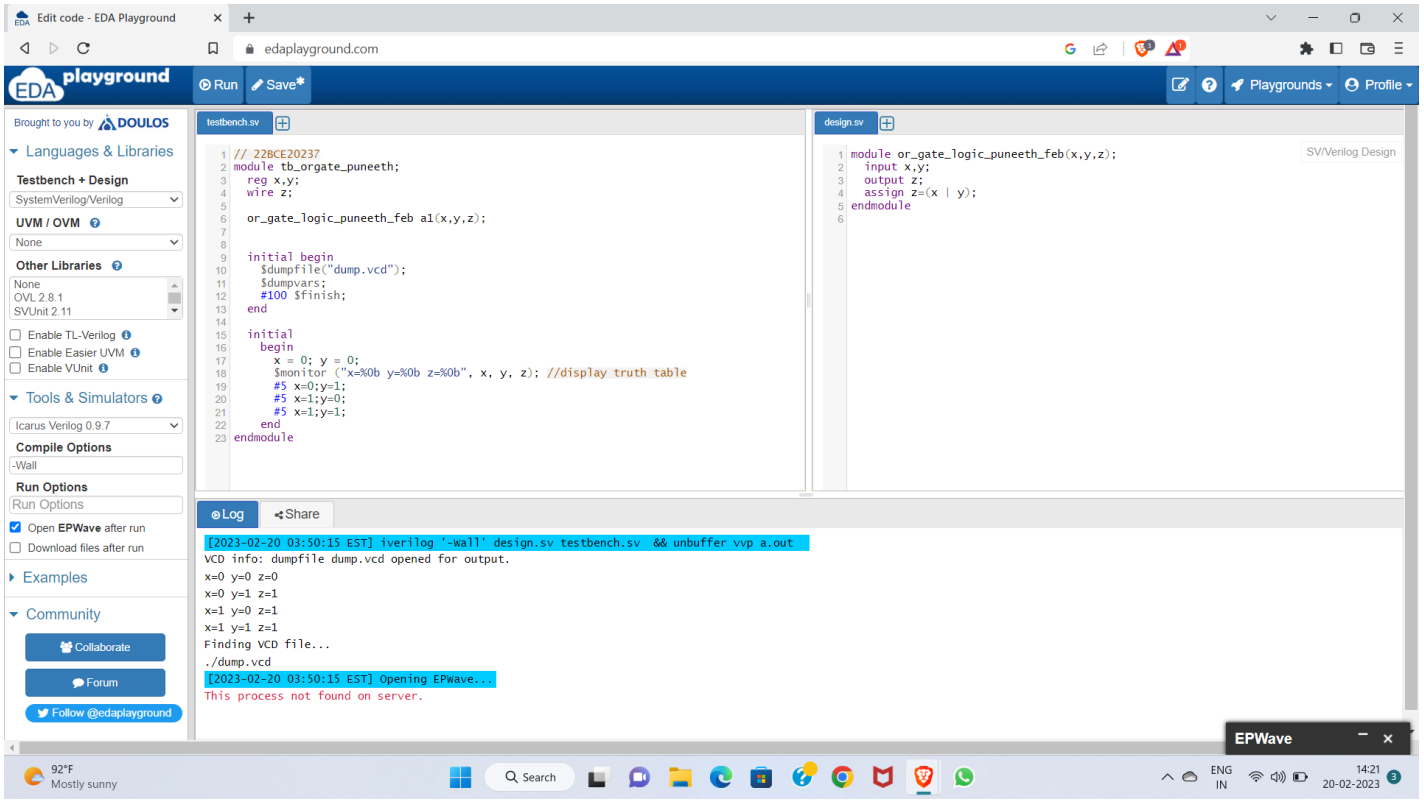
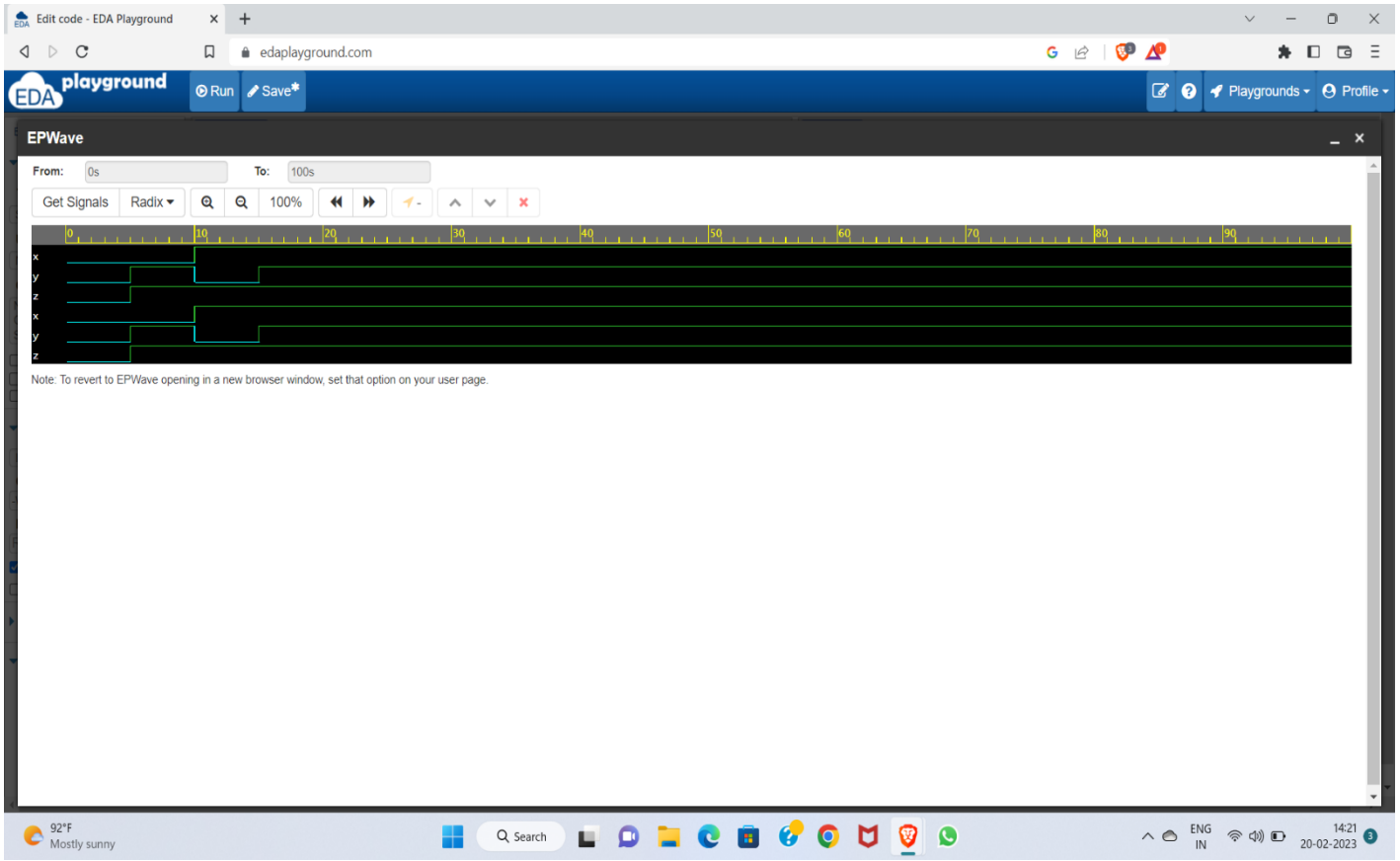


Fig 2.4

Implementation and output:



Waveform: -



Observations:

Y = A+B

Truth table for OR Gate

Input A	Input B	Output Y
0	0	0
0	1	1
1	1	1
1	0	1

AND GATE

OBJECTIVE : verification of AND gate

THEORY:TO evaluate AND gate (y=A.B) using eda playground. The AND gate is a basic digital logic gate that implements logical conjunction (∧) from mathematical logic – AND gate behaves according to the truth table. A HIGH output (1) results only if all the inputs to the AND gate are HIGH (1). If not all inputs to the AND gate are HIGH, LOW output results.

BLOCK DIAGRAM:

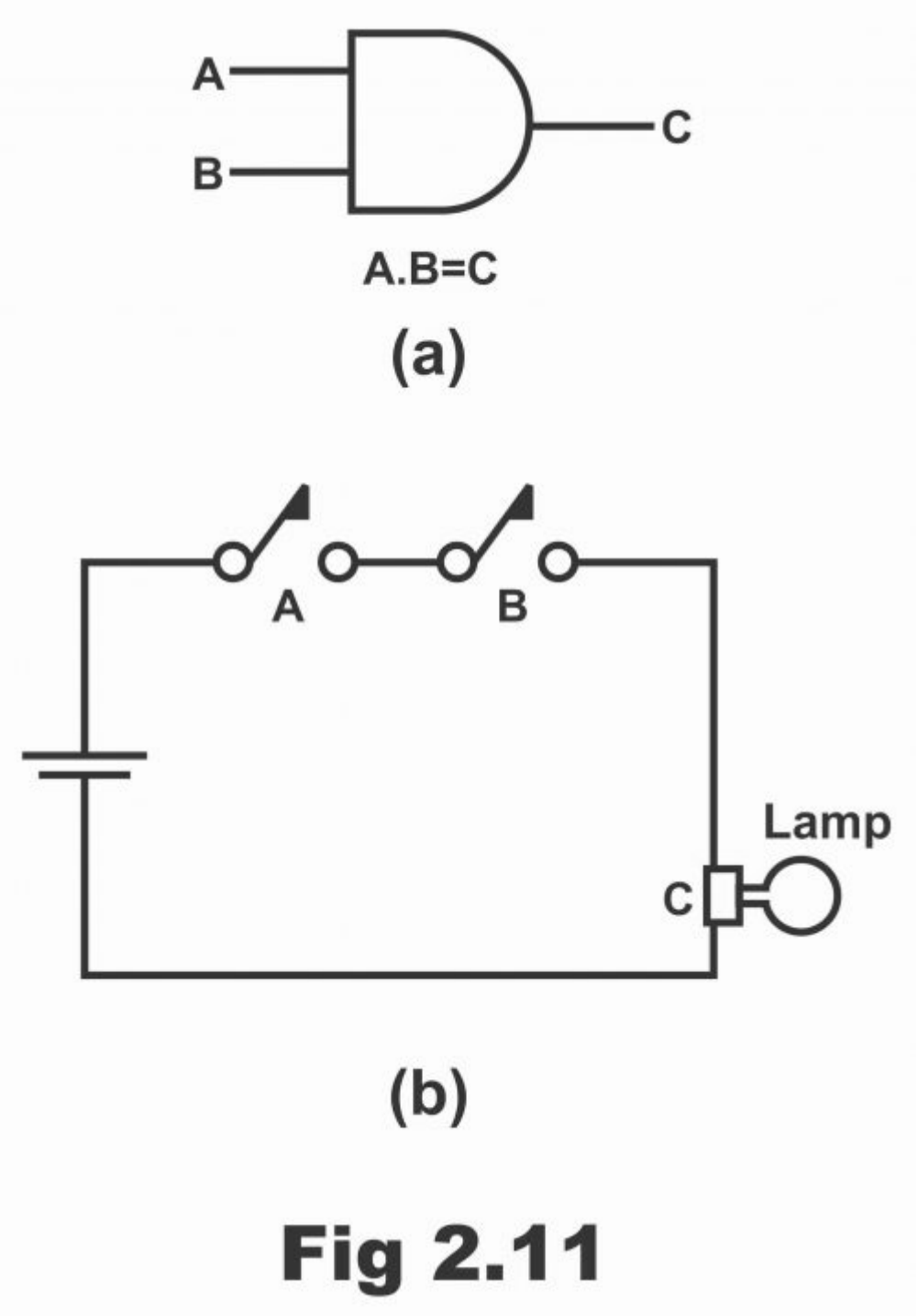
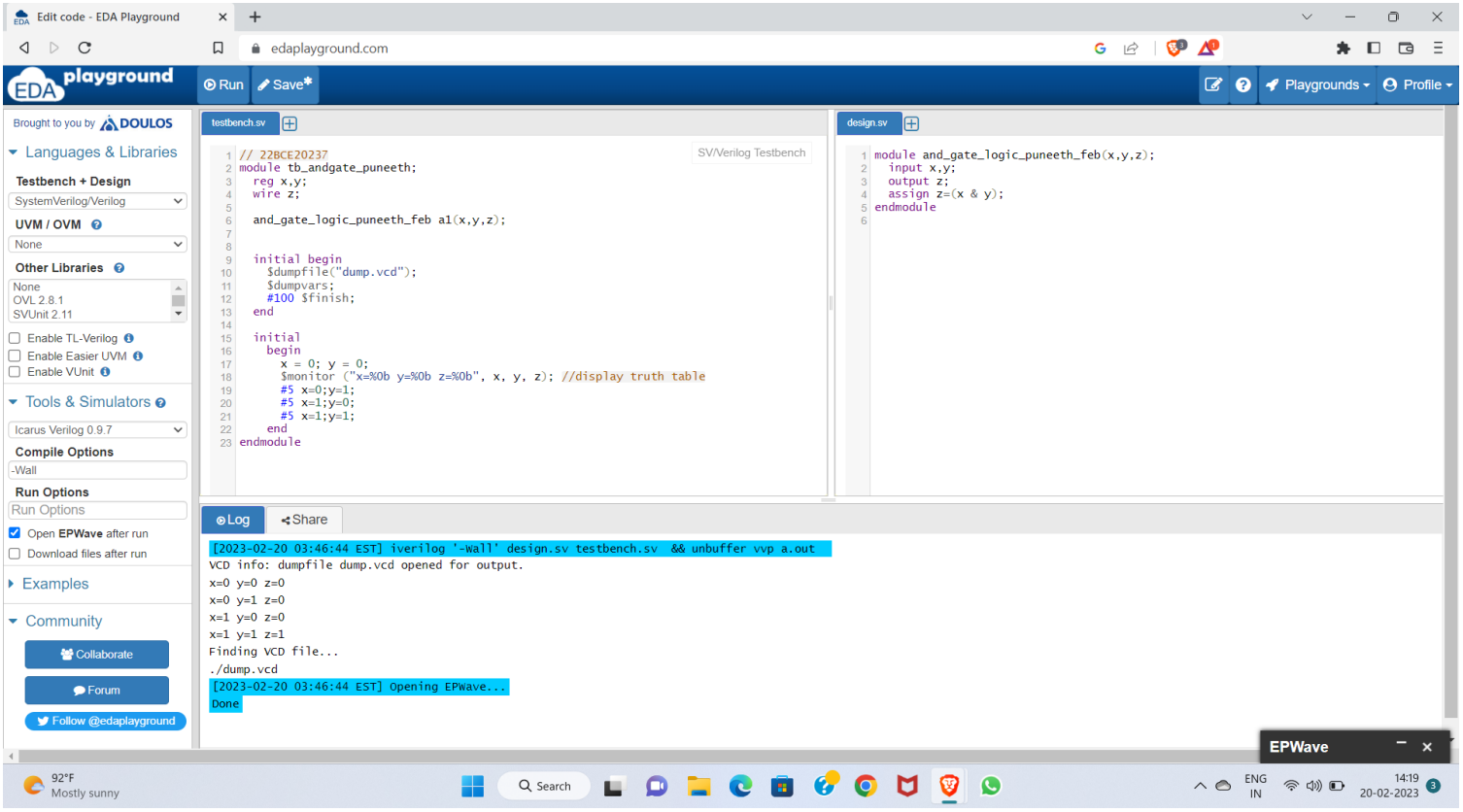
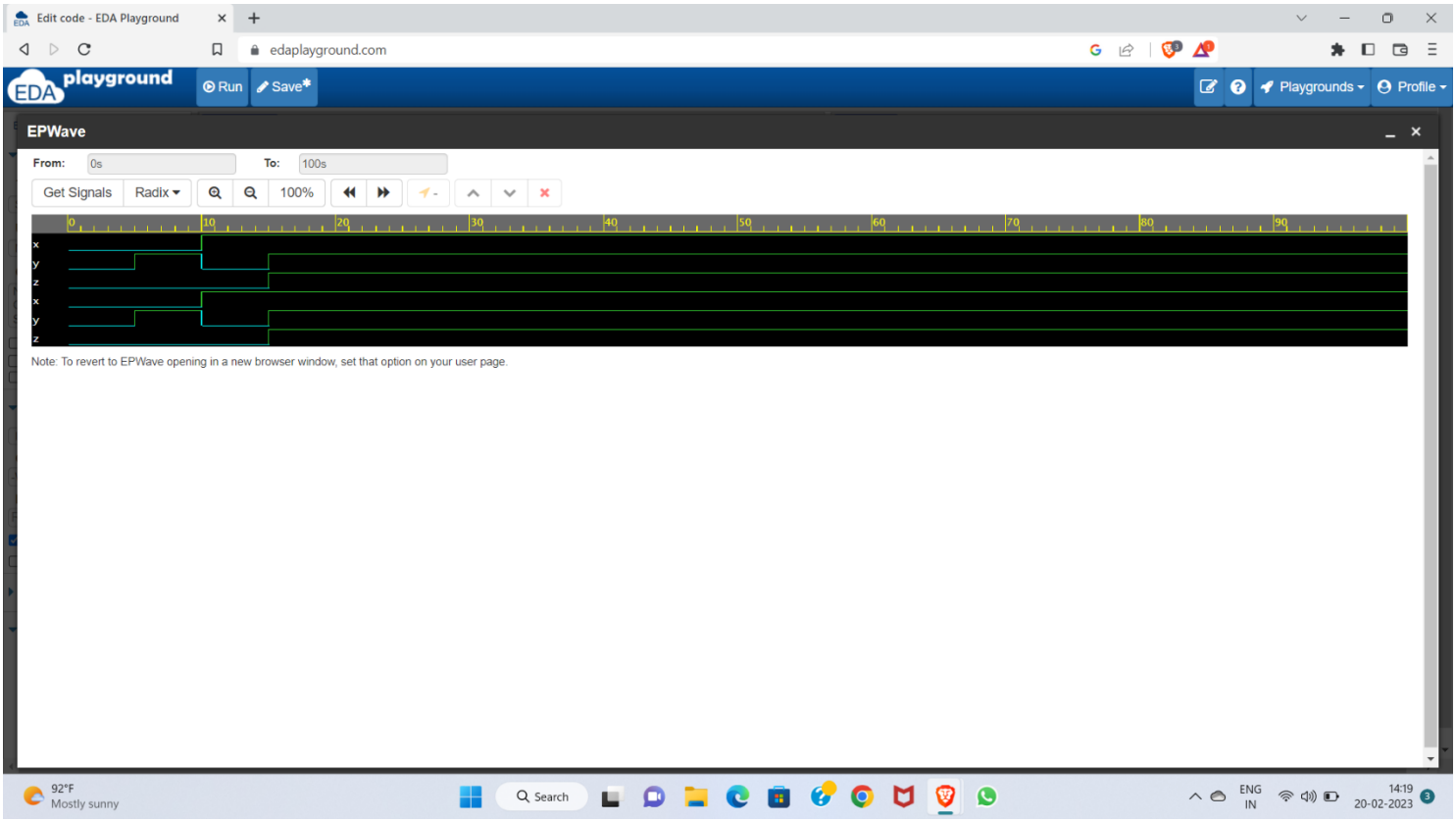


Fig 2.11

IMPLEMENTATION AND OUTPUT:



WAVE FORM:



OBSERVATION:

Z = A.B

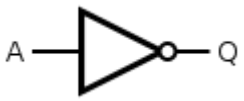
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

NOT GATE

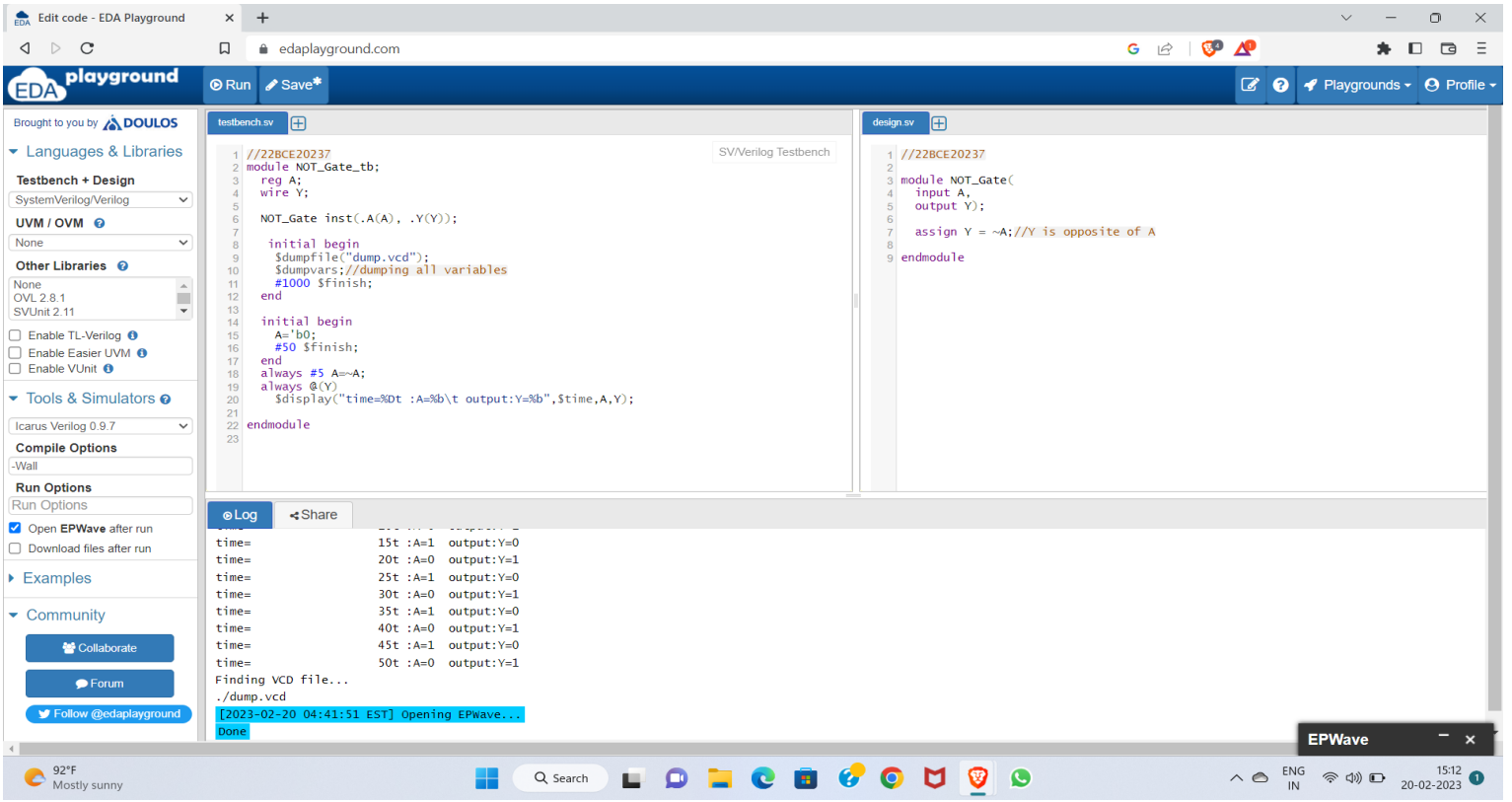
OBJECTIVE : VERIFICATION OF NOT GATE

THEORY: to verify not gate using eda playground. The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top, as shown at the outputs.

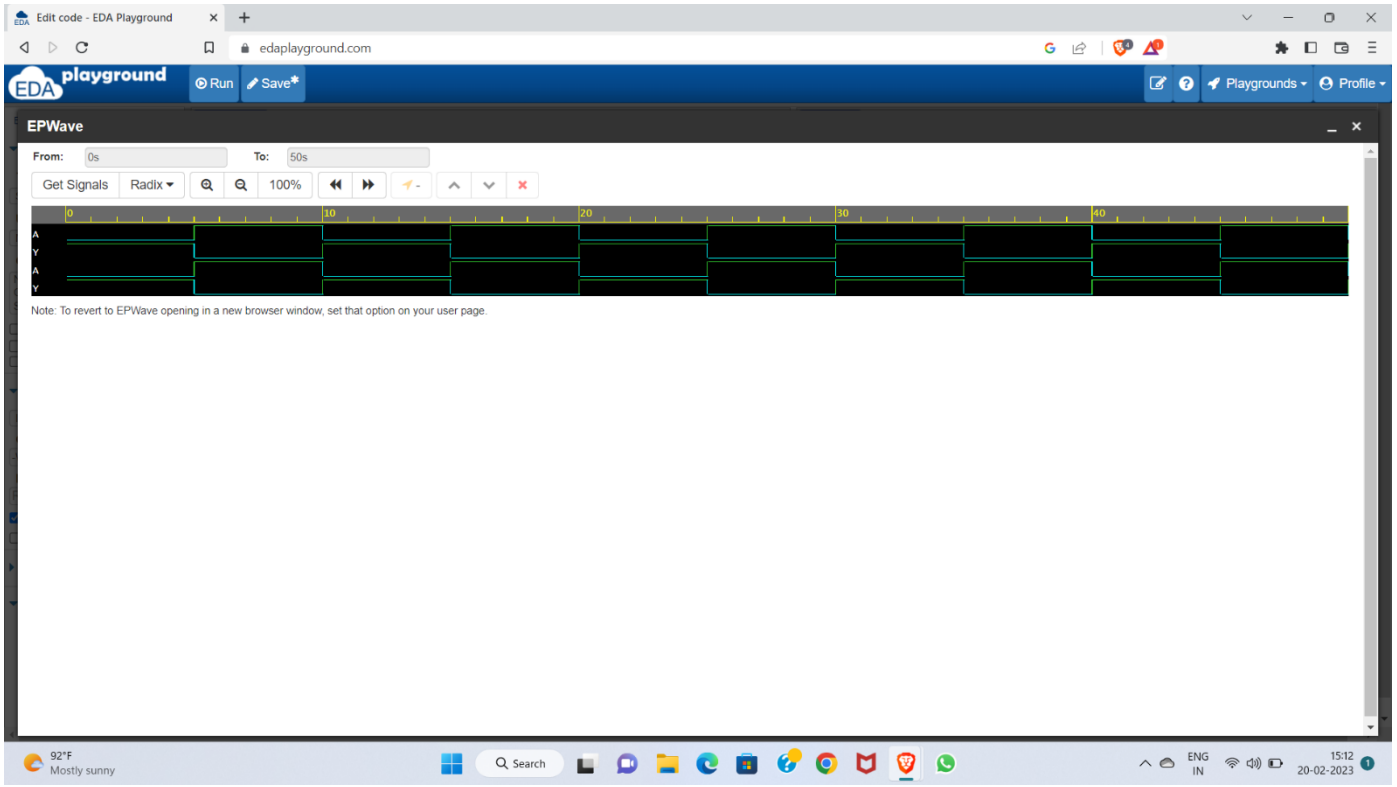
BLOCK DIAGRAM:



IMPLEMENTATION AND OUTPUT:



WAVE FORM:



OBSERVATION:

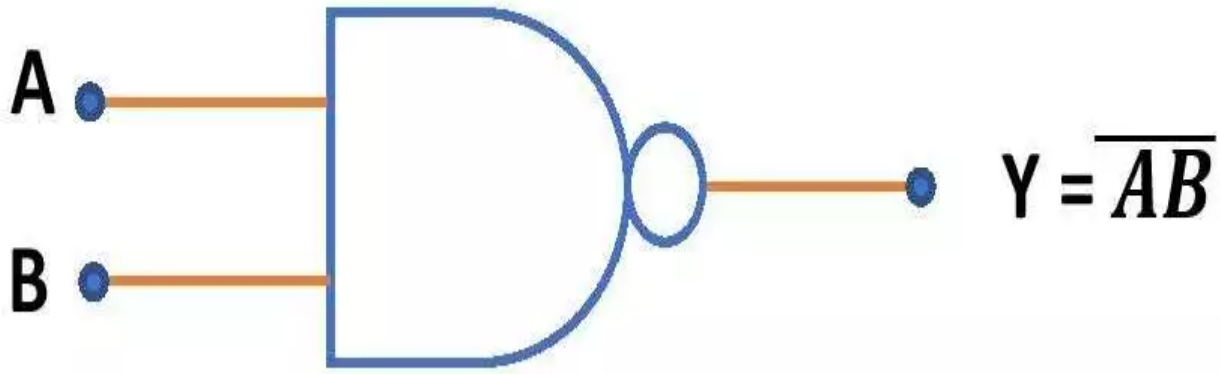
Input	Output
A	Y
0	1
1	0

NAND GATE

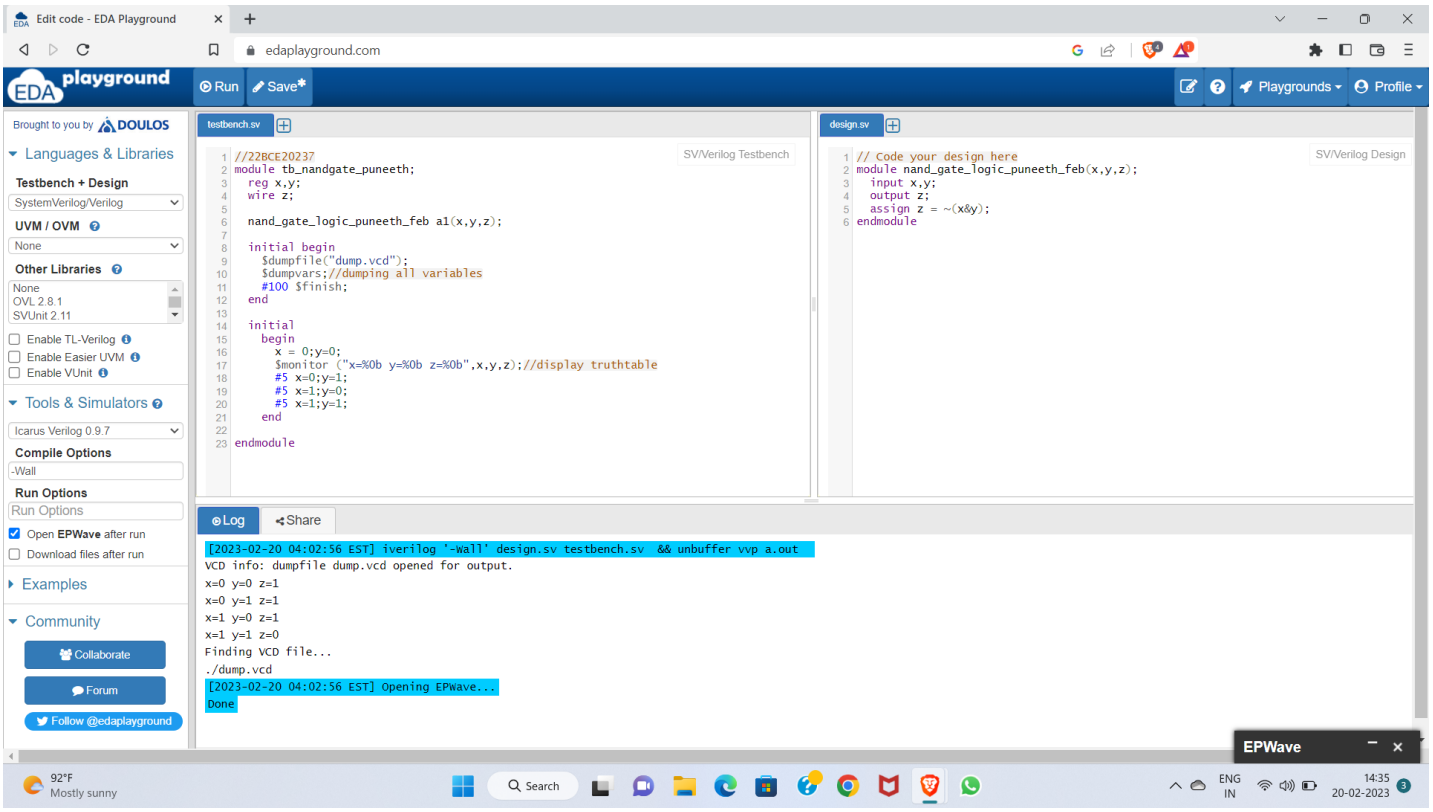
OBJECTIVE: VERIFICATION OF NAND GATE

THEORY: TO evaluate nand gate using eda play ground. In digital electronics, a NAND gate is a logic gate which produces an output which is false only if all its inputs are true; thus its output is complement to that of an AND gate. A LOW output results only if all the inputs to the gate are HIGH; if any input is LOW, a HIGH output results.

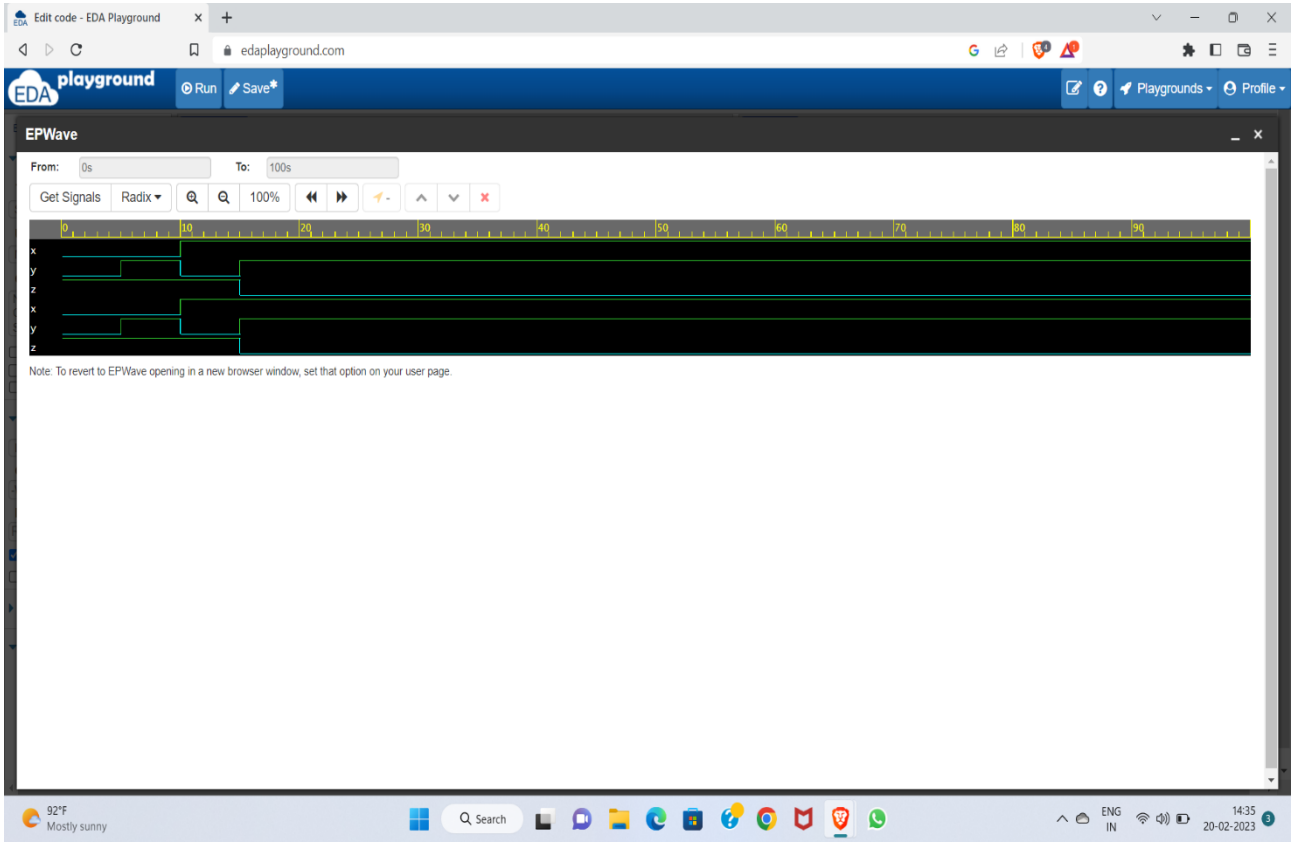
BLOCK DIAGRAM:



IMPLEMENTATION AND OUTPUT:



WAVE FORM:



OBSERVATIONS:

Input		Output
A	B	Y= $\overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

V

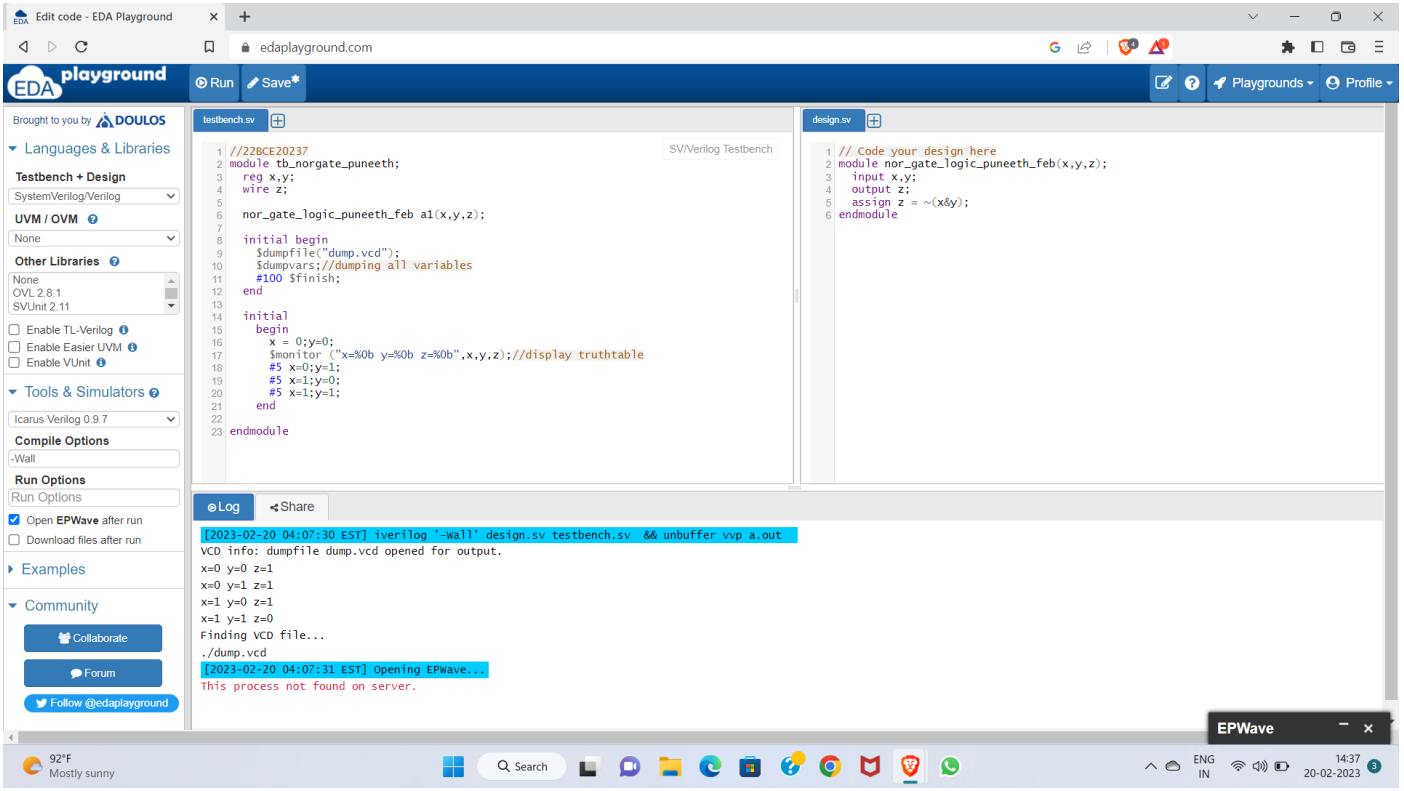
NOR GATE

OBJECTIVE : verification of nor gate

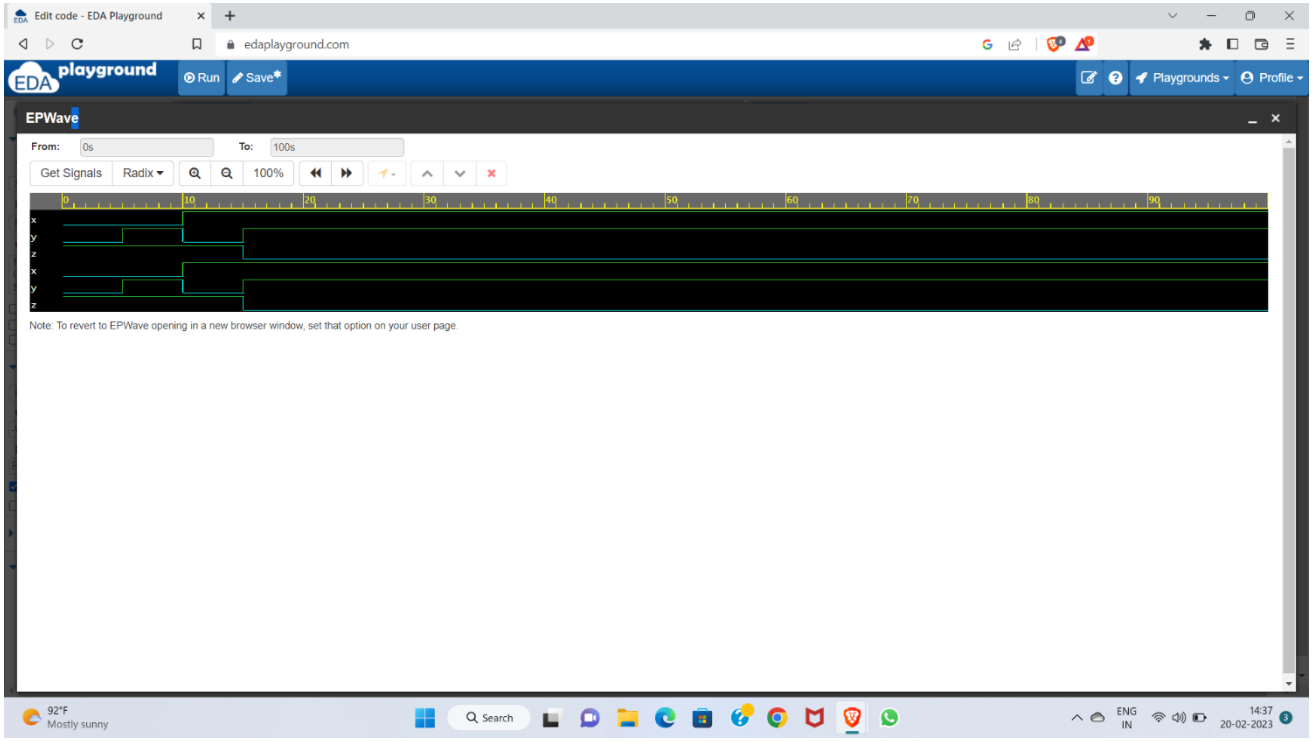
THEORY: TO verify nor gate using eda playground. The NOR gate is a digital logic gate that implements logical NOR - it behaves according to the truth table to the right. A HIGH output results if both the inputs to the gate are LOW; if one or both input is HIGH, a LOW output results. NOR is the result of the negation of the OR operator.

BLOCK DIAGRAM:

IMPLEMENTATION AND OUTPUT:



WAVE FORM:



OBSERVATIONS:

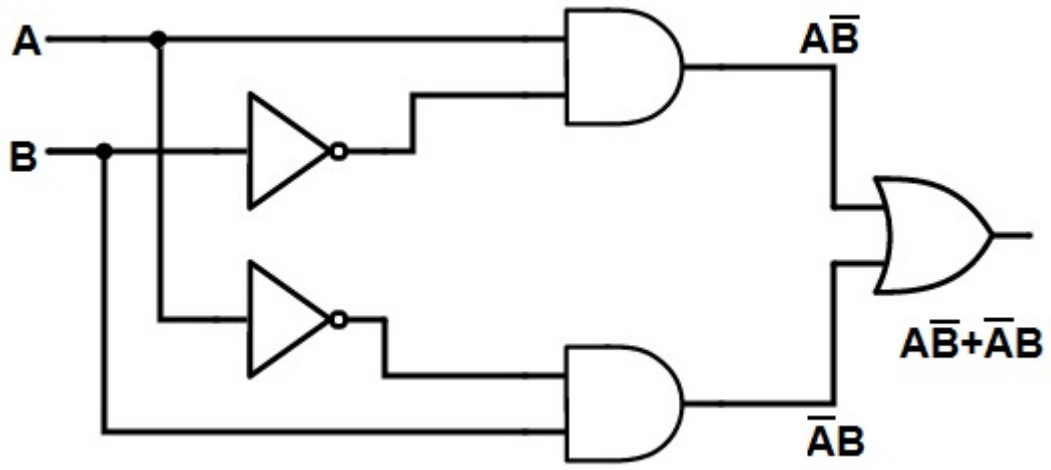
Input		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

XOR GATE

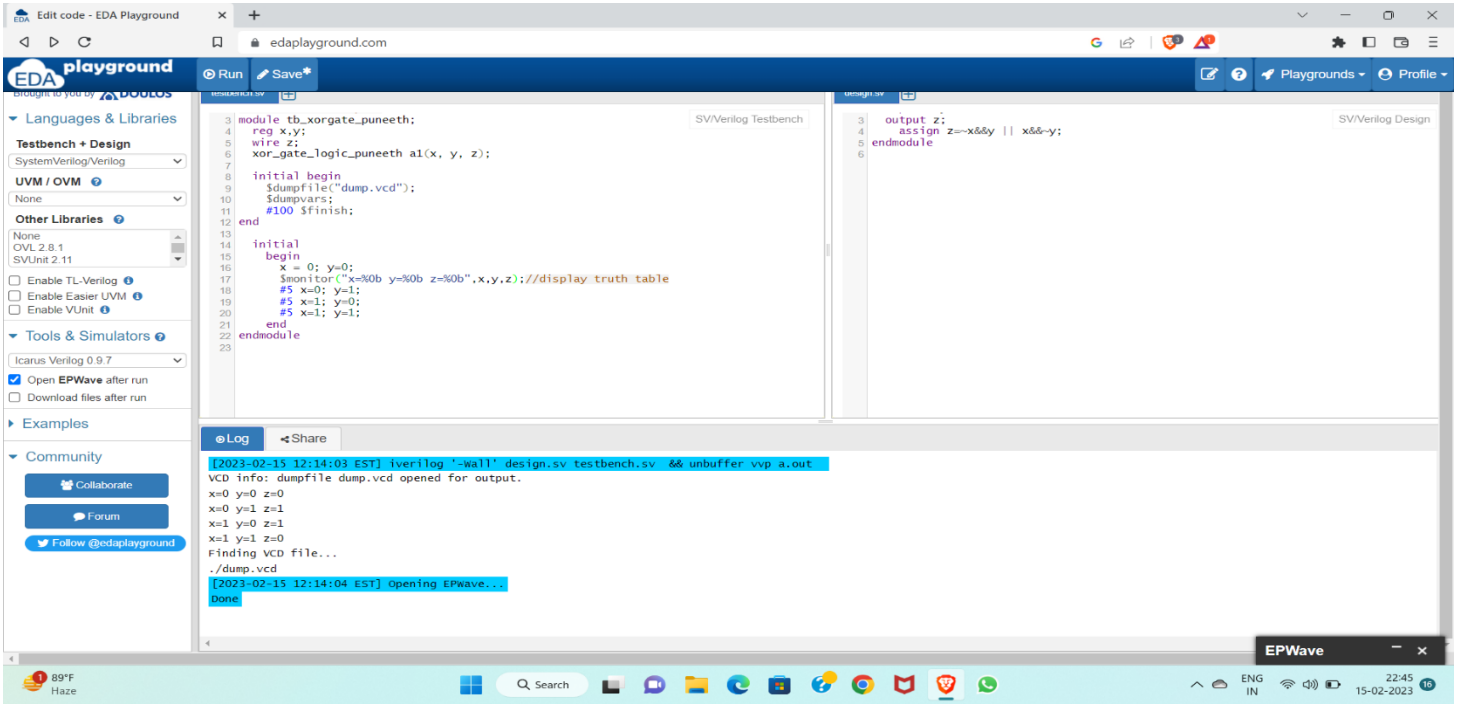
OBJECTIVE:verification of xor gate

THEORY: evaluation of xor gate using eda playground. The output is "true" if either, but not both, of the inputs are "true." The output is "false" if both inputs are "false" or if both inputs are "true."

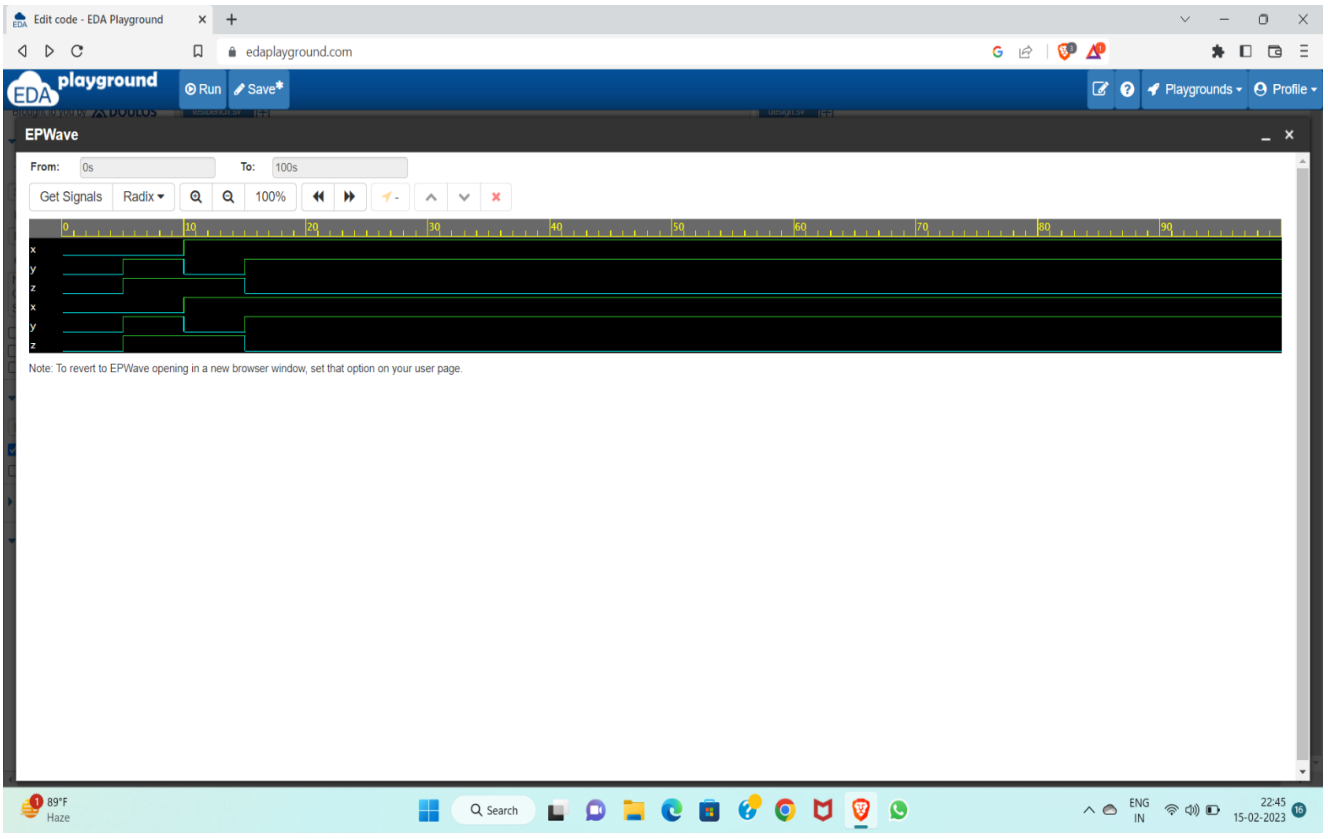
BLOCK DIAGRAM:



IMPLEMENTATION AND OUTPUT:



WAVE FORM:



OBSERVATIONS:

EX-OR (X-OR) Gate Truth Table

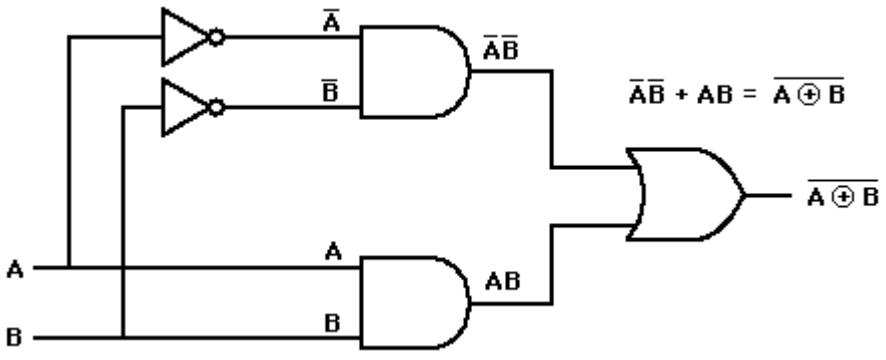
Inputs		Output $X = A \oplus B$
A	B	
0	0	0
0	1	1
1	0	1
1	1	0

XNOR GATE

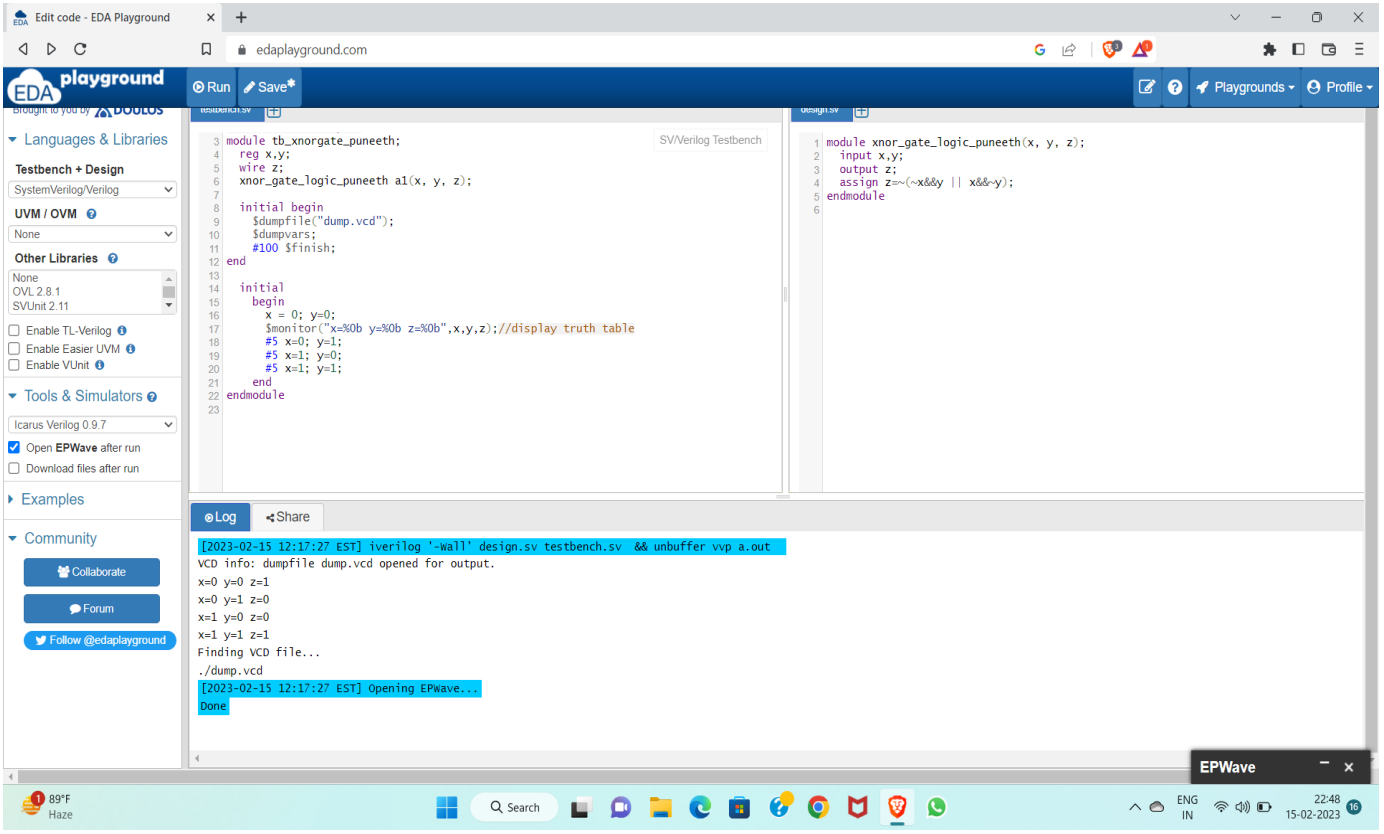
OBJECTIVE: Verification of xnor gate

THEORY: To evaluate xnor gate using eda playground. The XNOR (exclusive-NOR) is **a**combination XOR gate followed by an inverter. Its output is "true" if the inputs are the same, and "false" if the inputs are different.

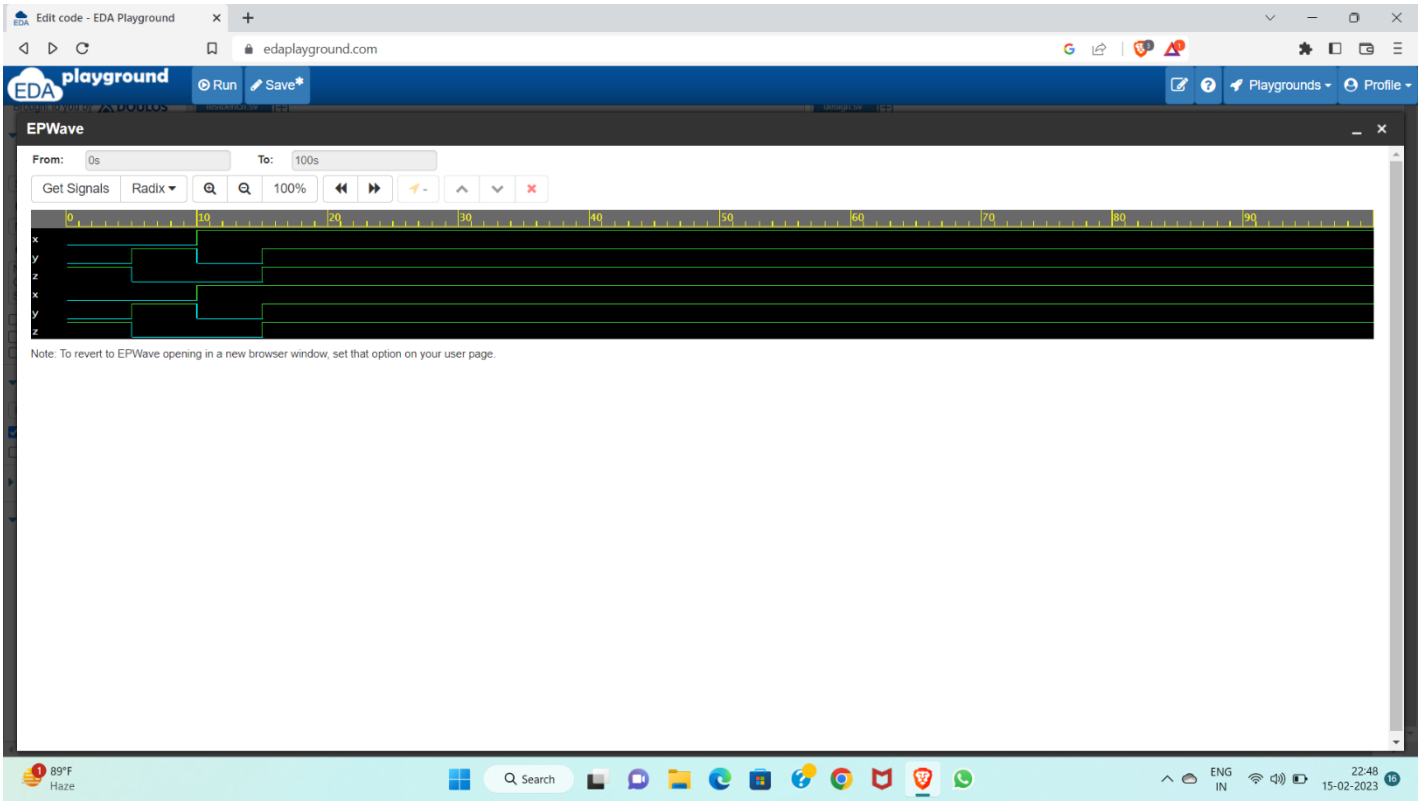
BLOCK DIAGRAM:



IMPLEMENTATION AND OUTPUT:



WAVE FORM:



OBSERVATIONS:

EX-NOR (X-NOR) Gate Truth Table

Inputs		Output $X = \overline{A \oplus B}$
A	B	
0	0	1
0	1	0
1	0	0
1	1	1