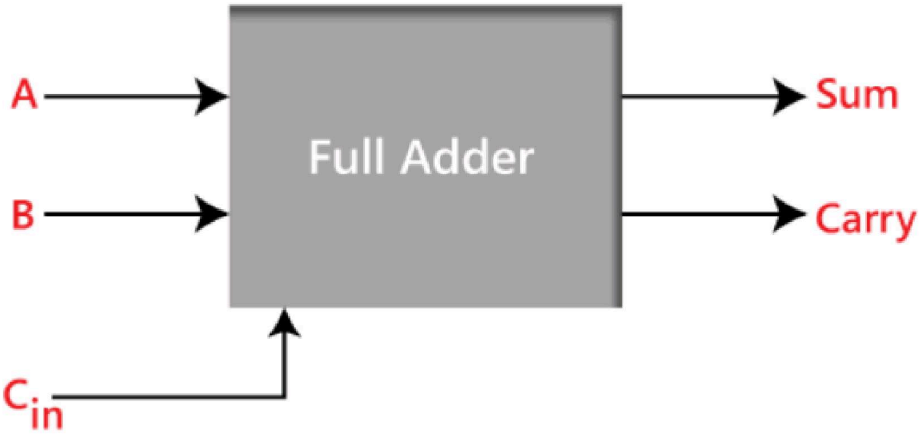
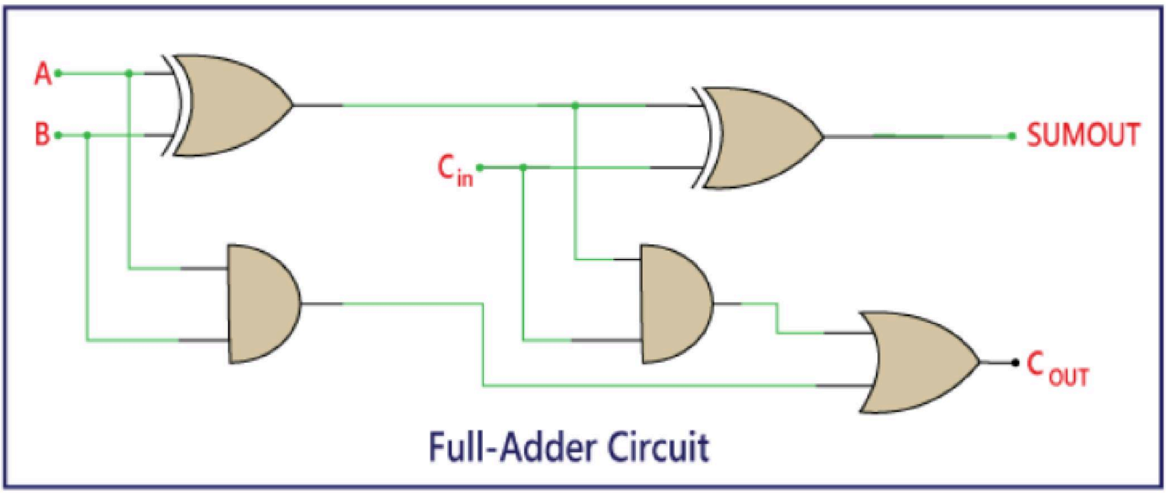
Experiment 3
Full Adder

Objective: Verification of Full adder

Theory:Full adder is a combinational logic circuit

Block Diagram: -

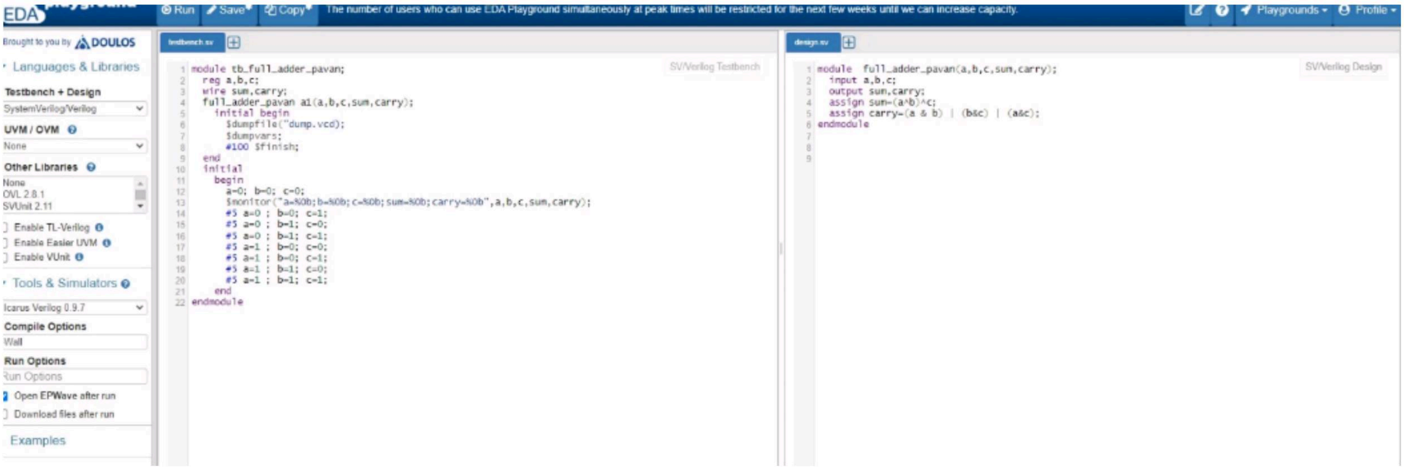




Full-Adder Circuit

Implementation: -

Dataflow: -



Testbench + Design: SystemVerilog/Verilog

UVM / OVM: None

Other Libraries: None, OVL 2.8.1, SVUnit 2.11

□ Enable TL-Verilog
□ Enable Easier UVM
□ Enable VUnit

Icarus Verilog 0.9.7

Compile Options: -Wall

Run Options: Run Options

☑ Open EPWave after run
□ Download files after run

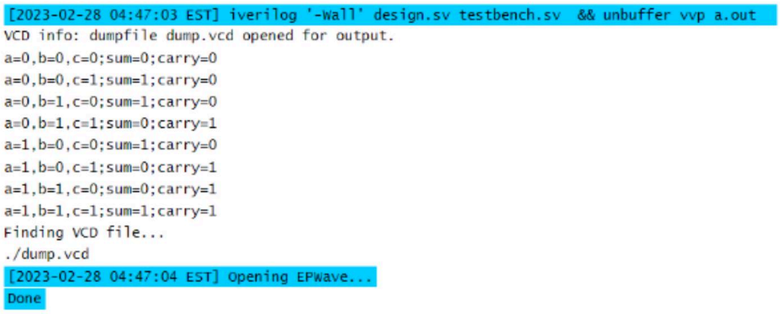
testbench.sv

```verilog
module tb_full_adder_pavan;
  reg a,b,c;
  wire sum,carry;
  full_adder_pavan a1(a,b,c,sum,carry);
    initial begin
      $dumpfile("dump.vcd");
      $dumpvars;
      #100 $finish;
  end
  initial
    begin
      a=0; b=0; c=0;
      $monitor("a=%0b;b=%0b;c=%0b;sum=%0b;carry=%0b",a,b,c,sum,carry);
      #5 a=0 ; b=0; c=1;
      #5 a=0 ; b=1; c=0;
      #5 a=0 ; b=1; c=1;
      #5 a=1 ; b=0; c=0;
      #5 a=1 ; b=0; c=1;
      #5 a=1 ; b=1; c=0;
      #5 a=1 ; b=1; c=1;
    end
endmodule
```

design.sv

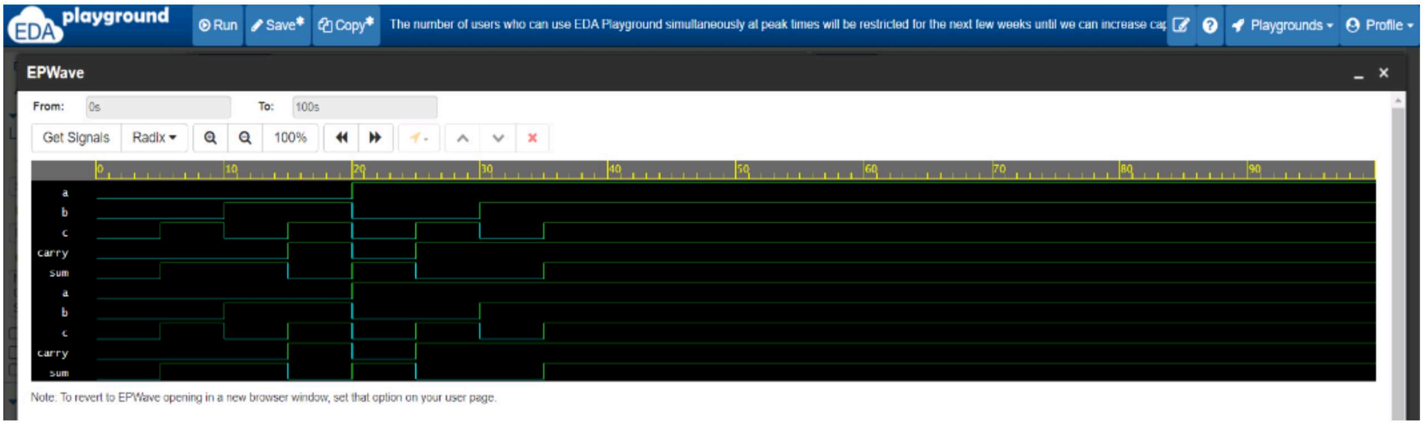
```verilog
module  full_adder_pavan(a,b,c,sum,carry);
  input a,b,c;
  output sum,carry;
  assign sum=(a^b)^c;
  assign carry=(a & b) | (b&c) | (a&c);
endmodule
```

Output: -



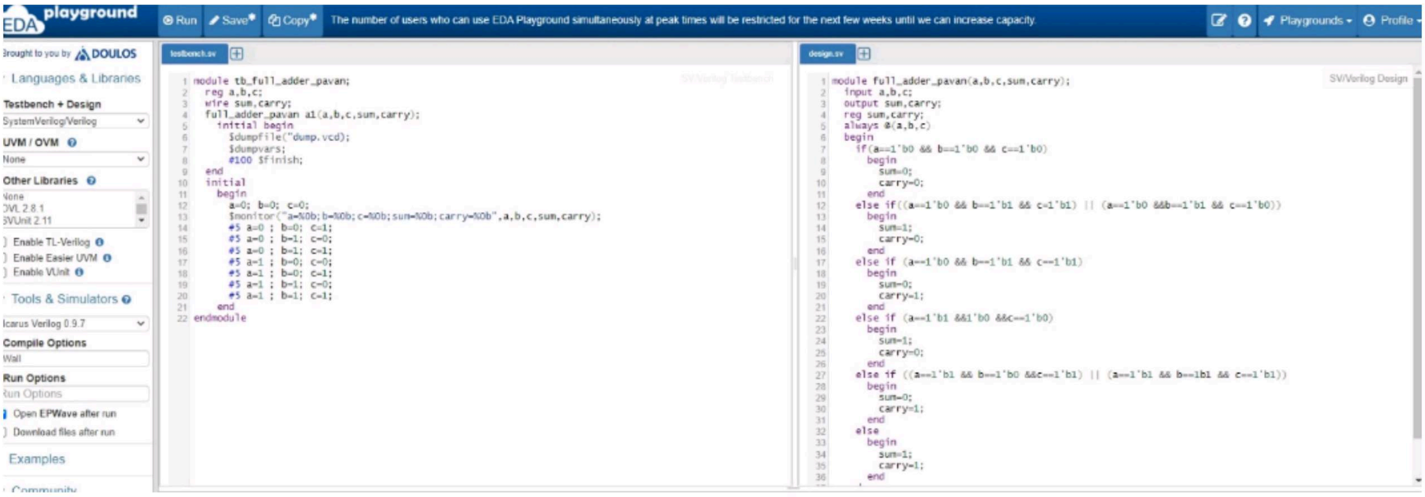
```
[2023-02-28 04:47:03 EST] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
a=0,b=0,c=0;sum=0;carry=0
a=0,b=0,c=1;sum=1;carry=0
a=0,b=1,c=0;sum=1;carry=0
a=0,b=1,c=1;sum=0;carry=1
a=1,b=0,c=0;sum=1;carry=0
a=1,b=0,c=1;sum=0;carry=1
a=1,b=1,c=0;sum=0;carry=1
a=1,b=1,c=1;sum=1;carry=1
Finding VCD file...
./dump.vcd
[2023-02-28 04:47:04 EST] Opening EPWave...
Done
```

Waveform: -


playground
Run
Save
Copy
The number of users who can use EDA Playground simultaneously at peak times will be restricted for the next few weeks until we can increase cap
Playgrounds
Profile
EPWave
From: 0s
To: 100s
Get Signals
Radix
100%
0
10
20
30
40
50
60
70
80
90
a
b
c
carry
sum
a
b
c
carry
sum

Note: To revert to EPWave opening in a new browser window, set that option on your user page.

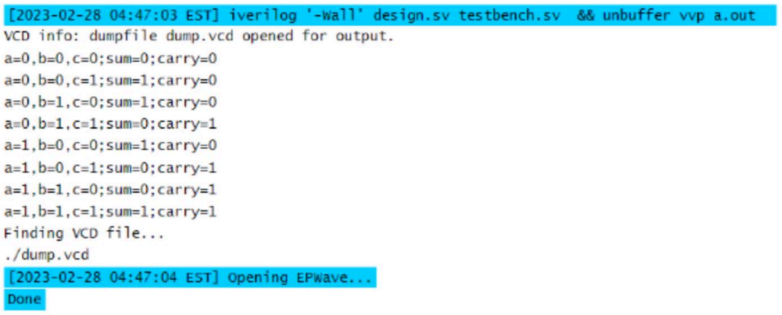
Behavioral: -



```
module tb_full_adder_pavan;
  reg a,b,c;
  wire sum,carry;
  full_adder_pavan a1(a,b,c,sum,carry);
    initial begin
      $dumpfile("dump.vcd);
      $dumpvars;
      #100 $finish;
  end
  initial
    begin
      a=0; b=0; c=0;
      $monitor("a=%0b;b=%0b;c=%0b;sum=%0b;carry=%0b",a,b,c,sum,carry);
      #5 a=0 ; b=0; c=1;
      #5 a=0 ; b=1; c=0;
      #5 a=0 ; b=1; c=1;
      #5 a=1 ; b=0; c=0;
      #5 a=1 ; b=0; c=1;
      #5 a=1 ; b=1; c=0;
      #5 a=1 ; b=1; c=1;
    end
endmodule
```

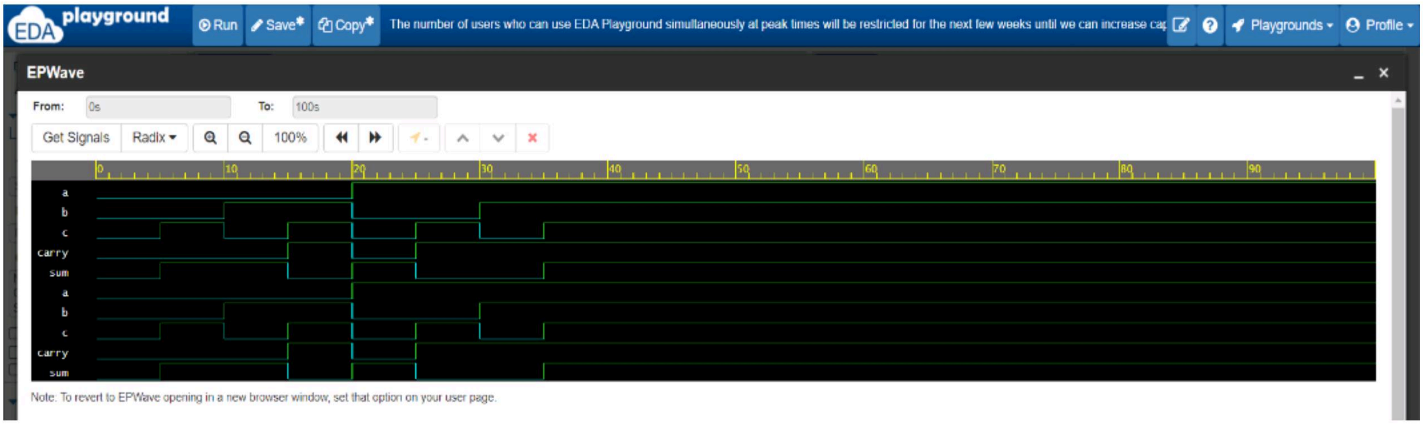
```
module full_adder_pavan(a,b,c,sum,carry);
  input a,b,c;
  output sum,carry;
  reg sum,carry;
  always @(a,b,c)
  begin
    if(a==1'b0 && b==1'b0 && c==1'b0)
      begin
        sum=0;
        carry=0;
      end
    else if((a==1'b0 && b==1'b1 && c=1'b1) || (a==1'b0 &&b==1'b1 && c==1'b0))
      begin
        sum=1;
        carry=0;
      end
    else if (a==1'b0 && b==1'b1 && c==1'b1)
      begin
        sum=0;
        carry=1;
      end
    else if (a==1'b1 &&1'b0 &&c==1'b0)
      begin
        sum=1;
        carry=0;
      end
    else if ((a==1'b1 && b==1'b0 &&c==1'b1) || (a==1'b1 && b==1b1 && c==1'b1))
      begin
        sum=0;
        carry=1;
      end
    else
      begin
        sum=1;
        carry=1;
      end
```

Output: -



```
[2023-02-28 04:47:03 EST] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
a=0,b=0,c=0;sum=0;carry=0
a=0,b=0,c=1;sum=1;carry=0
a=0,b=1,c=0;sum=1;carry=0
a=0,b=1,c=1;sum=0;carry=1
a=1,b=0,c=0;sum=1;carry=0
a=1,b=0,c=1;sum=0;carry=1
a=1,b=1,c=0;sum=0;carry=1
a=1,b=1,c=1;sum=1;carry=1
Finding VCD file...
./dump.vcd
[2023-02-28 04:47:04 EST] Opening EPWave...
Done
```

Wave Form: -



The number of users who can use EDA Playground simultaneously at peak times will be restricted for the next few weeks until we can increase cap

From: 0s

To: 100s

Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Observations:

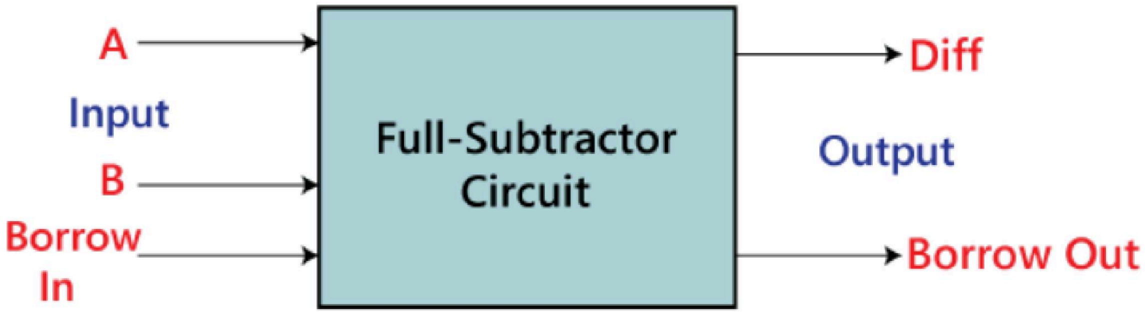
Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

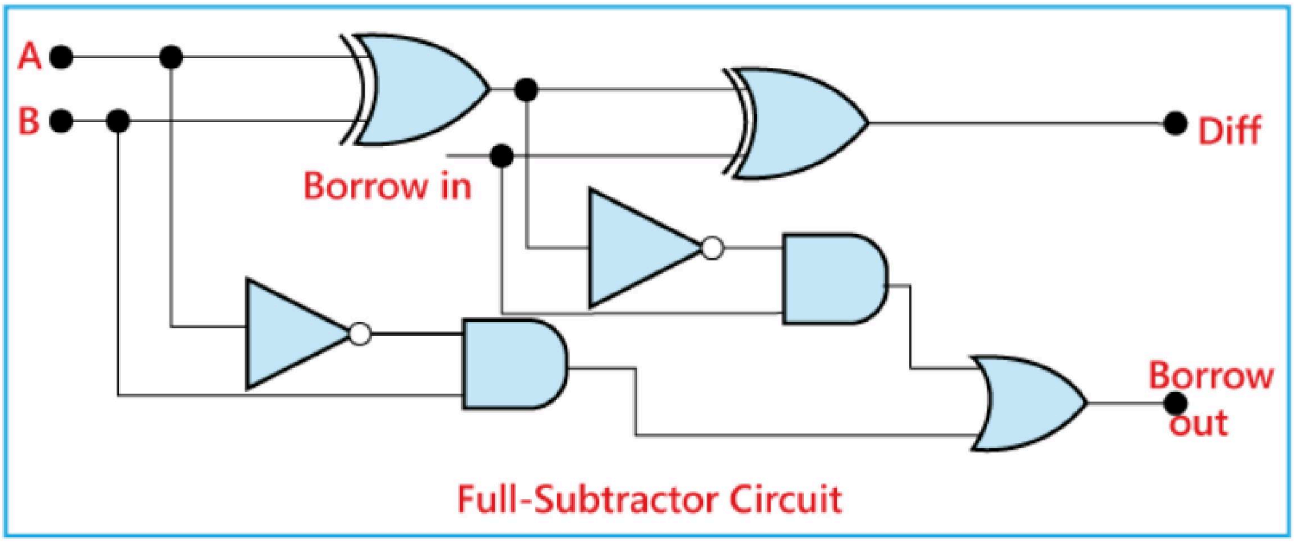
Full Subtractor

Objective: -Verification of Full Subtractor

Theorey: -Full Subtractor is a combinational logic gate

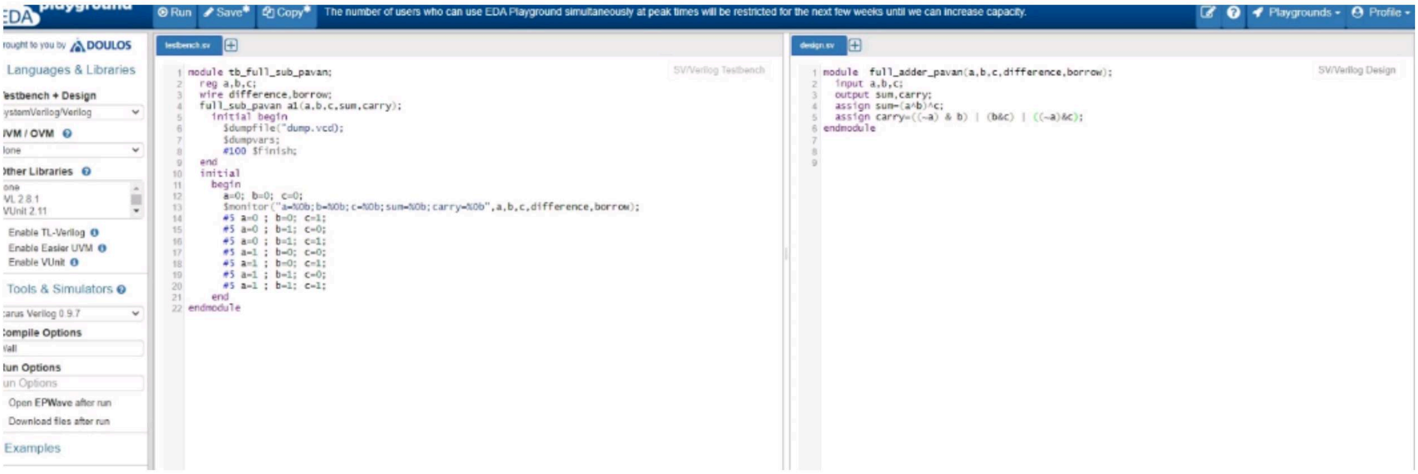
Block diagram:





Implementation: -

Dataflow:

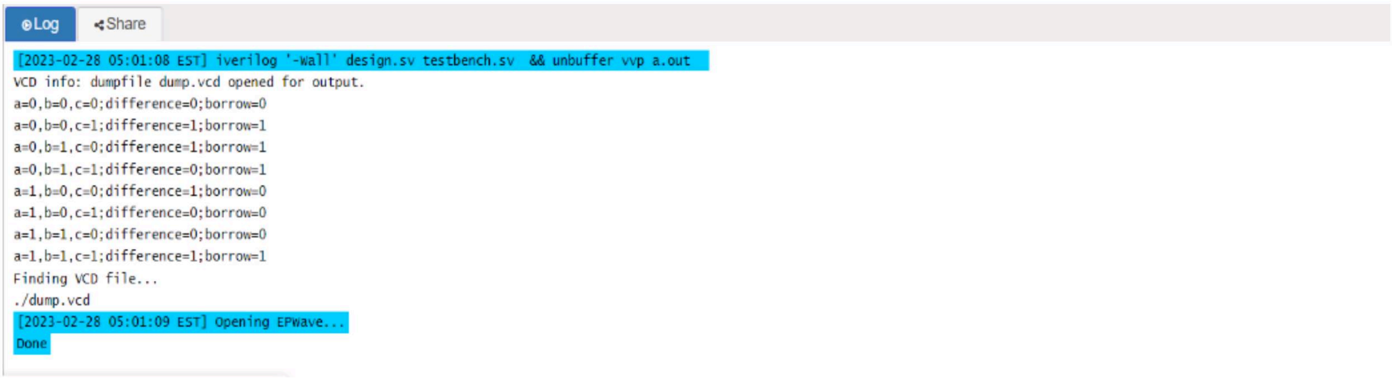


The number of users who can use EDA Playground simultaneously at peak times will be restricted for the next few weeks until we can increase capacity.

```
module tb_full_sub_pavan;
  reg a,b,c;
  wire difference,borrow;
  full_sub_pavan a1(a,b,c,sum,carry);
    initial begin
      $dumpfile("dump.vcd);
      $dumpvars;
      #100 $finish;
  end
  initial
    begin
      a=0; b=0; c=0;
      $monitor("a=%0b;b=%0b;c=%0b;sum=%0b;carry=%0b",a,b,c,difference,borrow);
      #5 a=0 ; b=0; c=1;
      #5 a=0 ; b=1; c=0;
      #5 a=0 ; b=1; c=1;
      #5 a=1 ; b=0; c=0;
      #5 a=1 ; b=0; c=1;
      #5 a=1 ; b=1; c=0;
      #5 a=1 ; b=1; c=1;
    end
endmodule
```

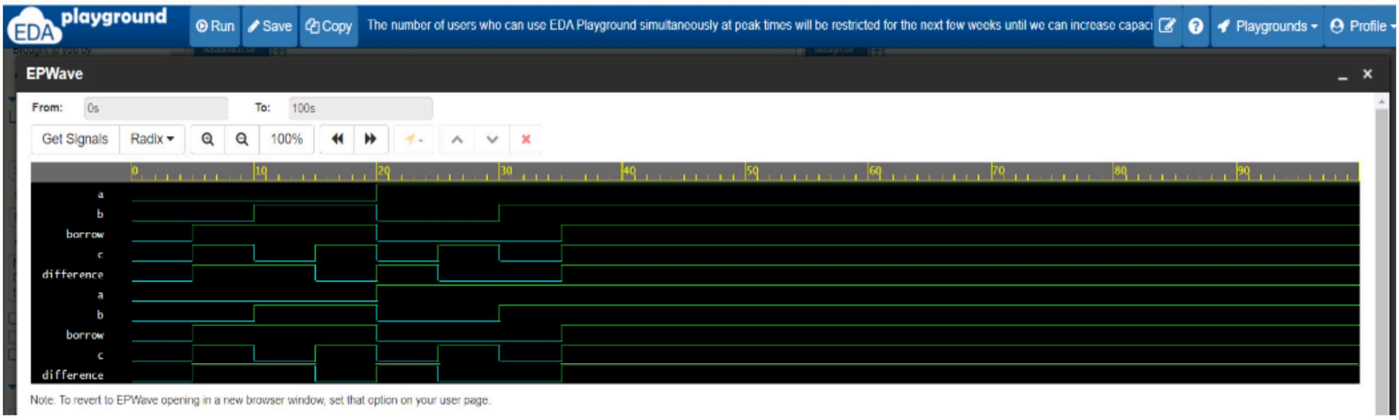
```
module  full_adder_pavan(a,b,c,difference,borrow);
  input a,b,c;
  output sum,carry;
  assign sum=(a^b)^c;
  assign carry=((~a) & b) | (b&c) | ((~a)&c);
endmodule
```

Output:



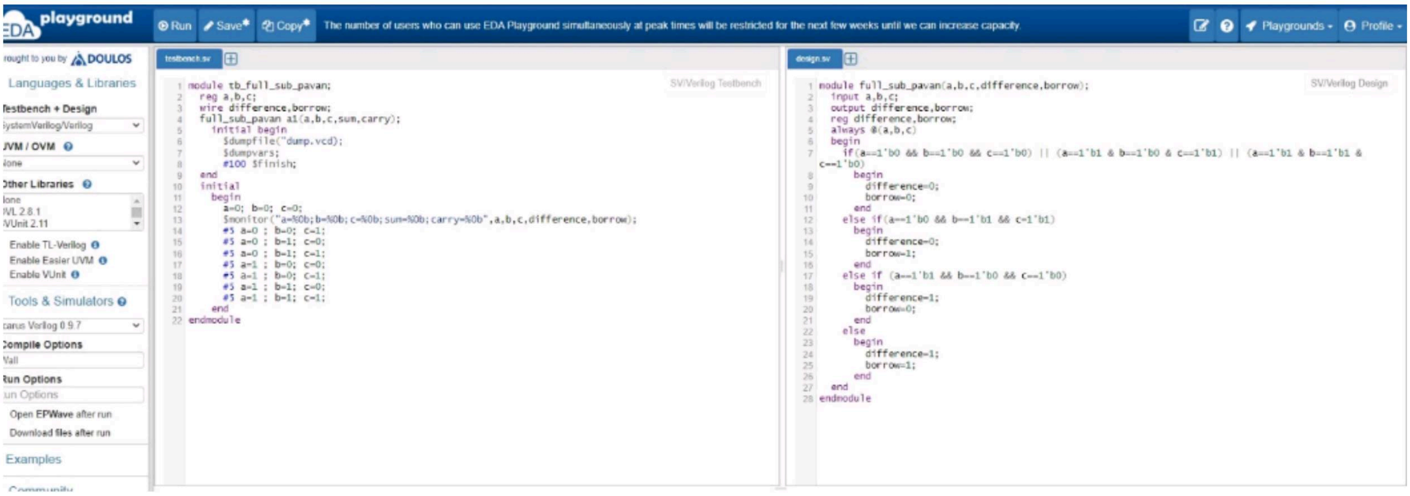
```
[2023-02-28 05:01:08 EST] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
a=0,b=0,c=0;difference=0;borrow=0
a=0,b=0,c=1;difference=1;borrow=1
a=0,b=1,c=0;difference=1;borrow=1
a=0,b=1,c=1;difference=0;borrow=1
a=1,b=0,c=0;difference=1;borrow=0
a=1,b=0,c=1;difference=0;borrow=0
a=1,b=1,c=0;difference=0;borrow=0
a=1,b=1,c=1;difference=1;borrow=1
Finding VCD file...
./dump.vcd
[2023-02-28 05:01:09 EST] Opening EPWave...
Done
```

Wave Form:



Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Behavioral:



estbench + Design: ystemVerilog/Verilog

JVM / OVM: Jone

Other Libraries: Jone, VL 2.8.1, VUnit 2.11

Enable TL-Verilog

Enable Easier UVM

Enable VUnit

carus Verilog 0.9.7

Compile Options: Wall

Run Options: un Options

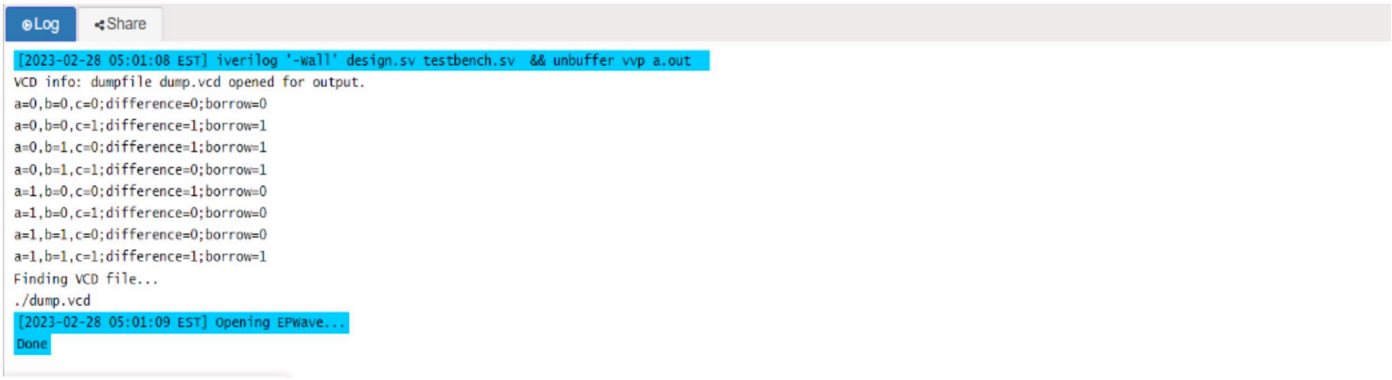
Open EPWave after run

Download files after run

```
module tb_full_sub_pavan;
  reg a,b,c;
  wire difference,borrow;
  full_sub_pavan a1(a,b,c,sum,carry);
    initial begin
      $dumpfile("dump.vcd);
      $dumpvars;
      #100 $finish;
  end
  initial
    begin
      a=0; b=0; c=0;
      $monitor("a=%0b;b=%0b; c=%0b; sum=%0b; carry=%0b",a,b,c,difference,borrow);
      #5 a=0 ; b=0; c=1;
      #5 a=0 ; b=1; c=0;
      #5 a=0 ; b=1; c=1;
      #5 a=1 ; b=0; c=0;
      #5 a=1 ; b=0; c=1;
      #5 a=1 ; b=1; c=0;
      #5 a=1 ; b=1; c=1;
    end
endmodule
```

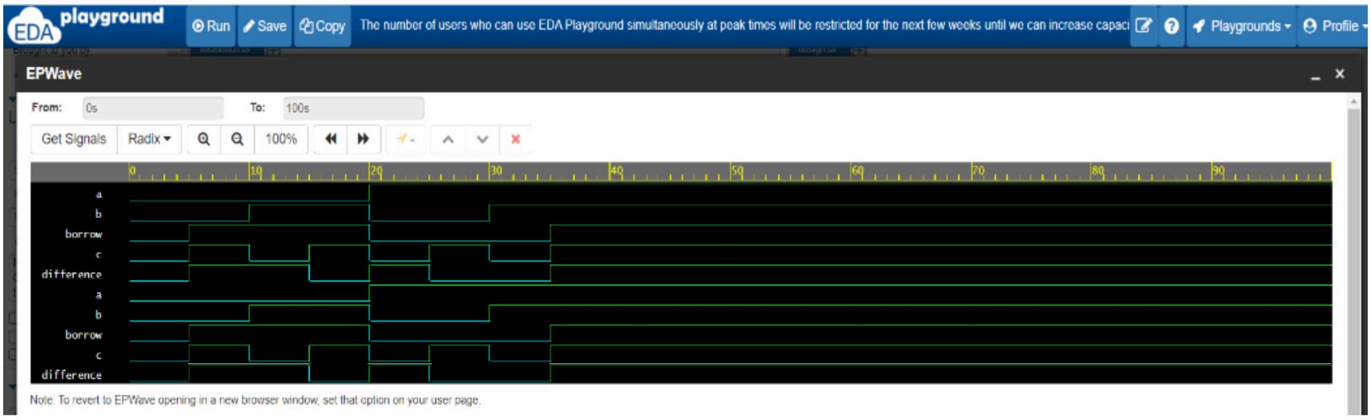
```
module full_sub_pavan(a,b,c,difference,borrow);
  input a,b,c;
  output difference,borrow;
  reg difference,borrow;
  always @(a,b,c)
  begin
    if(a==1'b0 && b==1'b0 && c==1'b0) || (a==1'b1 & b==1'b0 & c==1'b1) || (a==1'b1 & b==1'b1 &
c==1'b0)
      begin
        difference=0;
        borrow=0;
      end
    else if(a==1'b0 && b==1'b1 && c=1'b1)
      begin
        difference=0;
        borrow=1;
      end
    else if (a==1'b1 && b==1'b0 && c==1'b0)
      begin
        difference=1;
        borrow=0;
      end
    else
      begin
        difference=1;
        borrow=1;
      end
  end
endmodule
```

Output:



```
[2023-02-28 05:01:08 EST] iverilog '-Wall' design.sv testbench.sv  && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
a=0,b=0,c=0;difference=0;borrow=0
a=0,b=0,c=1;difference=1;borrow=1
a=0,b=1,c=0;difference=1;borrow=1
a=0,b=1,c=1;difference=0;borrow=1
a=1,b=0,c=0;difference=1;borrow=0
a=1,b=0,c=1;difference=0;borrow=0
a=1,b=1,c=0;difference=0;borrow=0
a=1,b=1,c=1;difference=1;borrow=1
Finding VCD file...
./dump.vcd
[2023-02-28 05:01:09 EST] Opening EPWave...
Done
```

Wave Form:



The number of users who can use EDA Playground simultaneously at peak times will be restricted for the next few weeks until we can increase capaci

From: 0s To: 100s

Note: To revert to EPWave opening in a new browser window, set that option on your user page.

Observations:

Inputs			Outputs	
A	B	Borrow$_{in}$	Diff	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1