ASIC 581 LAB1 REPORT

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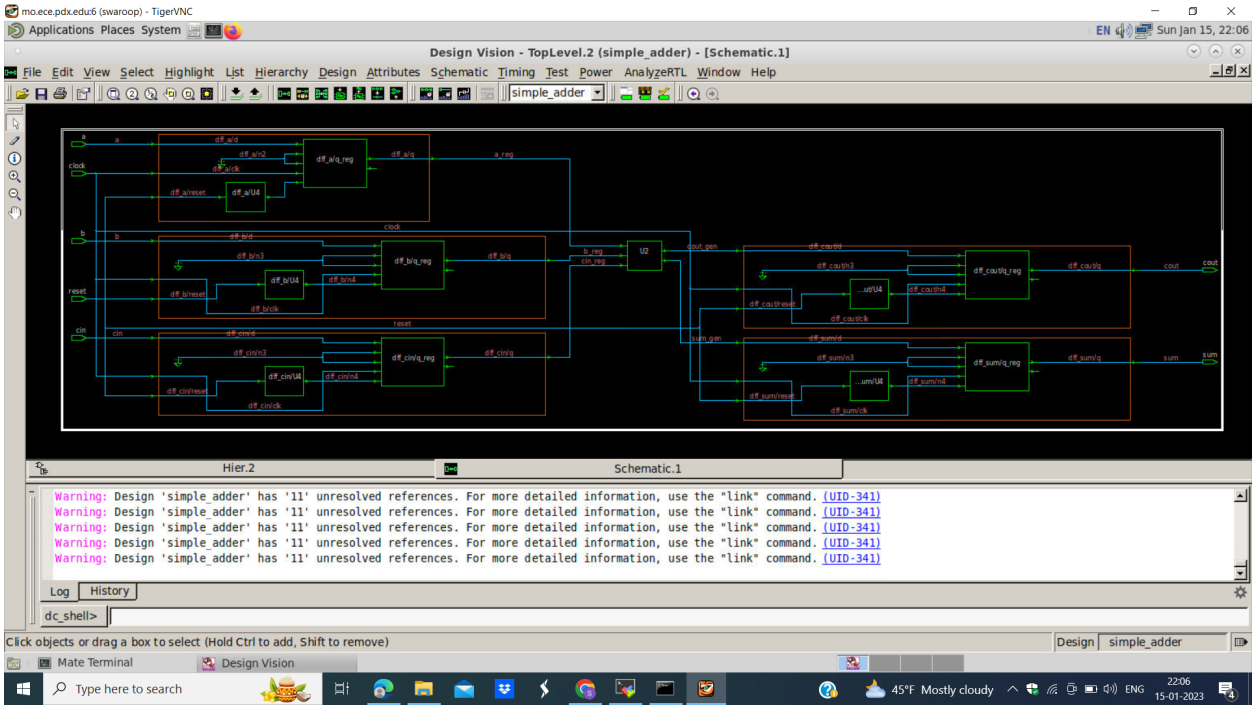
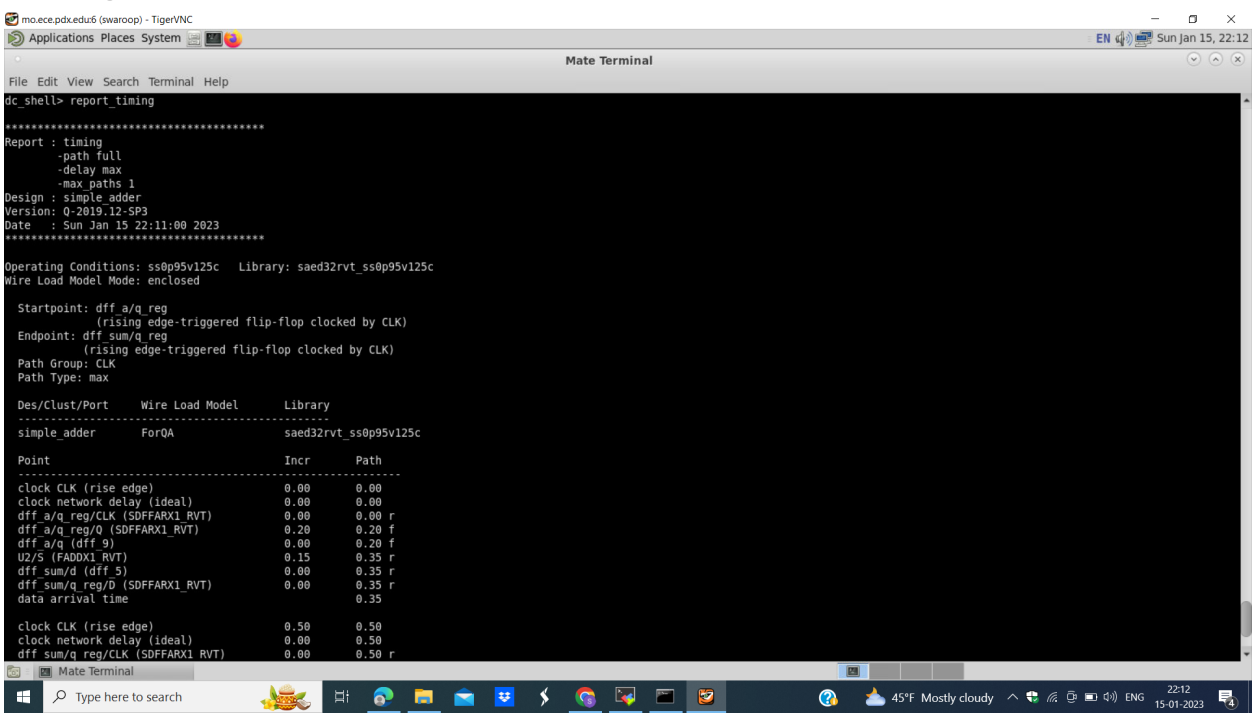
HW_LAB_1_A:

Snapshot of schematic circuit from DC:



Timing report from DC:



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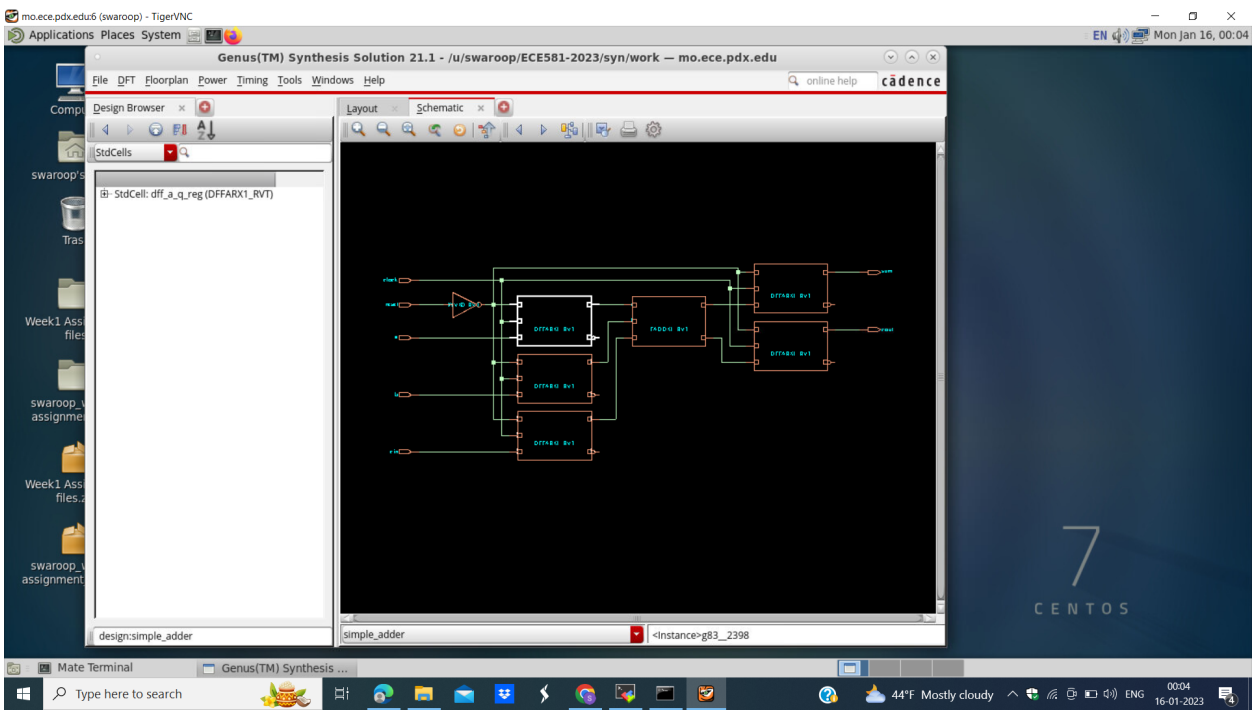
```
library setup time                          -0.12        0.38
data required time                                       0.38
-------------------------------------------------------------
data required time                                       0.38
data arrival time                                       -0.35
-------------------------------------------------------------
slack (MET)                                              0.03
```

HW_LAB_1_B:

Schematic from Genus:



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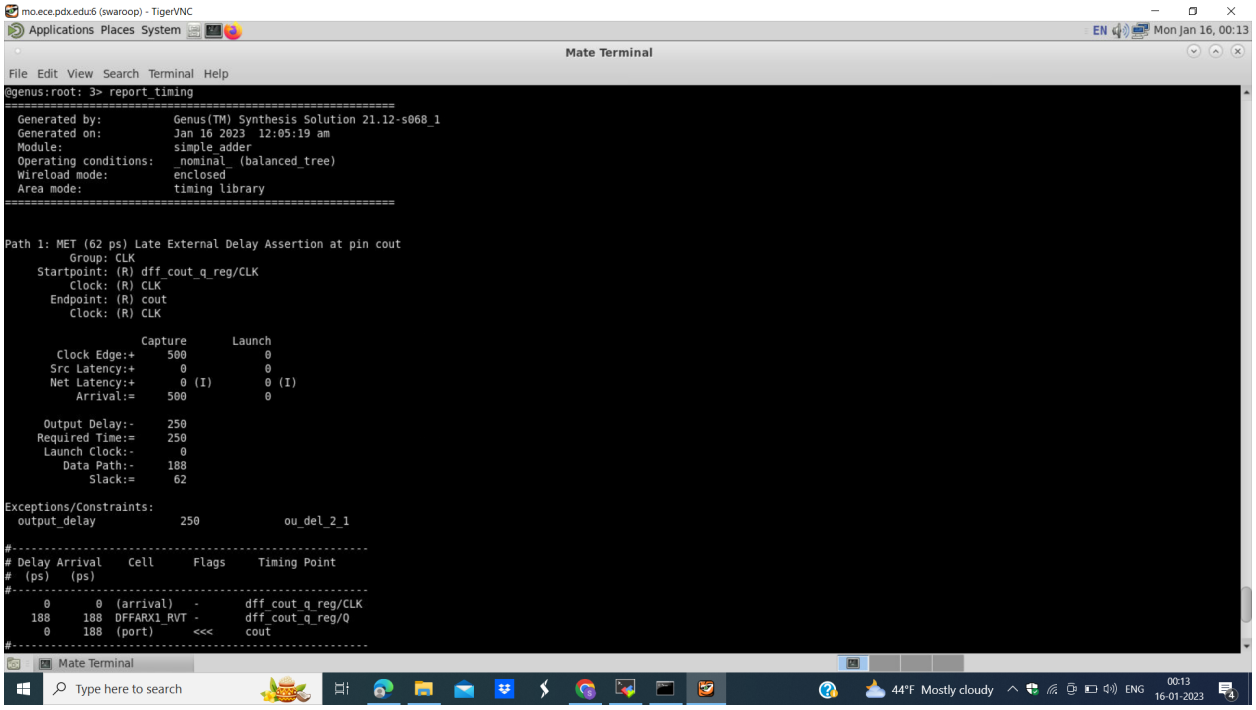
Timing report from Genus:



```
@genus:root: 3> report_timing
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.12-s068_1
  Generated on:           Jan 16 2023  12:05:19 am
  Module:                 simple_adder
  Operating conditions:   _nominal_ (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================


Path 1: MET (62 ps) Late External Delay Assertion at pin cout
          Group: CLK
     Startpoint: (R) dff_cout_q_reg/CLK
          Clock: (R) CLK
       Endpoint: (R) cout
          Clock: (R) CLK

                     Capture       Launch
        Clock Edge:+     500            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     500            0

      Output Delay:-     250
     Required Time:=     250
      Launch Clock:-       0
         Data Path:-     188
             Slack:=      62

Exceptions/Constraints:
  output_delay             250             ou_del_2_1

#-------------------------------------------------------
# Delay Arrival    Cell      Flags     Timing Point
#  (ps)   (ps)
#-------------------------------------------------------
      0       0  (arrival)   -       dff_cout_q_reg/CLK
    188     188  DFFARX1_RVT -       dff_cout_q_reg/Q
      0     188  (port)     <<<     cout
#-------------------------------------------------------
```

Area/Timing comparison :

	Synopsys	Cadence
Cell count	11	7
Combinational cell count	6	2
Sequential cell count	5	5
Area	56.928257	41.680
WNS	0	0
TNS	0	0
Violation count	0	0

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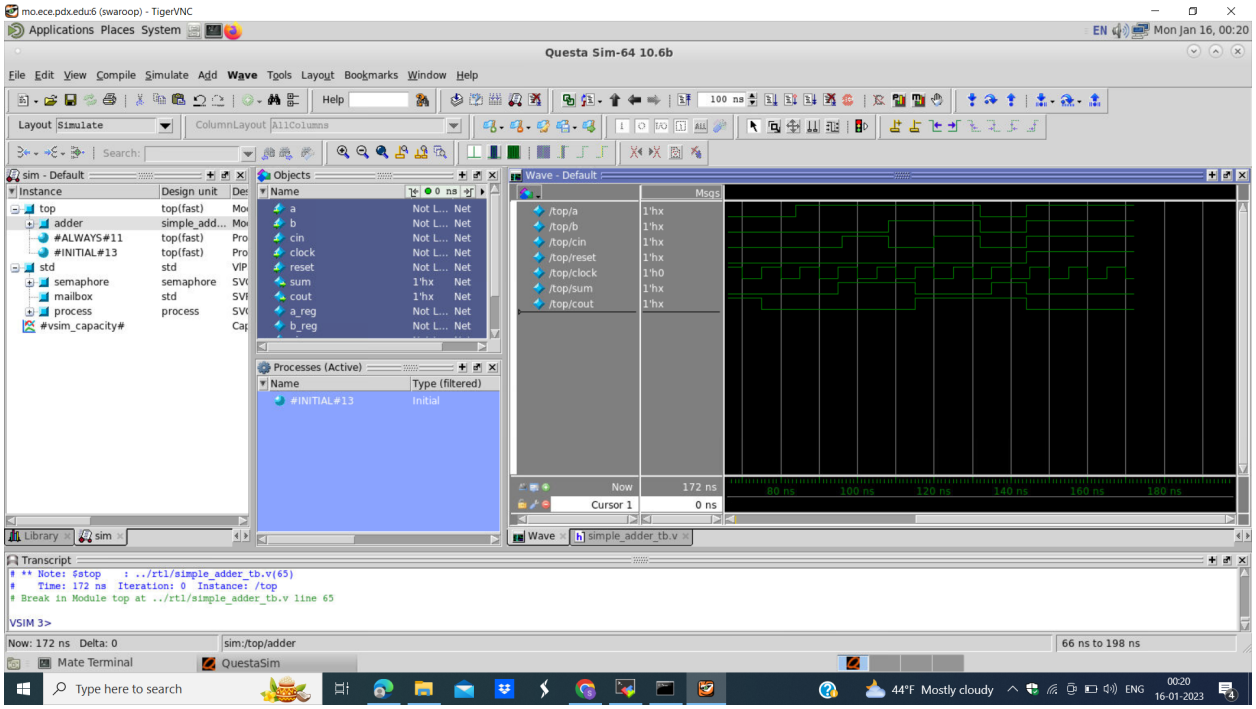
HW_LAB_1_C:

Questa FE waveforms:



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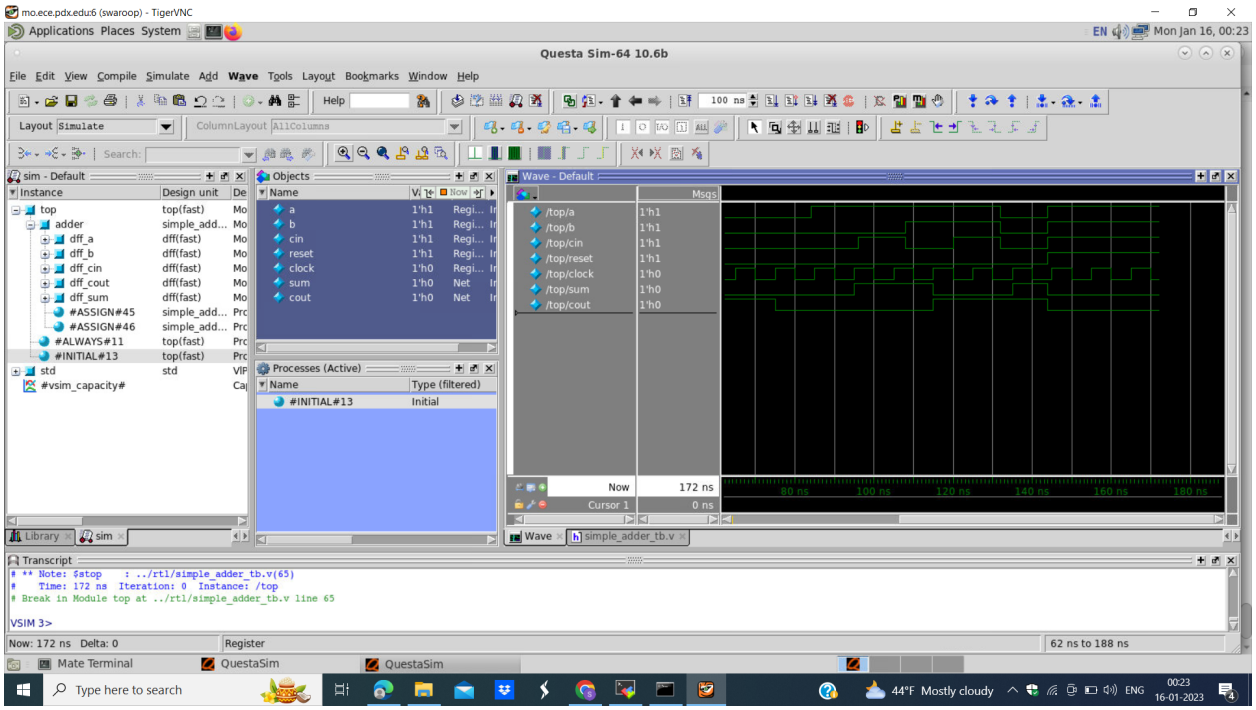
Questa BE waveforms:



Comparison statement between FE and BE:

Waveforms from both FE and BE are the same which implies the RTL and generated netlist has the same functionality.

Questa commands:

1)vlib - This creates the design library.
2)vmap - It defines the mapping between the logical library name and the directory.
3)vlog - This is used to compile the verilog source code into specified working library
4)vsim - This command is used to invoke the Questa simulator.

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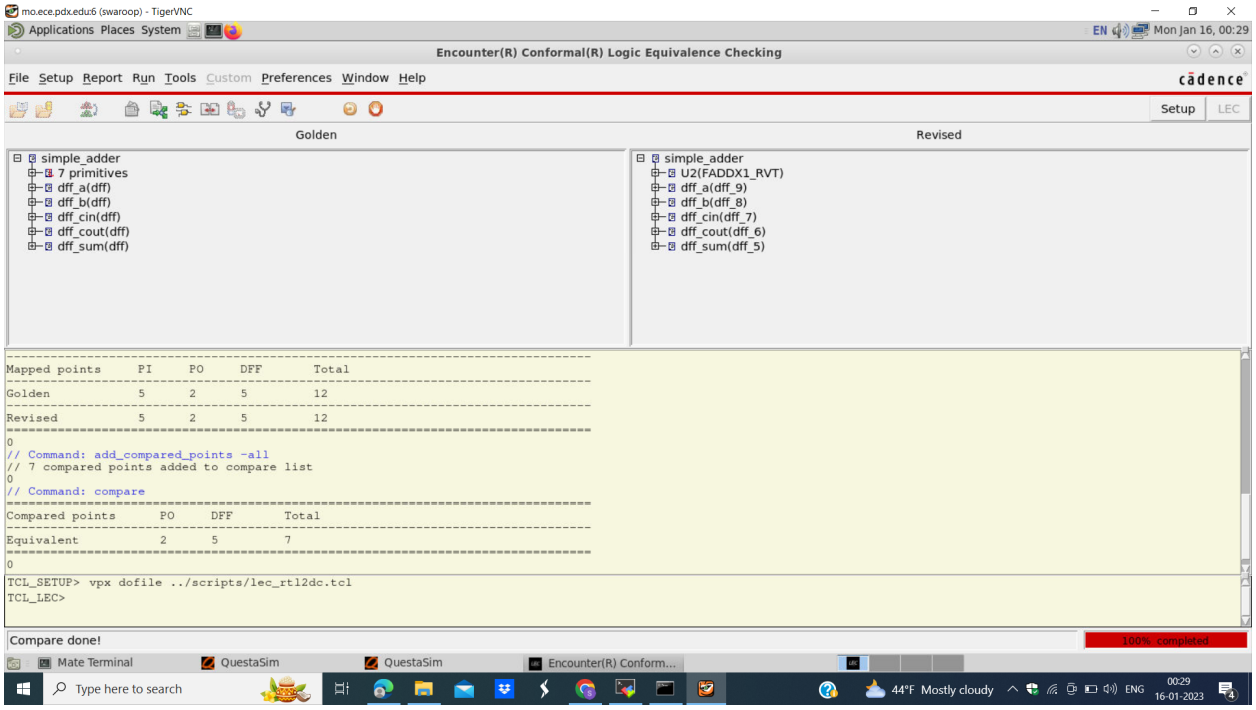
HW_LAB_1_D:

LEC picture:



LEC command description:

1)read_design : Reads the RTL and the netlist to be compared.
2)set_system mode lec: Compare mode for adding compare points and report compare results.
3)add_compared_points -all: This tells the LEC about what all points to be compared in both the designs.
4)compare: This performs the EC as per the above specified commands.