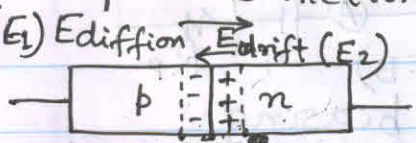
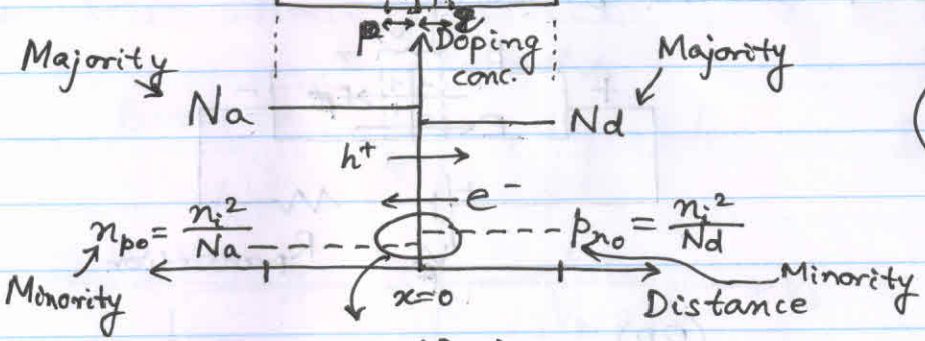
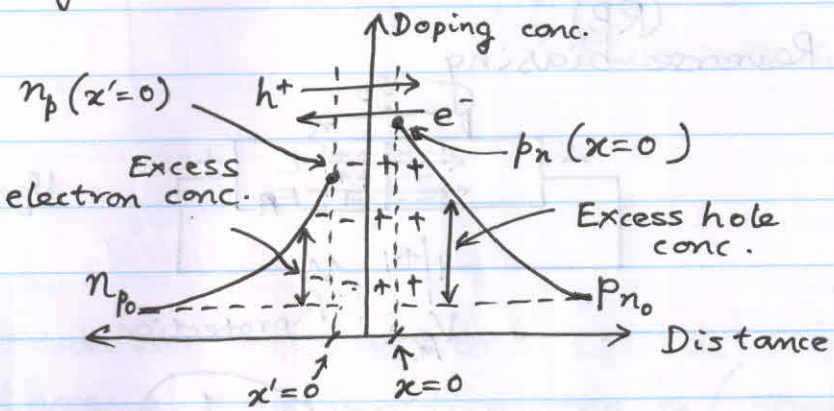
p-n Junction Diode



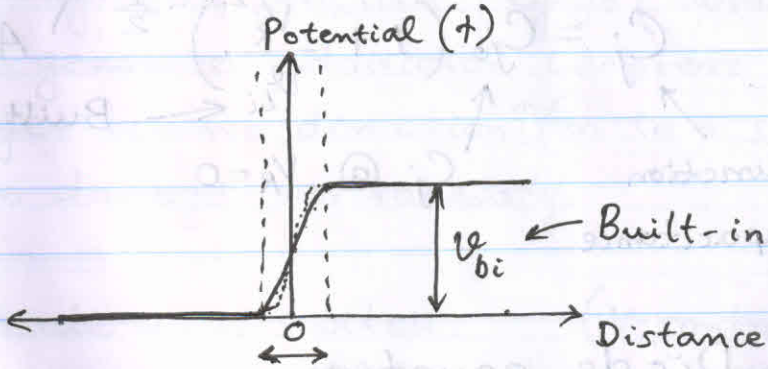
Symbol



(Majority & Minority Carriers)



(Minority Carriers)



(Potential Barrier)

$$V_{bi} = \frac{kT}{e}\ln\left(\frac{N_a N_d}{n_i^2}\right) = V_T \ln\left(\frac{N_a N_d}{n_i^2}\right)$$

, where, $\frac{kT}{q} = V_T$ ← Thermal V

→ Application of V or I

Biasing of a p-n junction:

1) Forward biasing
2) Reverse biasing

The positively charged region and the negatively charged region comprise the **space-charge** region, or **depletion region**, of the pn junction, in which there are essentially no mobile electrons or holes. Because of the electric field in the space-charge region, there is a potential difference across that region (Figure 1.11(b)). This potential difference is called the **built-in potential barrier**, or built-in voltage, and is given by

The potential difference, or built-in potential barrier, across the space-charge region cannot be measured by a voltmeter because new potential barriers form between the probes of the voltmeter and the semiconductor, canceling the effects of V_{bi}. In essence, V_{bi} maintains equilibrium, so no current is produced by this voltage. However, the magnitude of V_{bi} becomes important when we apply a forward-bias voltage, as discussed later in this chapter.

Forward Bias

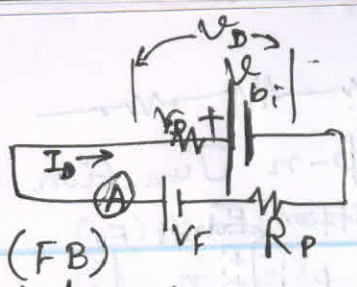
If a positive voltage v_D is applied to the p-region, the potential barrier decreases (Figure 1.15). The electric fields in the space-charge region are very large compared to those in the remainder of the p- and n-regions, so essentially all of the applied voltage exists across the pn junction region. The applied electric field, E_A, induced by the applied voltage is in the opposite direction from that of the thermal equilibrium space-charge E-field. However, the net electric field is *always* from the n- to the p-region. The net result is that the electric field in the space-charge region is lower than the equilibrium value. This upsets the delicate balance between diffusion and the E-field force. Majority carrier electrons from the n-region diffuse into the p-region, and majority carrier holes from the p-region diffuse into the n-region. The process continues as long as the voltage v_D is applied, thus creating a current in the pn junction. This process would be analogous to lowering a dam wall slightly. A slight drop in the wall height can send a large amount of water (current) over the barrier.

Reverse Bias

Assume a positive voltage is applied to the n-region of a pn junction, as shown in Figure 1.13. The applied voltage V_R induces an applied electric field, E_A, in the semiconductor. The direction of this applied field is the same as that of the E-field in the space-charge region. The magnitude of the electric field *in* the space-charge region increases above the thermal equilibrium value. This increased electric field holds back the holes in the p-region and the electrons in the n-region, so there is essentially no current across the pn junction. By definition, this applied voltage polarity is called **reverse bias.**

When the electric field in the space-charge region increases, the number of positive and negative charges must increase. If the doping concentrations are not changed, the increase in the fixed charge can only occur if the width W of the space-charge region increases. Therefore, with an increasing reverse-bias voltage V_R, space-charge width W also increases. This effect is shown in Figure 1.14.

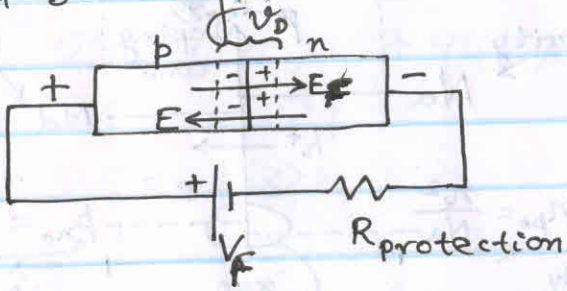
When a diode is reverse-biased by at least 0.1 V, the diode current is $i_D = -I_S$. The current is in the reverse direction and is a constant, hence the name reverse-bias saturation current. Real diodes, however, exhibit reverse-bias currents that are considerably larger than I_S. This additional current is called a generation current and is due to electrons and holes being generated within the space-charge region. Whereas a typical value of I_S may be 10^{-14} A, a typical value of reverse-bias current may be 10^{-9} A or 1 nA. Even though this current is much larger than I_S, it is still small and negligible in most cases.



$$I_D = \frac{V_F - V_{bi}}{R_P + r_D}$$

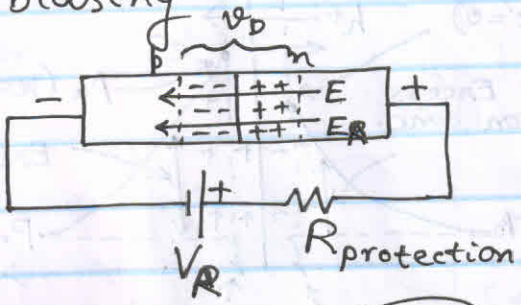
(FB)

1. Forward biasing



(RB)

2. Reverse biasing



$$v_D = V_R + \Delta V$$

$$C_j = C_{jo}\left(1 + \frac{V_R}{v_{bi}}\right)^{-\frac{1}{2}}$$

Applied V

Built-in potential

Junction Capacitance

C_j @ $V_R = 0$

3. Diode equation

$$i_D = I_S\left[e^{\frac{v_D}{nV_T}} - 1\right]$$

Diode Current

Reverse Bias Saturation Current

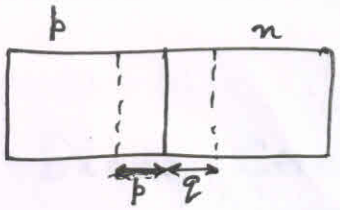
Emission Co-efficient or Ideality Factor

Thermal V $\left(\frac{kT}{q}\right)$

$V_T \cong 26$ mV @ 300K

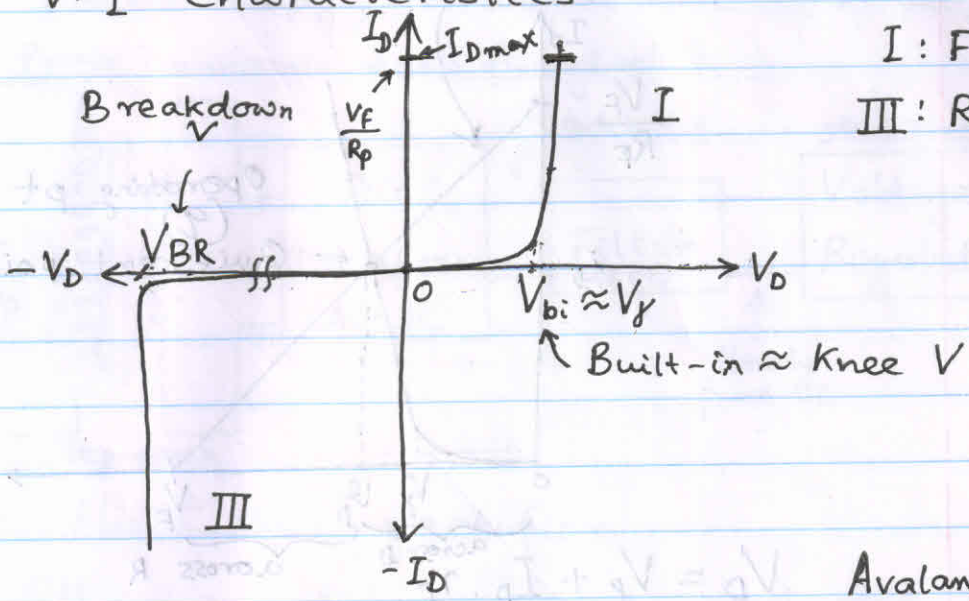
$n = 1$ to 2 (Generally = 1)

$I_S = 10^{-15}$ to 10^{-13} A



$p > q$

4. V-I characteristics



I : FB

III : RB

Avalanche Break-dn

Breakdown → Carriers collide while passing through the junction region (space charge region) and generates additional carriers, which causes larger reverse direction I (n to p sides), and thus damages permanently.

5. Diode as a switch.

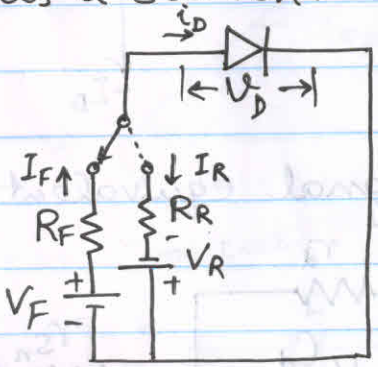
(V-controlled SW)

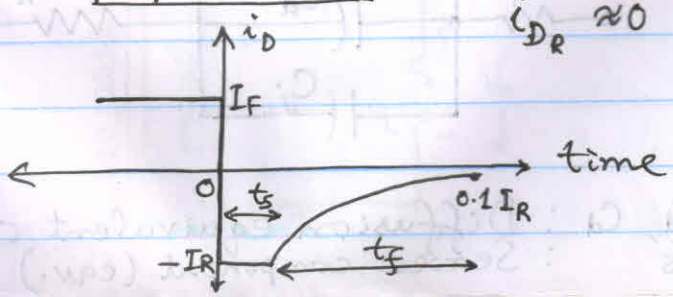
$i_{D_F} \approx 0$ (if $V_F \leq V_\gamma$)

$i_{D_F} = I_F = \frac{V_F - V_D}{R_F}$ (if $V_F > V_\gamma$)

$i_{D_R} = -I_R = -\frac{V_R}{R_R}$ (at breakdown)

$i_{D_R} \approx 0$ (not at brk-dn)





Temperature Effects

Since both I_S and V_T are functions of temperature, the diode characteristics also vary with temperature. The temperature-related variations in forward-bias characteristics are illustrated in Figure 1.20. For a given current, the required forward-bias voltage decreases as temperature increases. For silicon diodes, the change is approximately 2 mV/°C.

The parameter I_S is a function of the intrinsic carrier concentration n_i, which in turn is strongly dependent on temperature. Consequently, the value of I_S approximately doubles for every 5 °C increase in temperature. The actual reverse-bias diode current, as a general rule, doubles for every 10 °C rise in temperature. As an example of the importance of this effect, the relative value of n_i in germanium, is large, resulting in a large reverse-saturation current in germanium-based diodes. Increases in this reverse current with increases in the temperature make the germanium diode highly impractical for most circuit applications.

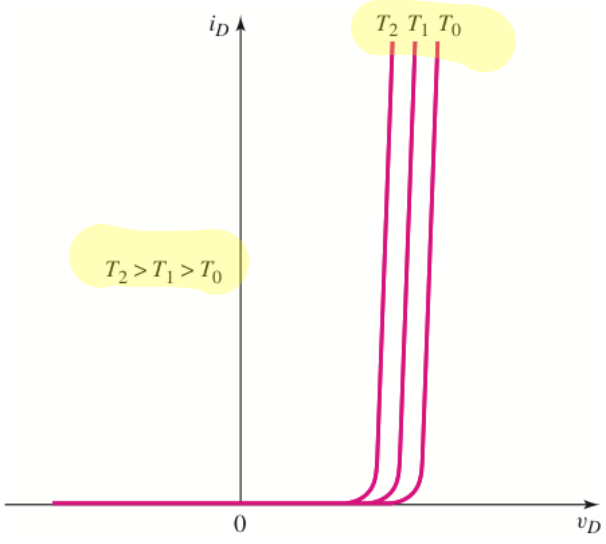


Figure 1.20 Forward-biased pn junction characteristics versus temperature. The required diode voltage to produce a given current decreases with an increase in temperature.

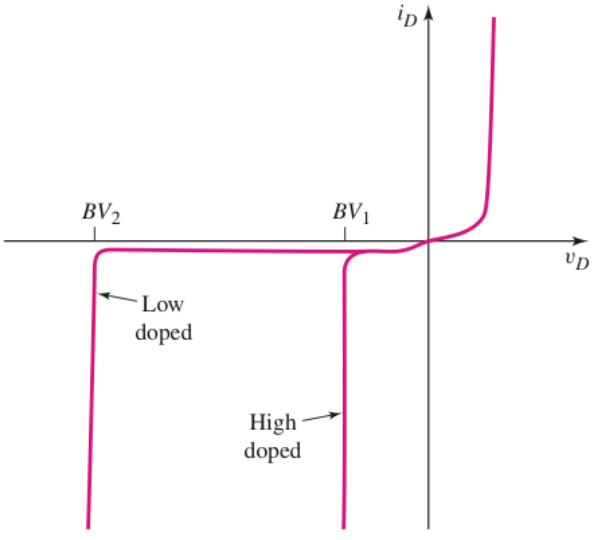


Figure 1.21 Reverse-biased diode characteristics showing breakdown for a low-doped pn junction and a high-doped pn junction. The reverse-bias current increases rapidly once breakdown has occurred.

Switching Transient

Since the pn junction diode can be used as an electrical switch, an important parameter is its transient response, that is, its speed and characteristics, as it is switched from one state to the other. Assume, for example, that the diode is switched from the forward-bias "on" state to the reverse-bias "off" state. Figure 1.23 shows a simple circuit that will switch the applied voltage at time $t = 0$. For $t < 0$, the forward-bias current i_D is

$$i_D = I_F = \frac{V_F - v_D}{R_F} \tag{1.19}$$

The minority carrier concentrations for an applied forward-bias voltage and an applied reverse-bias voltage are shown in Figure 1.24. Here, we neglect the change in the space charge region width. When a forward-bias voltage is applied, excess minority carrier charge is stored in both the p- and n-regions. The excess charge is the difference between the minority carrier concentrations for a forward-bias voltage and those for a reverse-bias voltage as indicated in the figure. This charge must be removed when the diode is switched from the forward to the reverse bias.

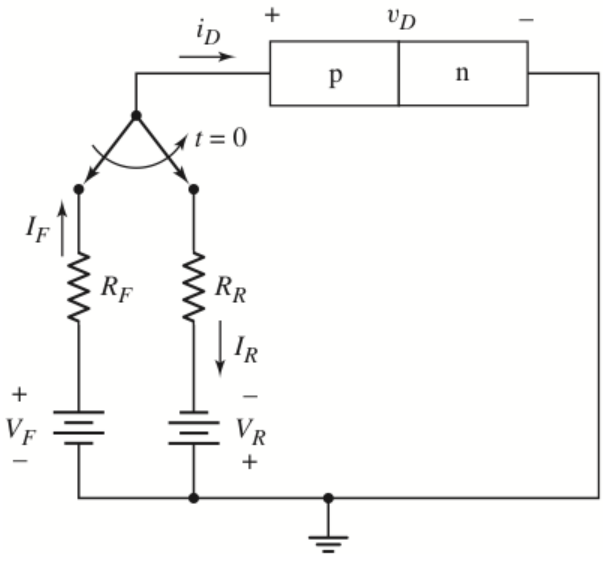


Figure 1.23 Simple circuit for switching a diode from forward to reverse bias

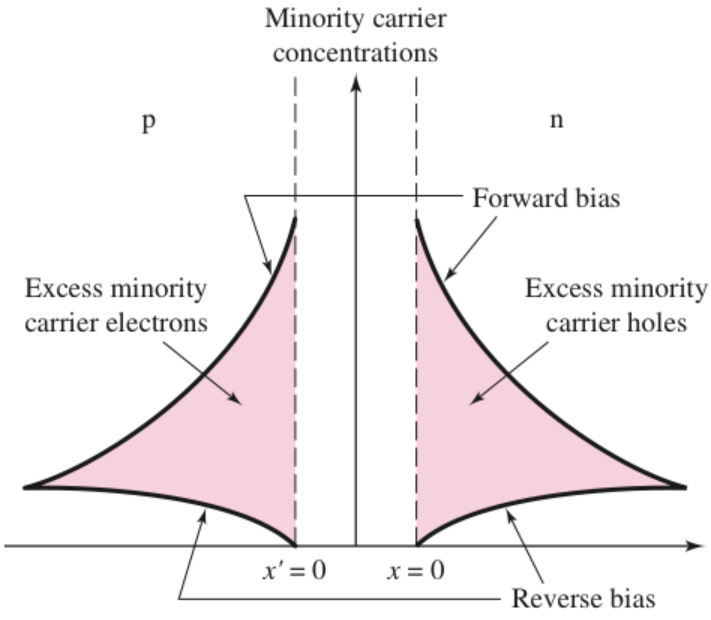


Figure 1.24 Stored excess minority carrier charge under forward bias compared to reverse bias. This charge must be removed as the diode is switched from forward to reverse bias.

As the forward-bias voltage is removed, relatively large diffusion currents are created in the reverse-bias direction. This happens because the excess minority carrier electrons flow back across the junction into the n-region, and the excess minority carrier holes flow back across the junction into the p-region.

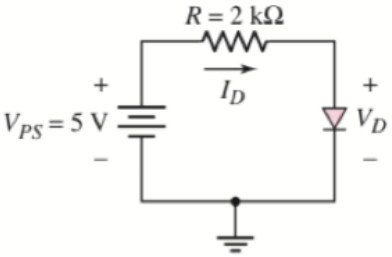


Figure 1.28 A simple diode circuit

Comment: Once the diode voltage is known, the current can also be determined from the ideal diode equation. However, dividing the voltage difference across a resistor by the resistance is usually easier, and this approach is used extensively in the analysis of diode and transistor circuits.

EXERCISE PROBLEM

Ex 1.8: Consider the circuit in Figure 1.28. Let $V_{PS} = 4$ V, $R = 4$ kΩ, and $I_S = 10^{-12}$ A. Determine V_D and I_D, using the ideal diode equation and the iteration method. (Ans. $V_D = 0.535$ V, $I_D = 0.866$ mA)

Graphical Approach

$$I_D = \frac{V_{PS}}{R} - \frac{V_D}{R}$$

which was also given by Equation (1.21(b)). This equation gives a linear relation between the diode current I_D and the diode voltage V_D for a given power supply voltage V_{PS} and resistance R. This equation is referred to as the circuit **load line,** and is usually plotted on a graph with the current I_D as the vertical axis and the voltage V_D as the horizontal axis.

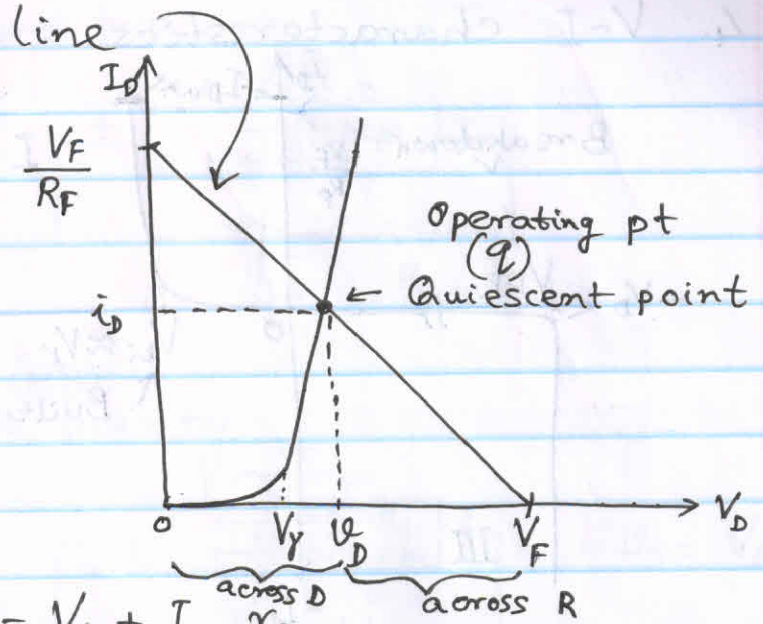
From Equation (1.21(b)), we see that if $I_D = 0$, then $V_D = V_{PS}$ which is the horizontal axis intercept. Also from this equation, if $V_D = 0$, then $I_D = V_{PS}/R$ which is the vertical axis intercept. The load line can be drawn between these two points. From Equation (1.21(b)), we see that the slope of the load line is $-1/R$.

Using the values given in Example (1.8), we can plot the straight line shown in Figure 1.29. The second plot in the figure is that of Equation (1.22), which is the ideal diode equation relating the diode current and voltage. The intersection of the load line and the device characteristics curve provides the dc current $I_D \approx 2.2$ mA through the diode and the dc voltage $V_D \approx 0.62$ V across the diode. This point is referred to as the **quiescent point,** or the ***Q*-point.**

The graphical analysis method can yield accurate results, but it is somewhat cumbersome. However, the concept of the load line and the graphical approach are useful for "visualizing" the response of a circuit, and the load line is used extensively in the evaluation of electronic circuits.

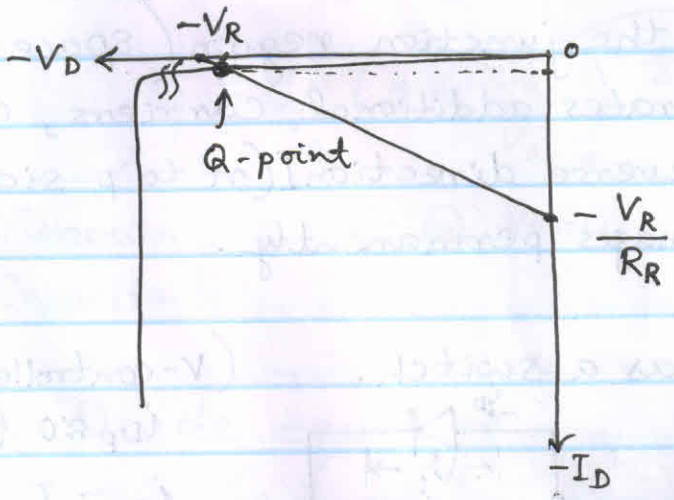
$$I_D = I_S\left[e^{\left(\frac{V_D}{V_T}\right)} - 1\right] \qquad (1.22)$$

5. Load line

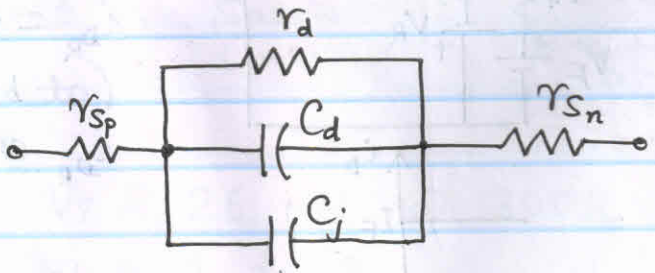


$$V_D = V_\gamma + I_D \cdot r_f$$

$$P_D = I_D \cdot V_D$$



6. Small signal equivalent ckt.



r_d, C_d : Diffusion equivalent components
r_s : Series component (eqv.)