

Finite Output Resistance

In the ideal case, when a MOSFET is biased in the saturation region, the drain current i_D is independent of drain-to-source voltage v_{DS} . However, in actual MOSFET i_D versus v_{DS} characteristics, a nonzero slope does exist beyond the saturation point. For $v_{DS} > v_{DS}(\text{sat})$, the actual point in the channel at which the inversion charge goes to zero moves away from the drain terminal (see Figure 3.9(d)). The effective channel length decreases, producing the phenomenon called **channel length modulation**.

An exaggerated view of the current–voltage characteristics is shown in Figure 3.20. The curves can be extrapolated so that they intercept the voltage axis at a point $v_{DS} = -V_A$. The voltage V_A is usually defined as a positive quantity. The slope of the curve in the saturation region can be described by expressing the i_D versus v_{DS} characteristic in the form, for an n-channel device,

$$i_D = K_n[(v_{GS} - V_{TN})^2(1 + \lambda v_{DS})] \quad (3.7)$$

where λ is a positive quantity called the channel-length modulation parameter.

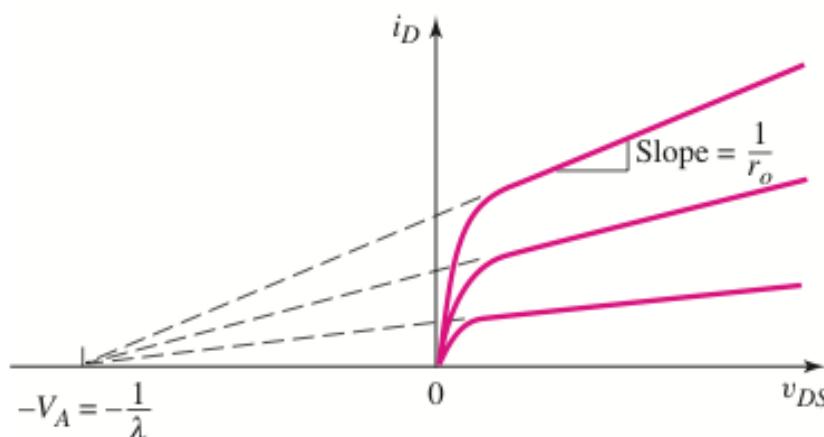


Figure 3.20 Family of i_D versus v_{DS} curves showing the effect of channel length modulation producing a finite output resistance

The output resistance due to the channel length modulation is defined as

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}} \right)^{-1} \Bigg|_{v_{GS}=\text{const.}} \quad (3.8)$$

From Equation (3.7), the output resistance, evaluated at the Q -point, is

$$r_o = [\lambda K_n (V_{GSQ} - V_{TN})^2]^{-1} \quad (3.9(a))$$

or

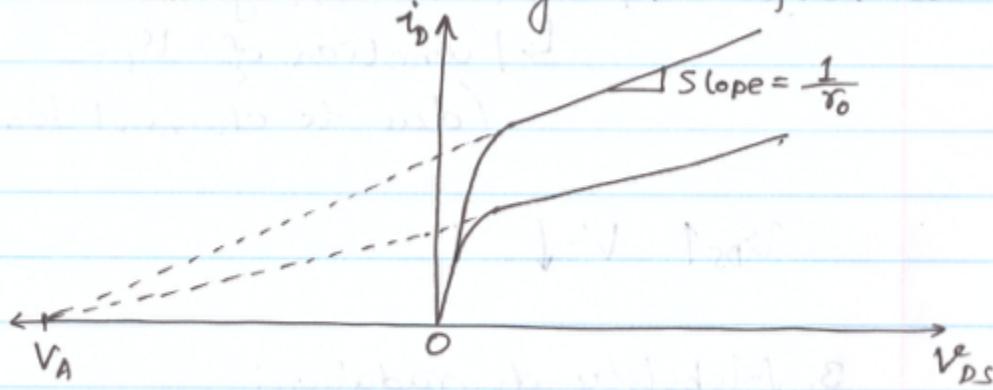
$$r_o \cong [\lambda I_{DQ}]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}} \quad (3.9(b))$$

Advantages of CMOS or MOSFETs

1. Compact
2. Low power
3. Robust
4. High density fabrication.

b. Non-ideal MOSFET characteristics:

i) V-I characteristics gets modified due to V_A .



In saturation region,

$$i_D = K_n [(V_{as} - V_{Tn})^2 \cdot (1 + \lambda \cdot V_{DS})]$$

where,

$\lambda \Rightarrow$ Channel length modulation parameter.

Use $(\frac{\partial i_D}{\partial V_{DS}})^{-1}$

$$r_0 = \frac{1}{\lambda \cdot I_{DQ}} = \frac{V_A}{I_{DQ}} \quad (\text{O/P resistance})$$

$$V_A = \frac{1}{\lambda}$$

ii) Short channel effects:

1. Velocity saturation.

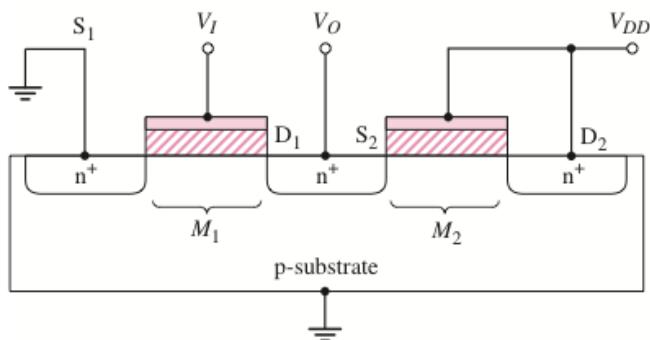
$V_{DS} \uparrow E_{DS} \uparrow$ Velocity of carrier \uparrow

(horizontal)

(upto a limit of V_{DS})

Another effect that occurs in short-channel devices is velocity saturation. As the horizontal electric field increases, the velocity of the carriers reaches a constant value and will no longer increase with an increase in drain voltage. Velocity saturation will lower the $V_{DS}(\text{sat})$ voltage value. The drain current will reach its saturation value at a smaller V_{DS} voltage. The drain current also becomes approximately a linear function of the gate voltage in the saturation region rather than the quadratic function of gate voltage in the long-channel characteristics.

Body Effect



When the two transistors are conducting, there is a nonzero drain-to-source voltage on M_1 , which means that the source of M_2 is not at the same potential as the substrate. These bias conditions mean that a zero or reverse-bias voltage exists across the source-substrate pn junction, and a change in the source-substrate junction voltage changes the threshold voltage. This is called the **body effect**. The same situation exists in p-channel devices.

Subthreshold Conduction

If we consider the ideal current-voltage relationship for the n-channel MOSFET biased in the saturation region, we have, from Equation (3.2(b)),

$$i_D = K_n(v_{GS} - V_{TN})^2$$

Taking the square root of both sides of the equation, we obtain

$$\sqrt{i_D} = \sqrt{K_n(v_{GS} - V_{TN})} \quad (3.11)$$

From Equation (3.11), we see that $\sqrt{i_D}$ is a linear function of v_{GS} . Figure 3.23 shows a plot of this ideal relationship.

Also plotted in Figure 3.23 are experimental results, which show that when v_{GS} is slightly less than V_{TN} , the drain current is not zero, as previously assumed. This current is called the **subthreshold current**. The effect may not be significant for a single device, but if thousands or millions of devices on an integrated circuit are biased just slightly below the threshold voltage, the power supply current will not be zero but may contribute to significant power dissipation in the integrated circuit.

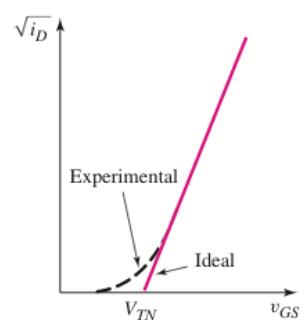
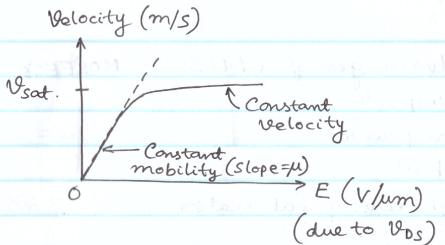


Figure 3.23 Plot of $\sqrt{i_D}$ versus v_{GS} for a MOSFET biased in the saturation region showing subthreshold conduction. Experimentally, a subthreshold current exists even for $v_{GS} < V_{TN}$.



2. Threshold voltage variation:

- $V_T \rightarrow$ Function of 'L' (directly proportional)
- \rightarrow Function of V_{DS} (due to channel length modulation)

$$V_{DS} \uparrow \quad V_T \downarrow$$

3. Mobility degradation:

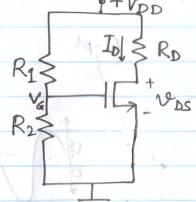
$$\frac{V_{GS}}{V_{SG}} \uparrow \quad E_{\text{vertical}} \uparrow \quad \mu \downarrow$$

(related to velocity saturation).

iii) Body effect & Substrate biasing:

A single substrate is shared among multiple MOSFETs (e.g. two n-ch). This causes threshold voltage variation in some MOSFETs as compared to others of same type.

i) Common source (DC) ckt:

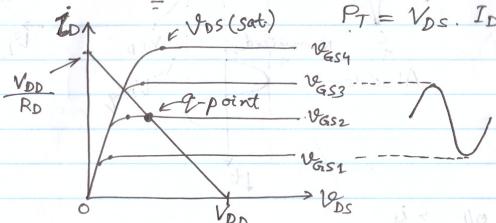


$$V_G = V_{GS} = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$$

$$I_D = K_n (V_{GS} - V_{Tn})^2 \quad (\text{Saturation})$$

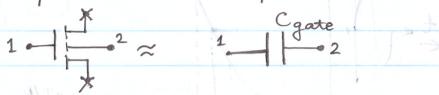
$$V_{DS} = V_{DD} - I_D \cdot R_D$$

$$P_T = V_{DS} \cdot I_D$$

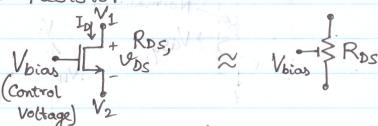


j) MOSFET as other electrical components:

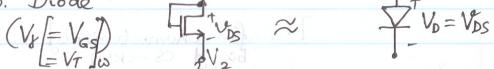
1. Capacitor: MOS capacitor



2. Resistor



3. Diode



3.3.1

NMOS Inverter

The MOSFET can be used as a switch in a wide variety of electronic applications. The transistor switch provides an advantage over mechanical switches in both speed and reliability. The transistor switch considered in this section is also called an inverter. Two other switch configurations, the NMOS transmission gate and the CMOS transmission gate, are discussed in Chapter 16.

Figure 3.45 shows the n-channel enhancement-mode MOSFET inverter circuit. If $v_I < V_{TN}$, the transistor is in cutoff and $i_D = 0$. There is no voltage drop across R_D , and the output voltage is $v_O = V_{DD}$. Also, since $i_D = 0$, no power is dissipated in the transistor.

If $v_I > V_{TN}$, the transistor is on and initially is biased in the saturation region, since $v_{DS} > v_{GS} - V_{TN}$. As the input voltage increases, the drain-to-source voltage

decreases, and the transistor eventually becomes biased in the nonsaturation region.

When $v_I = V_{DD}$, the transistor is biased in the nonsaturation region, v_O reaches a minimum value, and the drain current reaches a maximum value. The current and voltage are given by

$$i_D = K_n [2(v_I - V_{TN})v_O - v_O^2] \quad (3.26)$$

and

$$v_O = V_{DD} - i_D R_D \quad (3.27)$$

where $v_O = v_{DS}$ and $v_I = v_{GS}$.

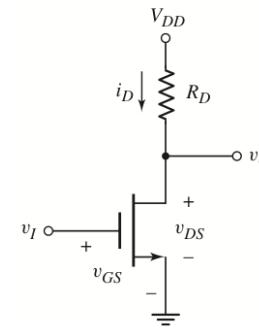
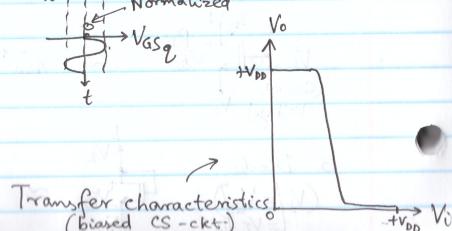
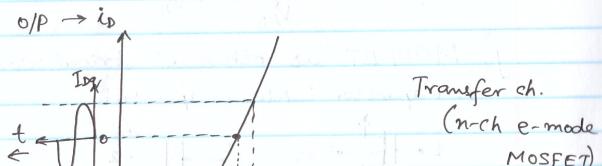
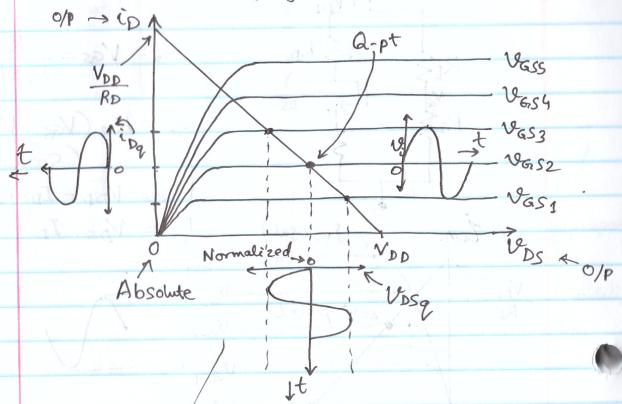


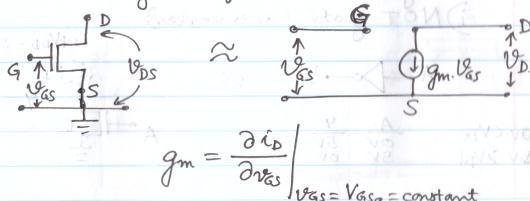
Figure 3.45 NMOS inverter circuit

k. MOSFET amplifier: Common Source



$$V_O = V_{DD} - i_D \cdot R_D$$

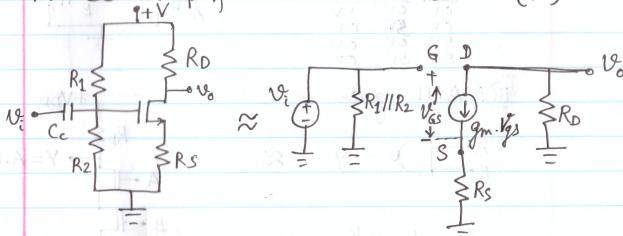
l. Small signal equivalent ckt: AC



$$g_m = \frac{\partial i_D}{\partial v_{as}} \quad |_{V_{as} = V_{GSQ}}$$

$$g_m = 2 \sqrt{K_n \cdot I_{DQ}} = 2 \cdot K_n (V_{GSQ} - V_{Tn})$$

m. CS amplifier with S-resistor(R_S)



$$V_O = -g_m \cdot V_{GS} \cdot R_D$$

$$V_i = V_{GS} + (g_m \cdot V_{GS}) R_S = V_{GS} (1 + g_m \cdot R_S)$$

$$A_V = \frac{V_O}{V_i} = \frac{-g_m \cdot R_D}{1 + g_m \cdot R_S} \approx -\frac{R_D}{R_S}$$

($\because g_m$ is large)

CS Amplifier

From Figure 4.1, we see that the instantaneous gate-to-source voltage is

$$v_{GS} = V_{GSQ} + v_i = V_{GSQ} + v_{gs} \quad (4.1)$$

where V_{GSQ} is the dc component and v_{gs} is the ac component. The instantaneous drain current is

$$i_D = K_n(v_{GS} - V_{TN})^2 \quad (4.2)$$

Substituting Equation (4.1) into (4.2) produces

$$i_D = K_n[V_{GSQ} + v_{gs} - V_{TN}]^2 = K_n[(V_{GSQ} - V_{TN}) + v_{gs}]^2 \quad (4.3(a))$$

or

$$i_D = K_n(V_{GSQ} - V_{TN})^2 + 2K_n(V_{GSQ} - V_{TN})v_{gs} + K_n v_{gs}^2 \quad (4.3(b))$$

The first term in Equation (4.3(b)) is the dc or quiescent drain current I_{DQ} , the second term is the time-varying drain current component that is linearly related to the signal v_{gs} , and the third term is proportional to the square of the signal voltage. For a sinusoidal input signal, the squared term produces undesirable harmonics, or nonlinear distortion, in the output voltage. To minimize these harmonics, we require

$$v_{gs} \ll 2(V_{GSQ} - V_{TN}) \quad (4.4)$$

which means that the third term in Equation (4.3(b)) will be much smaller than the second term. *Equation (4.4) represents the small-signal condition that must be satisfied for linear amplifiers.*

Neglecting the v_{gs}^2 term, we can write Equation (4.3(b)) as

$$i_D = I_{DQ} + i_d \quad (4.5)$$

Again, small-signal implies linearity so that the total current can be separated into a dc component and an ac component. The ac component of the drain current is given by

$$i_d = 2K_n(V_{GSQ} - V_{TN})v_{gs} \quad (4.6)$$

The small-signal drain current is related to the small-signal gate-to-source voltage by the transconductance g_m . The relationship is

$$g_m = \frac{i_d}{v_{gs}} = 2K_n(V_{GSQ} - V_{TN}) \quad (4.7)$$

The transconductance is a transfer coefficient relating output current to input voltage and can be thought of as representing the gain of the transistor.

The transconductance can also be obtained from the derivative

$$g_m = \left. \frac{\partial i_D}{\partial v_{GS}} \right|_{v_{GS}=V_{GSQ}=\text{const.}} = 2K_n(V_{GSQ} - V_{TN}) \quad (4.8(a))$$

which can be written as

$$g_m = 2\sqrt{K_n I_{DQ}} \quad (4.8(b))$$

The drain current versus gate-to-source voltage for the transistor biased in the saturation region is given in Equation (4.2) and is shown in Figure 4.3. The transconductance g_m is the slope of the curve. If the time-varying signal v_{gs} is sufficiently small, the transconductance g_m is a constant. With the Q -point in the saturation region, the transistor operates as a current source that is linearly controlled by v_{gs} . If the Q -point moves into the nonsaturation region, the transistor no longer operates as a linearly controlled current source.

As shown in Equation (4.8(a)), the transconductance is directly proportional to the conduction parameter K_n , which in turn is a function of the width-to-length ratio. Therefore, increasing the width of the transistor increases the transconductance, or gain, of the transistor.

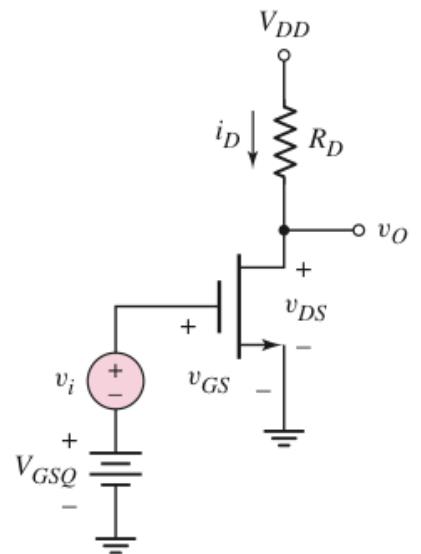


Figure 4.1 NMOS common-source circuit with time-varying signal source in series with gate dc source

3.3.2 Digital Logic Gate

For the transistor inverter circuit in Figure 3.45, when the input is low and approximately zero volts, the transistor is cut off, and the output is high and equal to V_{DD} . When the input is high and equal to V_{DD} , the transistor is biased in the nonsaturation region and the output reaches a low value. Since the input voltages will be either high or low, we can analyze the circuit in terms of dc parameters.

Now consider the case when a second transistor is connected in parallel, as shown in Figure 3.46. If the two inputs are zero, both M_1 and M_2 are cut off, and $V_O = 5$ V. When $V_1 = 5$ V and $V_2 = 0$, the transistor M_1 turns on and M_2 is still cut off. Transistor M_1 is biased in the nonsaturation region, and V_O reaches a low value. If we reverse the input voltages such that $V_1 = 0$ and $V_2 = 5$ V, then M_1 is cut off and M_2 is biased in the nonsaturation region. Again, V_O is at a low value. If both inputs are high, at $V_1 = V_2 = 5$ V, then both transistors are biased in the nonsaturation region and V_O is low.

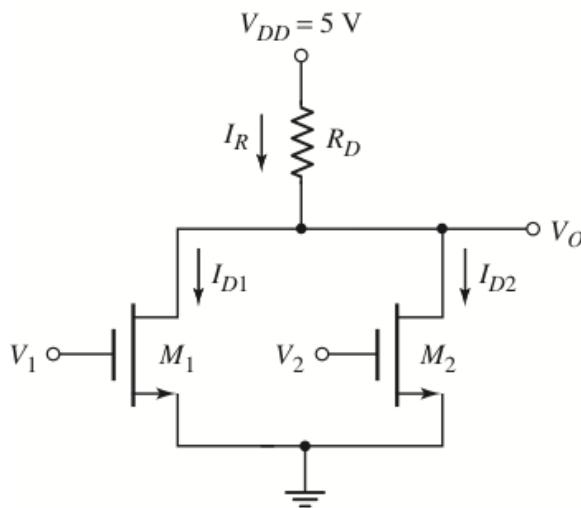


Figure 3.46 A two-input NMOS NOR logic gate

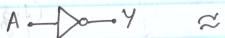
Table 3.2 shows these various conditions for the circuit in Figure 3.46. In a positive logic system, these results indicate that this circuit performs the NOR logic function, and, it is therefore called a two-input NOR logic circuit. In actual NMOS logic circuits, the resistor R_D is replaced by another NMOS transistor.

Table 3.2 NMOS NOR logic circuit response

$V_1(V)$	$V_2(V)$	$V_O(V)$
0	0	High
5	0	Low
0	5	Low
5	5	Low

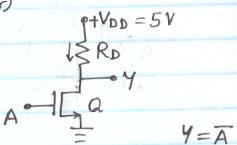
m. Digital circuits using MOSFETs:

i) NOT gate (or inverter)



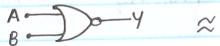
$$0V < V_{Tn}$$

$$\frac{A}{0V} \quad \frac{Y}{5V}$$

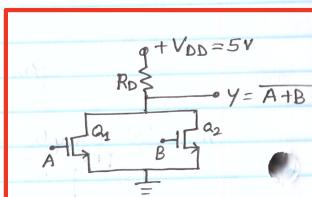


$$Y = \bar{A}$$

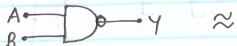
ii) NOR gate:



A	B	Y
0V	0V	5V
0V	5V	0V
5V	0V	0V
5V	5V	0V

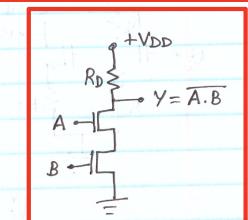


iii) NAND gate:



A	B	Y
0V	0V	5V
0V	5V	5V
5V	0V	5V
5V	5V	0V

A	B	Y
0V	5V	5V
5V	0V	5V
5V	5V	0V



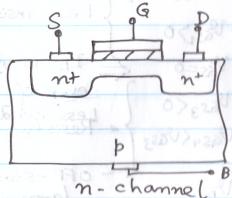
0V: Logic '0'
5V: Logic '1' (or +VDD)

For depletion-mode MOSFETs, the drain terminal is connected to the body/substrate.

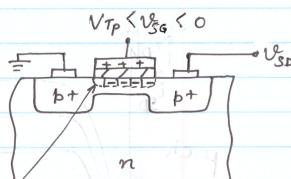
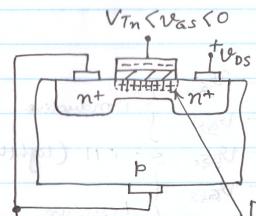
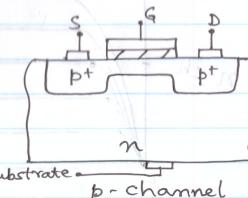
Normally-on

n. Depletion-mode MOSFETs : n & p channels.

Structure



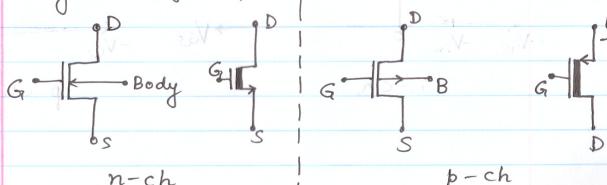
or



Depletion region forms due to inversion (blocks the channel)

At $V_{GS} \approx V_T$, the channel is completely blocked.
At $V_{GS} \approx 0$, the channel is ON.

Symbols of depletion-mode MOSFETs:



n-Channel Depletion-Mode MOSFET

Figure 3.14(a) shows the cross section of an n-channel **depletion-mode** MOSFET. When zero volts are applied to the gate, an n-channel region or inversion layer exists under the oxide as a result, for example, of impurities introduced during device fabrication. Since an n-region connects the n-source and n-drain, a drain-to-source current may be generated in the channel even with zero gate voltage. The term **depletion mode** means that a channel exists even at zero gate voltage. A negative gate voltage must be applied to the n-channel depletion-mode MOSFET to turn the device off.

Figure 3.14(b) shows the n-channel depletion mode MOSFET with a negative applied gate-to-source voltage. A negative gate voltage induces a space-charge region under the oxide, thereby reducing the thickness of the n-channel region. The reduced thickness decreases the channel conductance, which in turn reduces the drain current. When the gate voltage is equal to the threshold voltage, which is

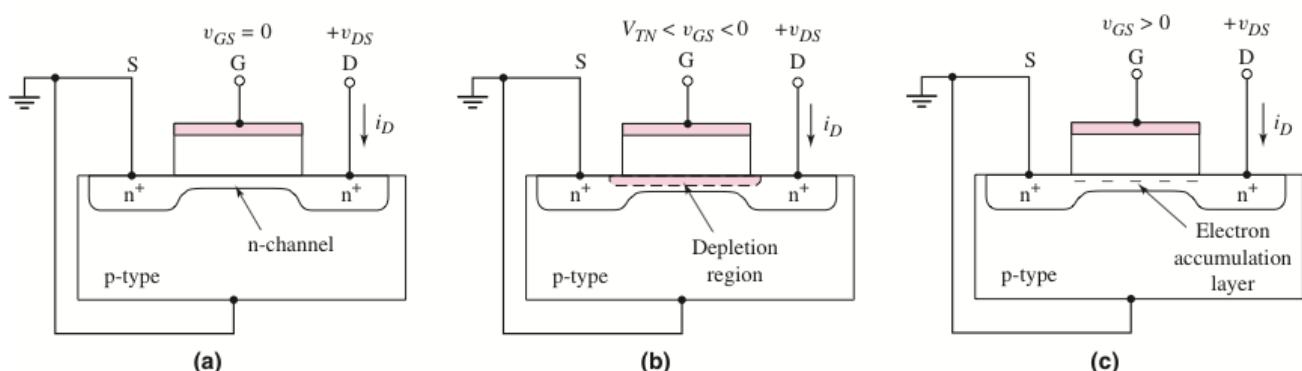


Figure 3.14 Cross section of an n-channel depletion mode MOSFET for: (a) $v_{GS} = 0$, (b) $v_{GS} < 0$, and (c) $v_{GS} > 0$

negative for this device, the induced space-charge region extends completely through the n-channel region, and the current goes to zero. A positive gate voltage creates an electron accumulation layer, as shown in Figure 3.14(c) which increases the drain current. The general i_D versus v_{DS} family of curves for the n-channel depletion-mode MOSFET is shown in Figure 3.15.

The current-voltage characteristics defined by Equations (3.2(a)) and (3.2(b)) apply to both enhancement- and depletion-mode n-channel devices. The only difference is that the threshold voltage V_{TN} is positive for the enhancement-mode MOSFET and negative for the depletion-mode MOSFET. Even though the current-voltage characteristics of enhancement- and depletion-mode devices are described by the same equations, different circuit symbols are used, simply for purposes of clarity.

N-I characteristics (n-ch) & (p-ch)

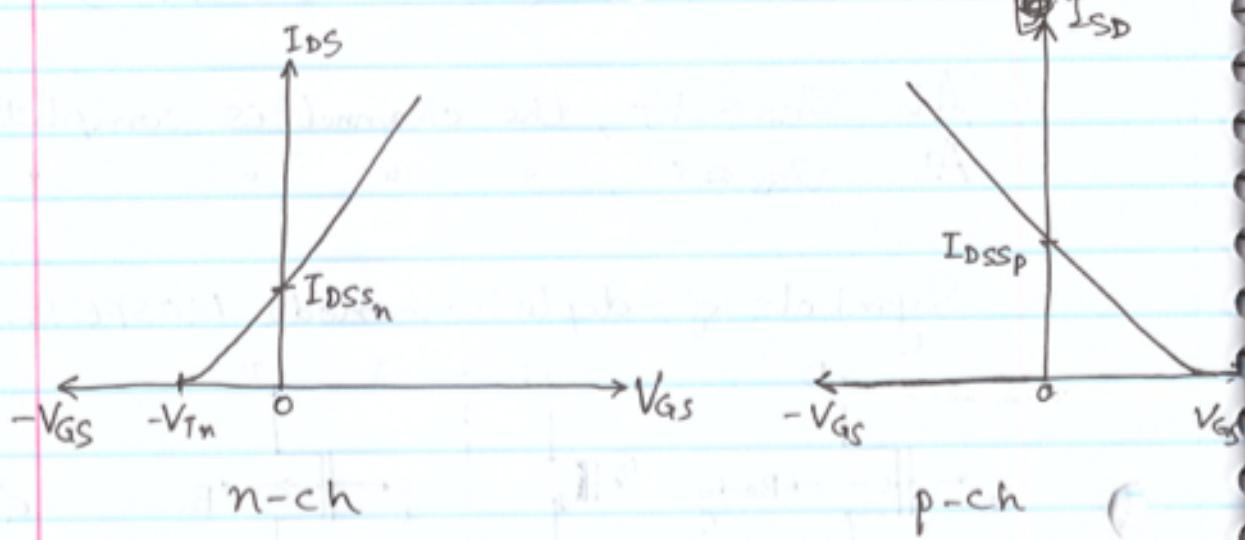
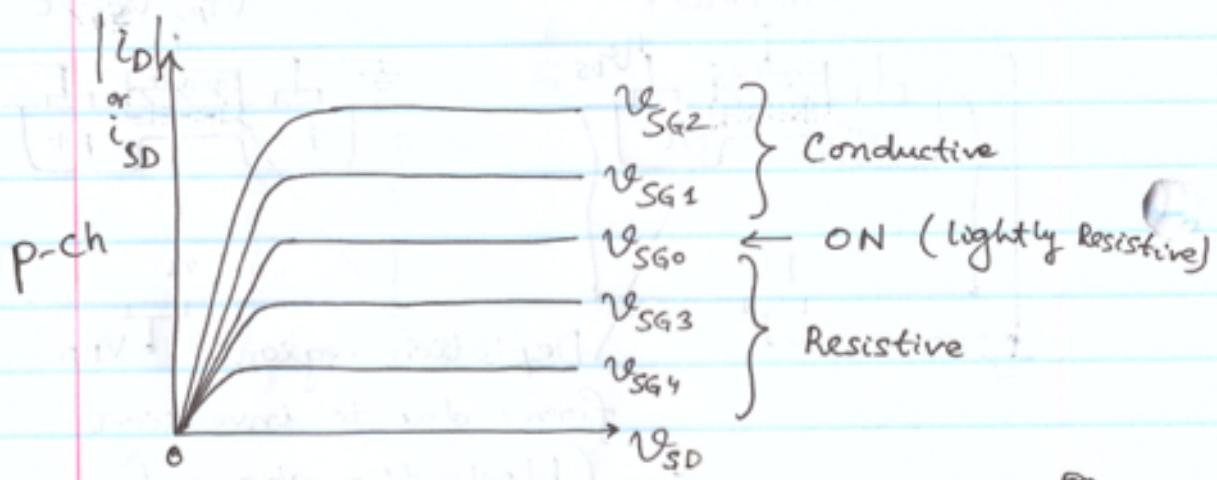
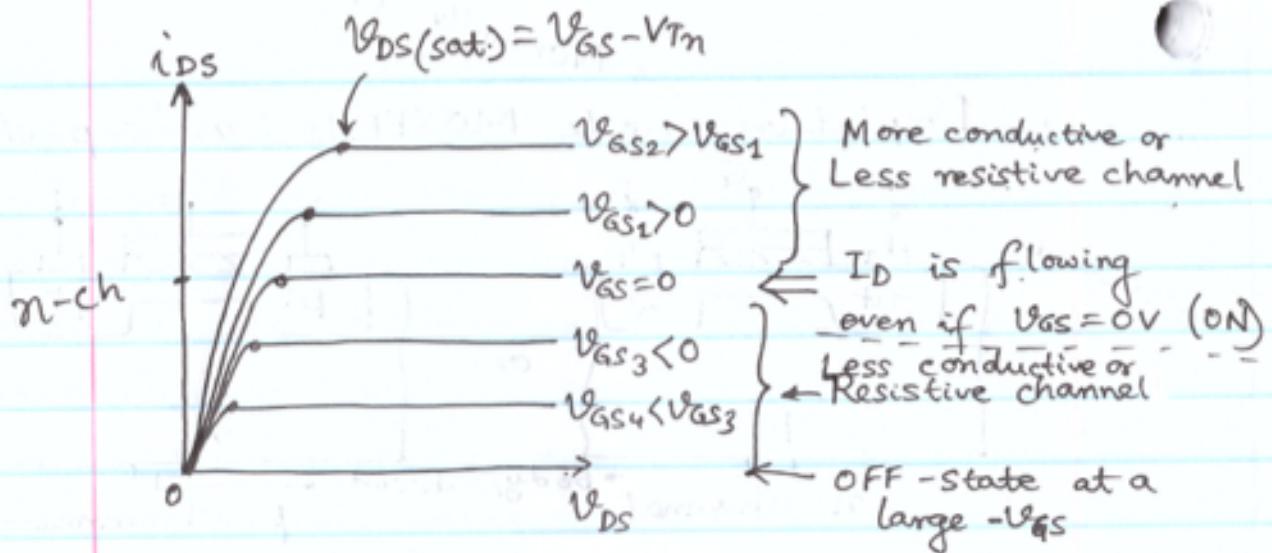


Table 3.1 Summary of the MOSFET current–voltage relationships

NMOS	PMOS
Nonsaturation region ($v_{DS} < v_{DS}(\text{sat})$)	Nonsaturation region ($v_{SD} < v_{SD}(\text{sat})$)
$i_D = K_n[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$i_D = K_p[2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation region ($v_{DS} > v_{DS}(\text{sat})$)	Saturation region ($v_{SD} > v_{SD}(\text{sat})$)
$i_D = K_n(v_{GS} - V_{TN})^2$	$i_D = K_p(v_{SG} + V_{TP})^2$
Transition point	Transition point
$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement mode	Enhancement mode
$V_{TN} > 0$	$V_{TP} < 0$
Depletion mode	Depletion mode
$V_{TN} < 0$	$V_{TP} > 0$