MS31007: Chapter 8 (IV)

Electrical Properties

Part 4

MSC, IIT Kharagpur

Content

1. Introduction
2. Electrical Conduction
3. Metal, Semiconductor and Insulator
4. Band Structure of Solids and conduction mechanism
5. Semiconductivity: Intrinsic and Extrinsic
6. Hall Effect
7. Electrical Conduction in Ionic Ceramics and in Polymers

8. Other Electrical Characteristics of Materials

Electronic Devices and Fabrication

Extrinsic Semiconductors

Extrinsic semiconductors - electrical properties (conductivity) is dictated by impurity atoms. Example: Si is considered to be extrinsic at room T if impurity concentration is one atom per 10^{12}

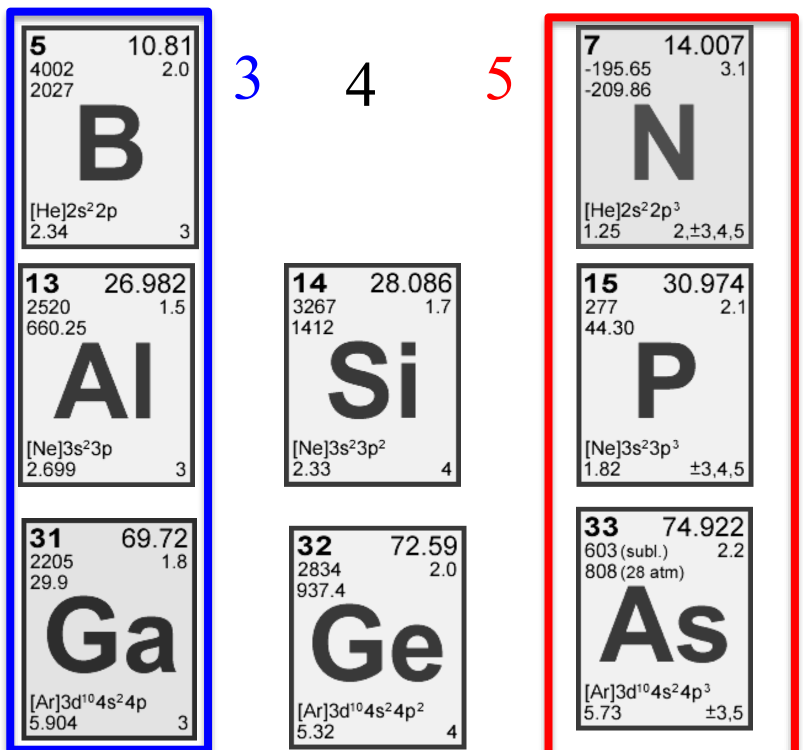
An extrinsic semiconductor may have different concentrations of holes and electrons.

It is called **p-type** if p >> n and **n-type** if n >> p.

– Two common methods of doping are diffusion and ion implantation.

These elements have one less valence e- relative to Si

When present as impurities, they will create lots of extra holes called “p-type”



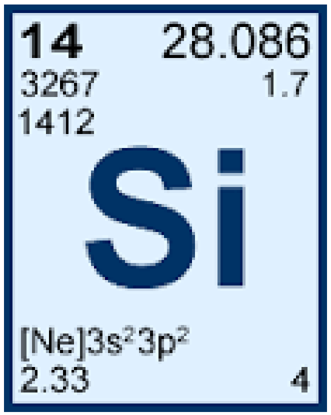
These elements have one more valence e- relative to Si

When present as impurities, they will create lots of extra mobile e- called “n-type”

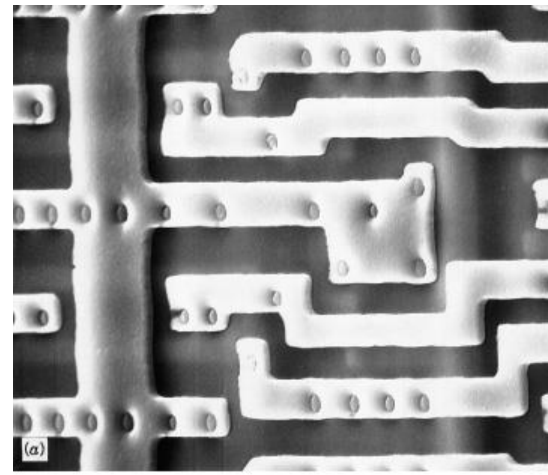
Semiconductor Devices

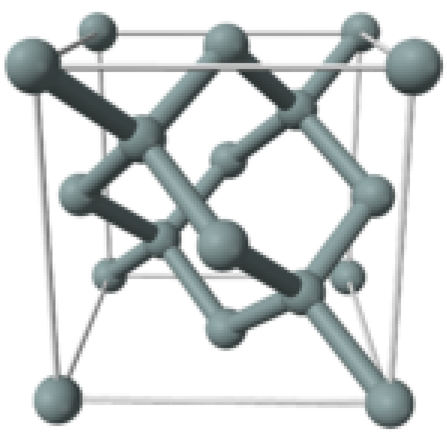
Electrical properties of semiconductors allow them to be used to perform electronic functions – diodes, transistors

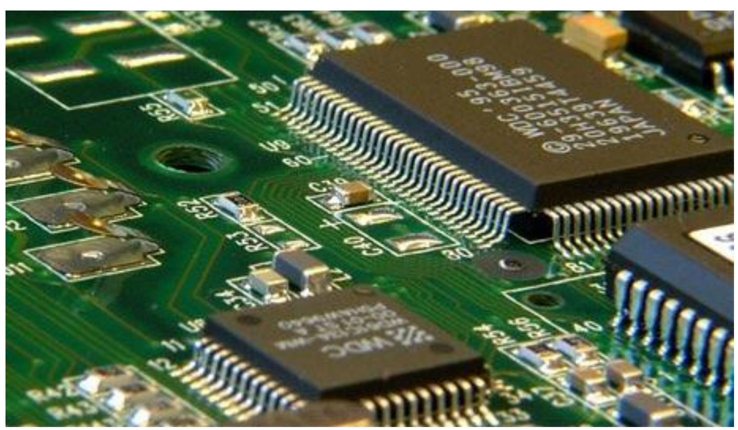
- Advantages: small size, low power consumption, no warmup time
- In short, these are the workhorse of the semiconductor industry and why your phone is so small!

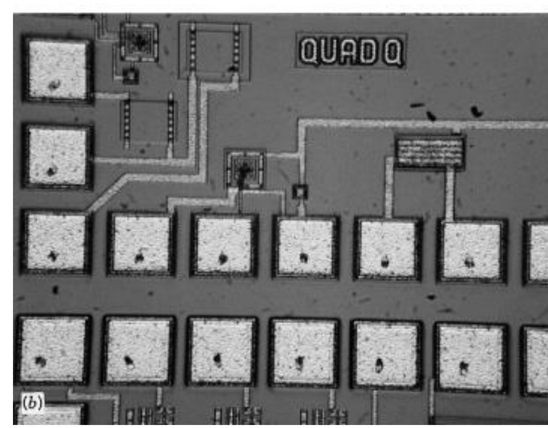


The Silicon Age



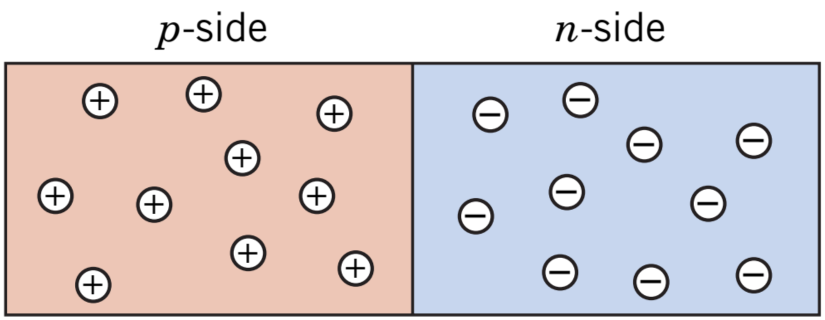






Semiconductor: p-n Junction

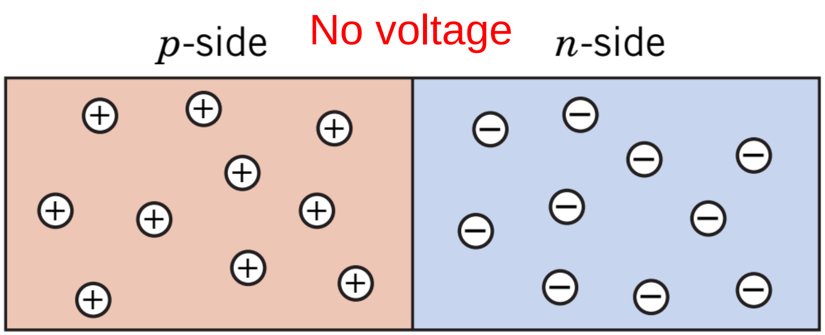
- **In p-n junction**; P-doped semiconductor is relatively conductive. The same is true of N-doped semiconductor, but the junction between them is a nonconductor (depletion region).
- This nonconducting layer, called the depletion zone, occurs because the electrical charge carriers in doped n-type and p-type silicon (electrons and holes, respectively) attract and eliminate each other in a process called recombination.
- By manipulating this nonconductive layer, p-n junctions are commonly used as diodes:
- electrical switches that allow a flow of electricity in one direction but not in the other (opposite) direction.



- This property is explained in terms of the *forward-bias* and *reverse-bias* effects, where the term *bias* refers to an application of electric voltage to the p-n junction.

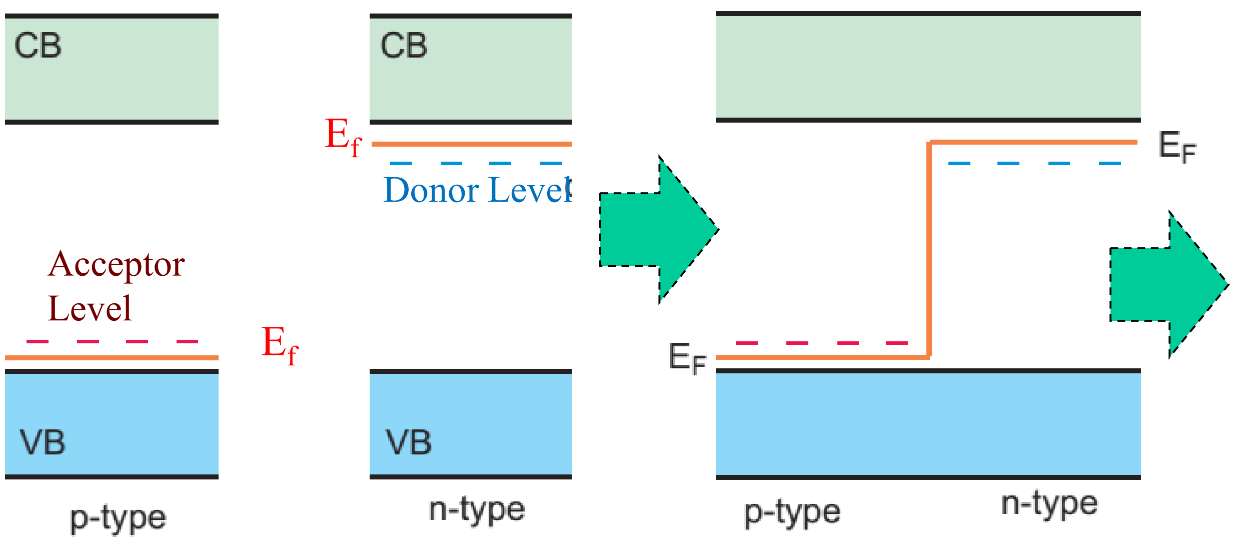
Semiconductor: *p-n* Rectifying Junction

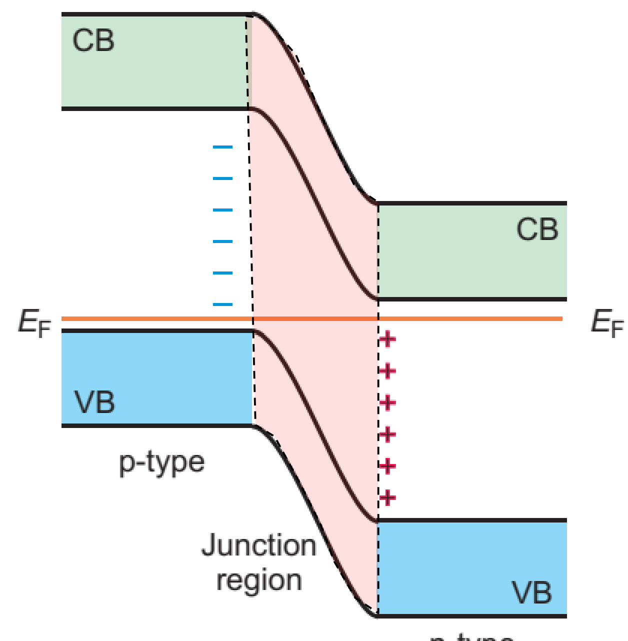
Rectifier/diode – permits current to flow in one direction only. A rectifier can transform alternating current to direct current



❖Construct *p-n* rectifying junction from a single piece of semiconductor doped such that one side is *n*-type and the other is *p*-type

At the junction electrons and holes recombine : Depletion region (~ 1 μm)



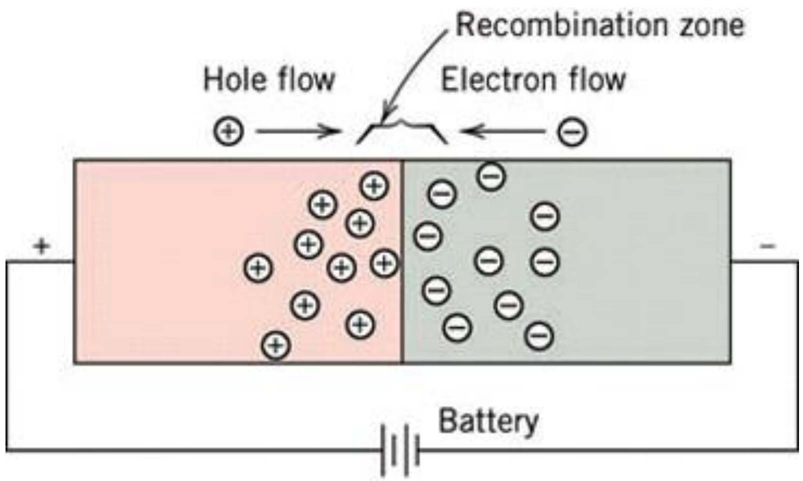


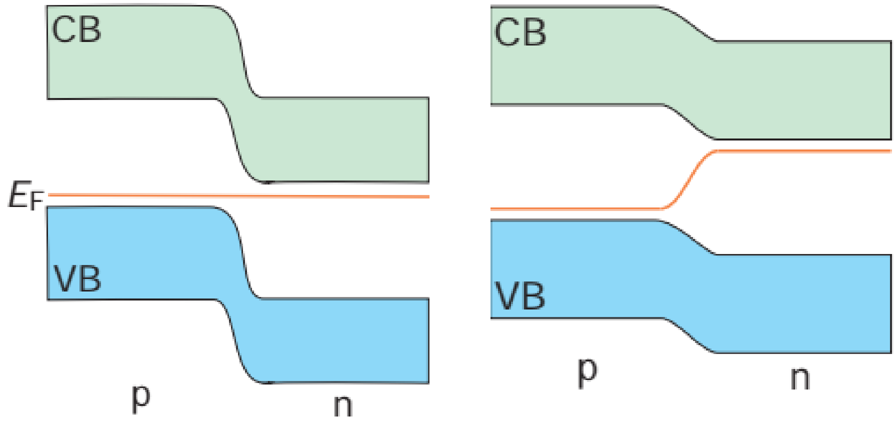
(a) energy bands of separated p-type and n-type materials;
(b) energy bands for juxtaposed p-type and n-type materials;
(c) distorted energy bands in the junction region at equilibrium

If the Fermi level slopes it is energetically favourable for electrons to 'roll downhill' and holes to 'roll uphill'

p-n junction: forward bias

- The 'holes' in the p-type region and the electrons in the **n-type** region are pushed towards the junction. This reduces the width of the depletion zone.
- The positive charge applied to the **p-type** block repels the holes, while the negative charge applied to the **n-type** block repels the electrons.
- As electrons and holes are pushed towards the junction, the distance between them decreases. This lowers the barrier in potential.
- With increasing bias voltage, eventually the nonconducting depletion zone becomes so thin that the charge carriers can tunnel across the barrier, and the electrical resistance falls to a low value.

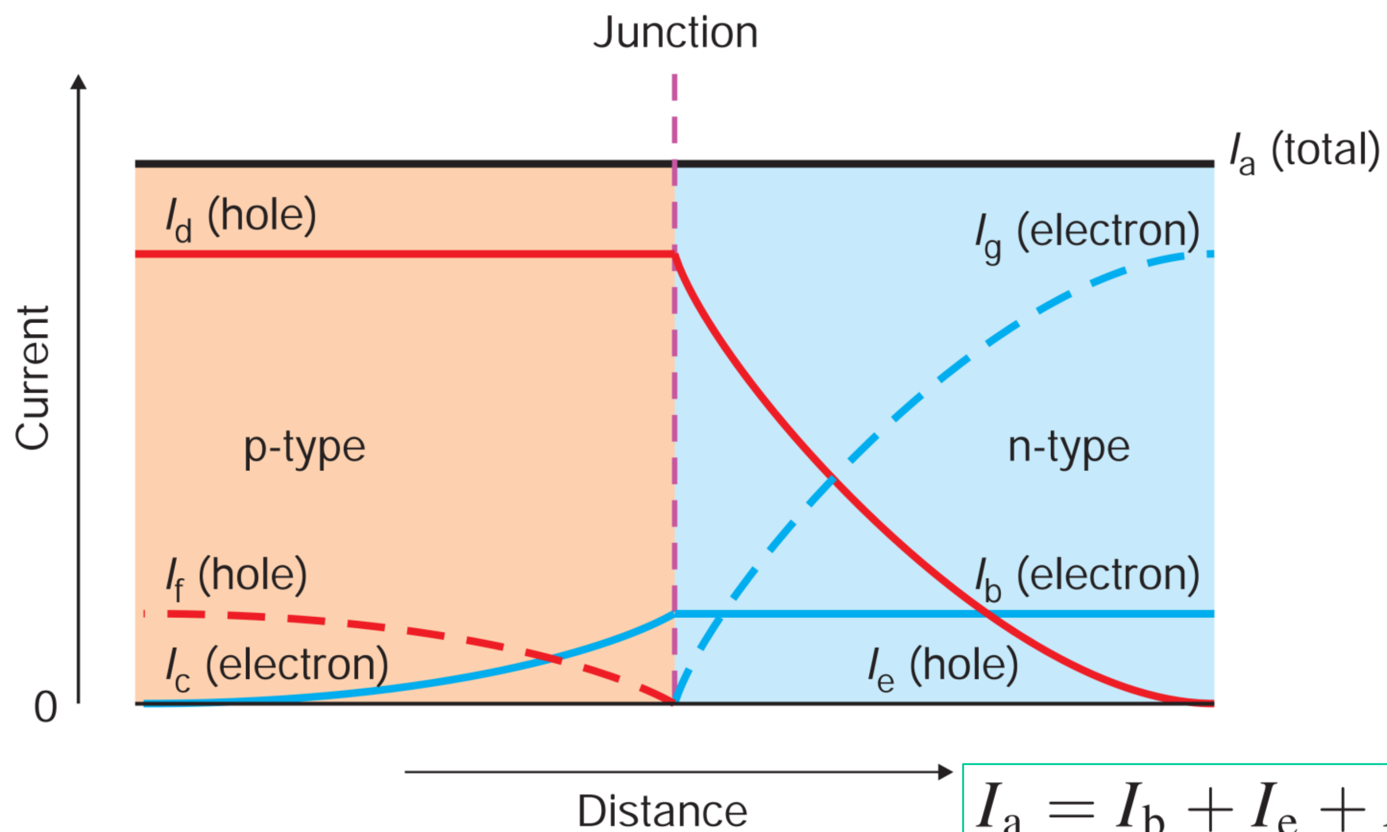




Band structure across a p-n junction: (a) no bias, (b) under forward bias

- The electrons which pass the junction barrier enter the p-type region and a current flows.

The currents flowing across a p-n junction under forward bias



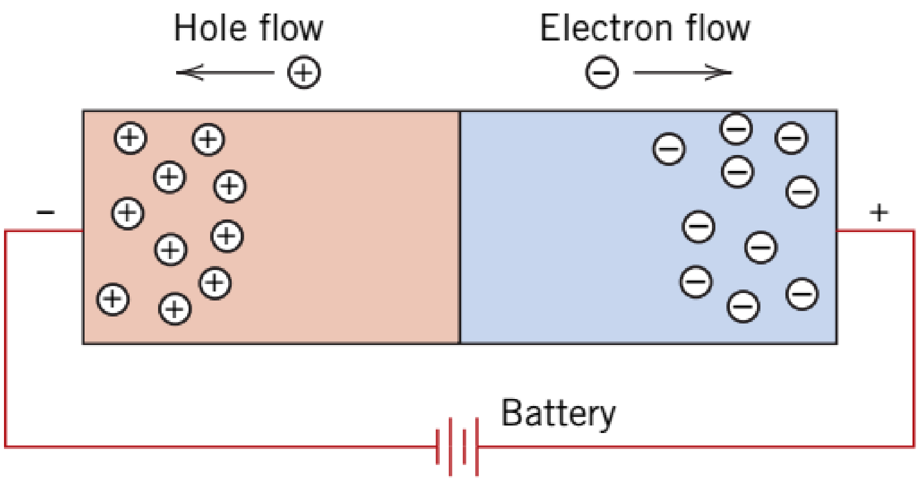
$$\boxed{I_a = I_b + I_e + I_g = I_c + I_d + I_f}$$

where $\mathbf{I_a}$ **is the constant total current**;
I_b is the electron current flowing in the n-type region (constant);
I_c is the injected (introduced) electron current in the p-type region (decaying);
I_d is the hole current in the p-type region (constant);
I_e is the injected hole current in the n-type region (decaying);
I_f is the declining hole current in the p-type region to balance and annihilate I_c;
and I_g is the declining electron current in the n-type region to balance and annihilate I_e.

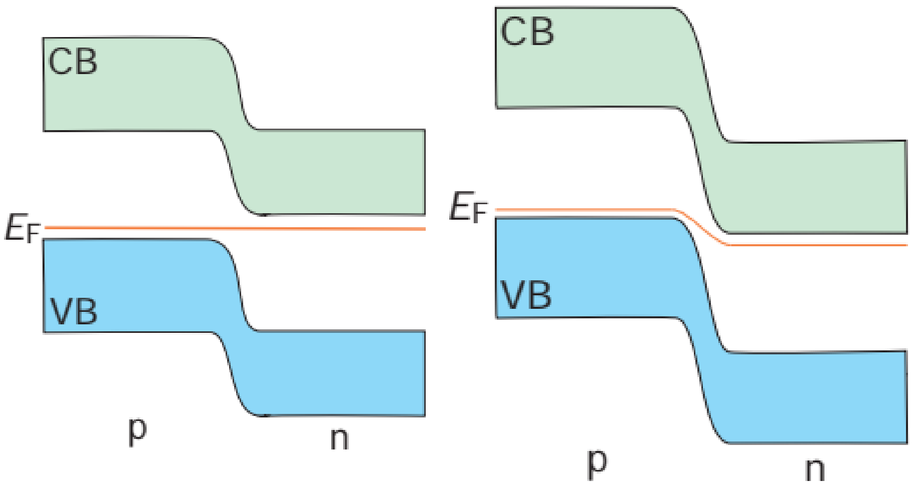
p-n junction: Reverse bias

Thus for a forward bias large numbers of charge carriers move across the semiconductor to the junction

- **<u>Reverse bias</u> – now switch potential; holes and electrons move away from the junction.**

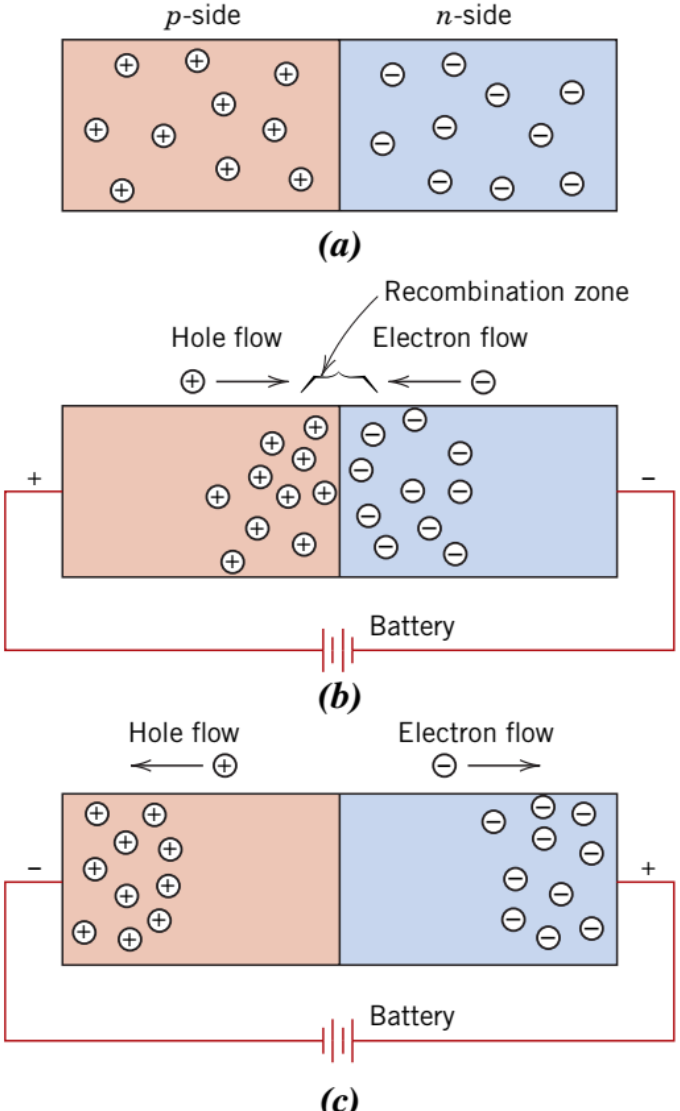


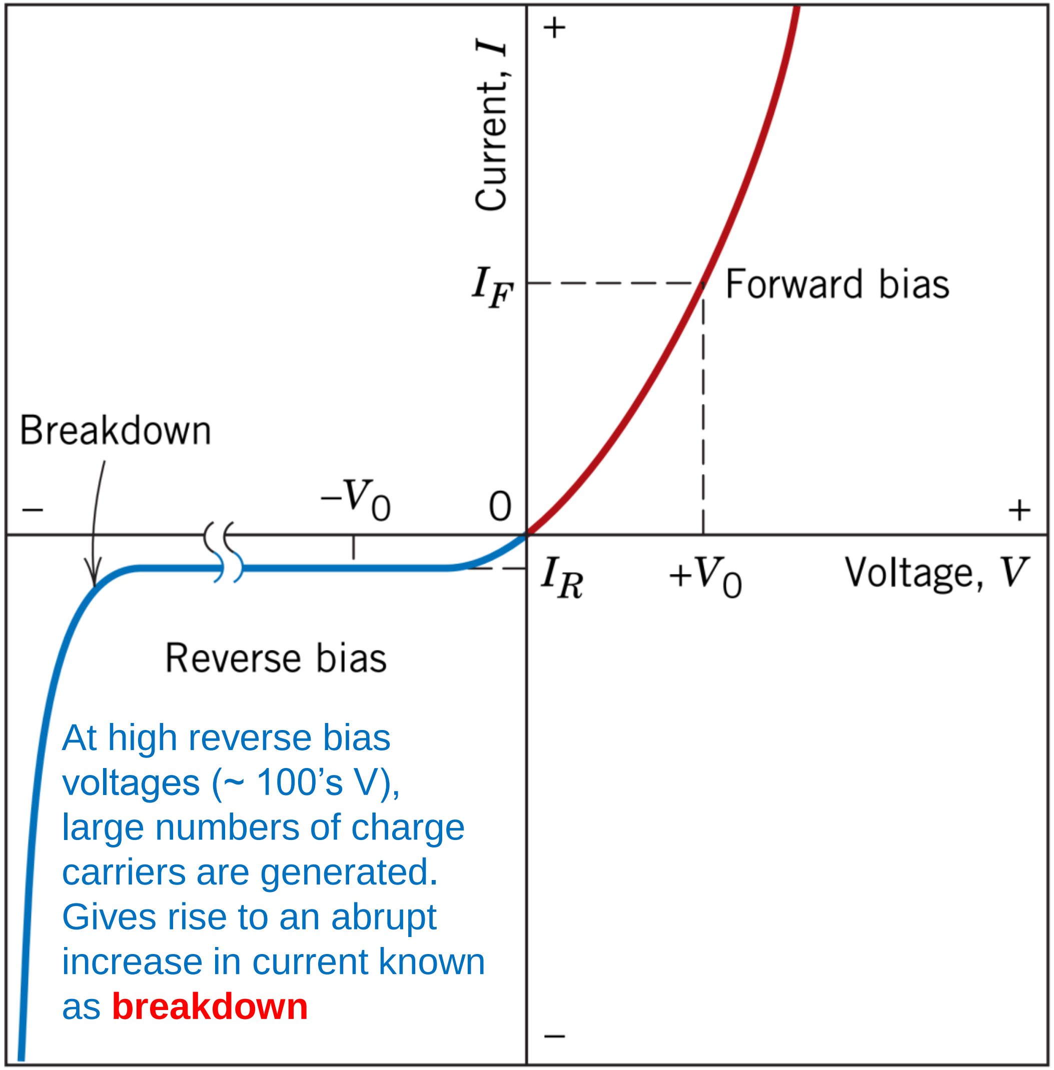
Reverse bias: carrier flow away from p-n junction; carrier conc. greatly reduced at junction; little current flow.



Band structure across a p-n junction: (a) no bias, (b) under forward bias

Current-Voltage behavior in junctions

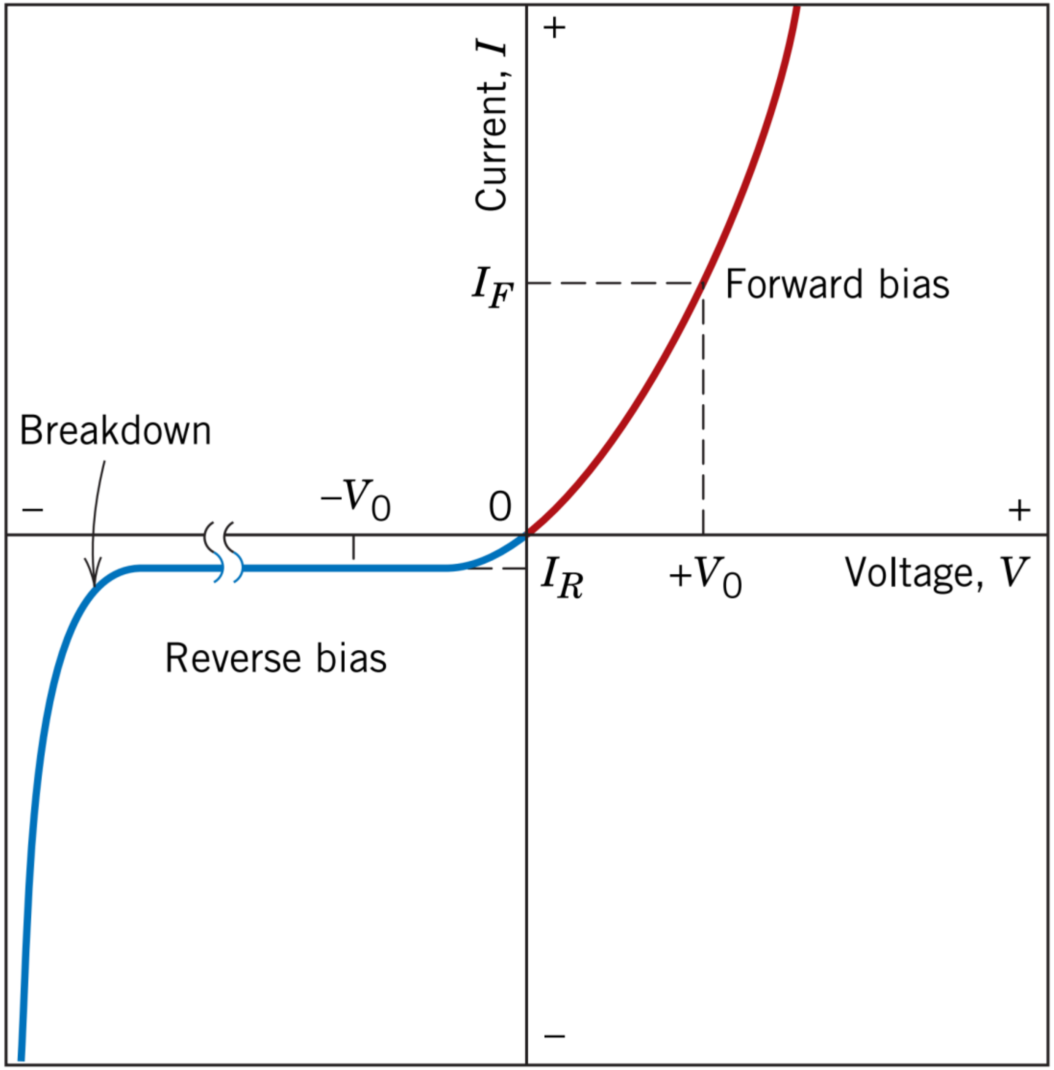




Forward bias – appreciable current, low resistivity

Reverse bias – highly insulative (low current, high resistance)

Current-Voltage behavior in junctions



Forward bias – appreciable current, low resistivity
Reverse bias – highly insulative (low current, high resistance)

The change of current with applied voltage is given by the Shockley equation.

$$I = I_0\left[\exp\left(\frac{eV}{k_B T}\right) - 1\right]$$

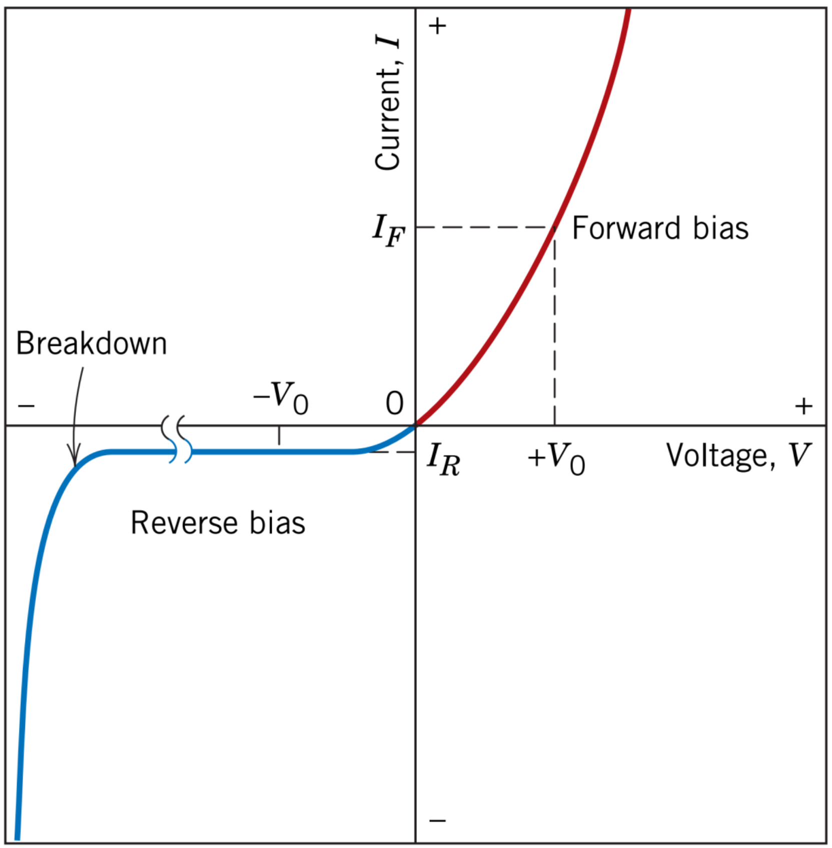
where I_0 is a constant term, the saturation current, determined by the junction geometry and the doping levels, e is the charge on the electrons and holes, V is the applied voltage, k_B is Boltzmann's constant and T the temperature

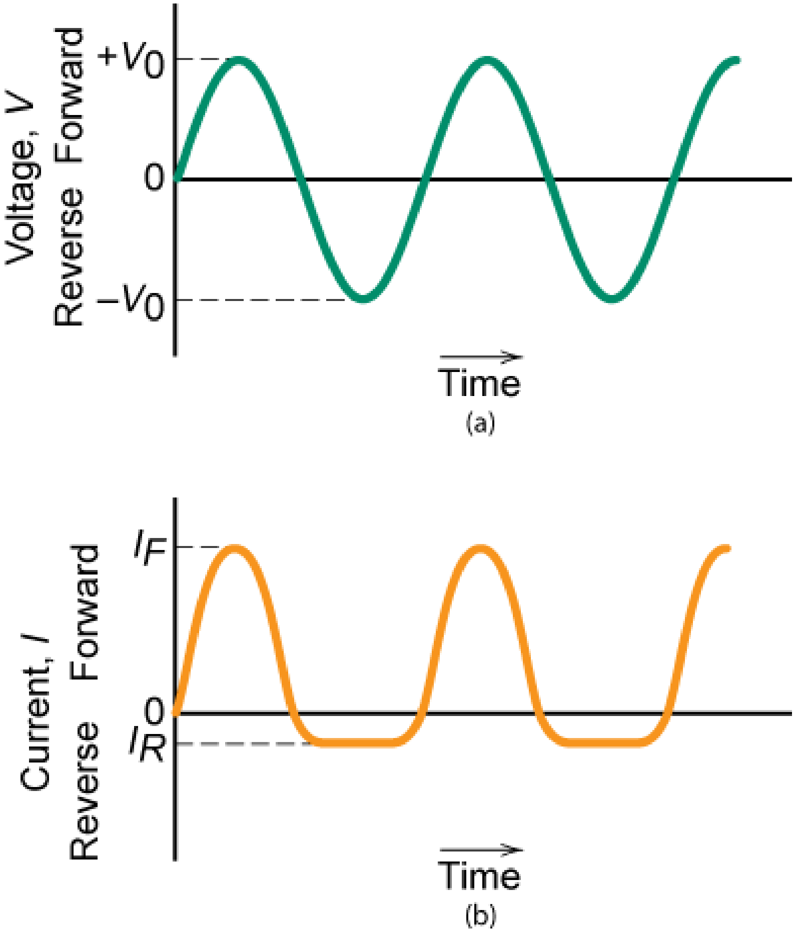
- When a forward bias is applied the number of electrons moving to the left will increase rapidly, by a factor of **$\exp(V/k_B T)$.**
- If V is 0.1 V, this is a factor of about 55x at room temperature. Thus the number of electrons appearing at the p-type boundary is about 55 times higher than the equilibrium concentration there.

p-n Rectifying Junction

What does this have to do with electronics

- **By switching the bias you control current flow through the junction**
- **Current in the reverse bias mode I_R is very small compared to that in forward bias mode I_F**





$I_R << I_F$; this is called rectification

The Transistor

Perform two primary functions

- Amplify electrical signals
- Serve as switching devices for processing/storing information

– **Two major types**

- Junction (bimodal) transistor
- Metal oxide semiconductor field-effect transistor (MOSFET)

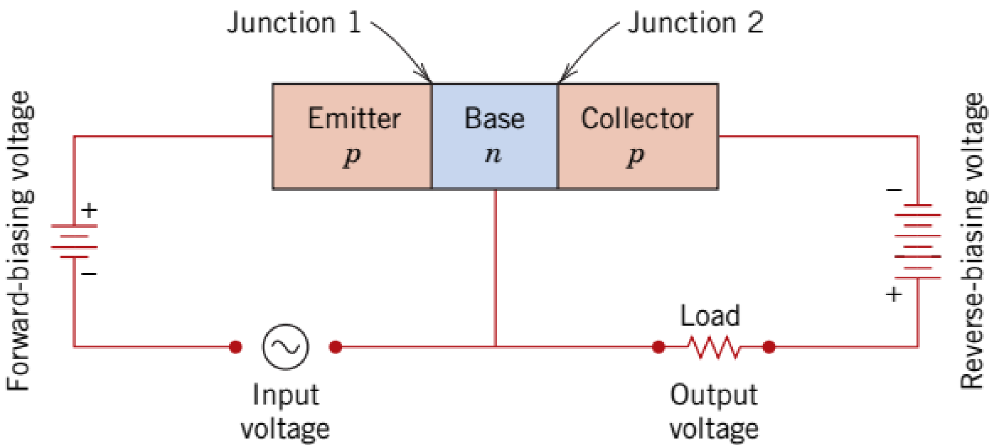
Junction transistors

Basic idea: two *p-n* junctions arranged back to back (either *n-p-n* or *p-n-p*)

– Place thin *n*-type *base (thin)* region between the two *p*-type regions; one is called the **emitter** and the other is called the **collector**

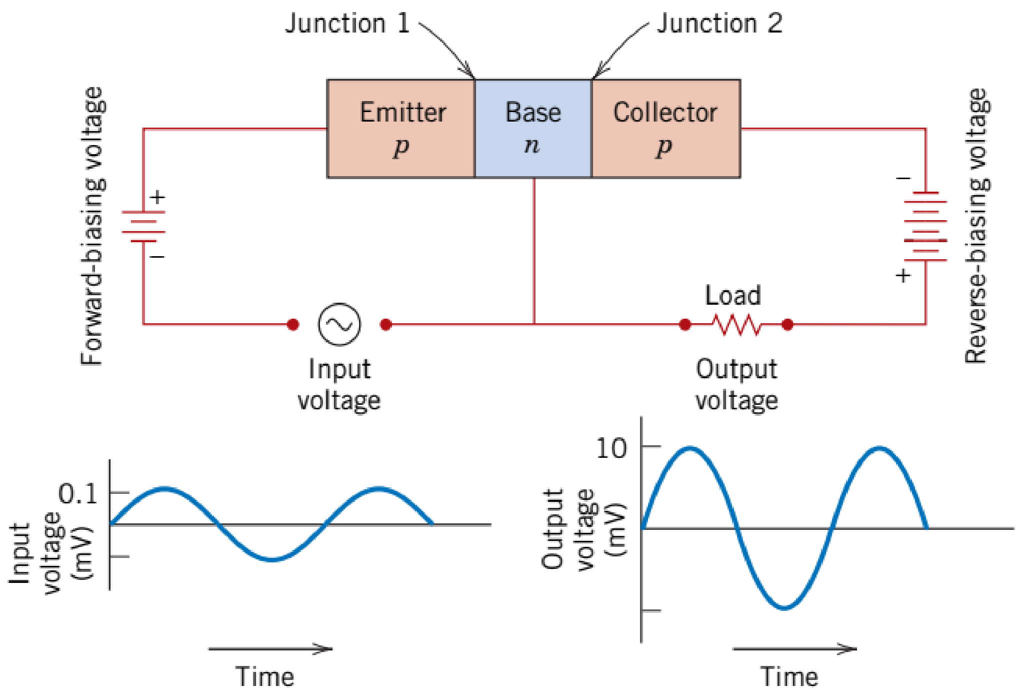
– Note biasing of the circuitry

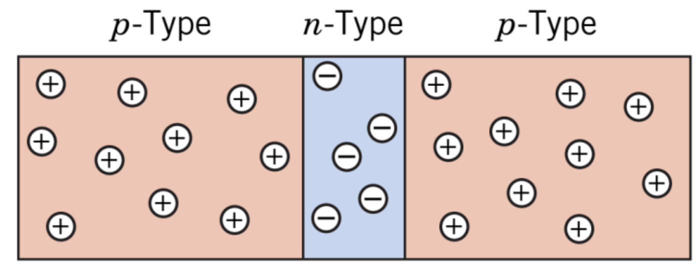
Junction transistors – how they work?



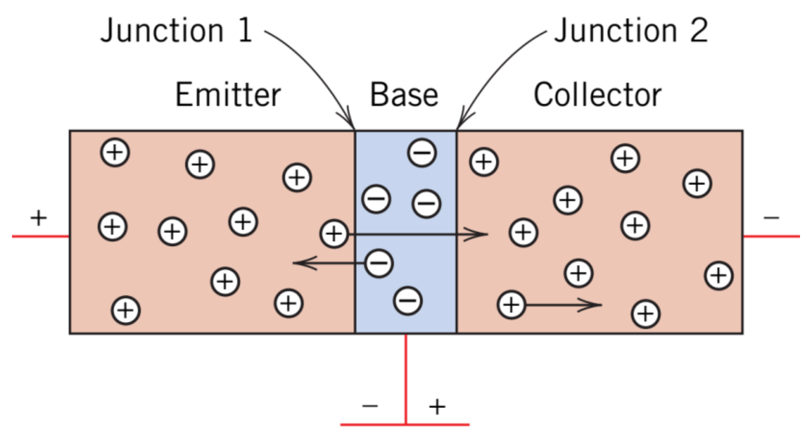
Junction 1: Emitter–Base junction is forward biased,
Junction 2: Base–Collector junction is reverse bias

Junction Transistors





(a)



- Given forward bias, large numbers of holes enter the base region. While some recombine with electrons, if the material is properly designed, most are swept through the base *without recombining* and into junction two
- Since there is a reverse bias on the output side (into the collector), holes are effectively driven away from junction 2
- Small increase in input voltage within emitter-base circuit leads to large increase in current across junction 2 (collector current), leads to large increase in voltage across load resistor
- **Voltage signal that passes through a junction transistor experiences amplification**

Similar reasoning applies to the operation of an *n–p–n* transistor, except that electrons instead of holes are injected across the base and into the collector.

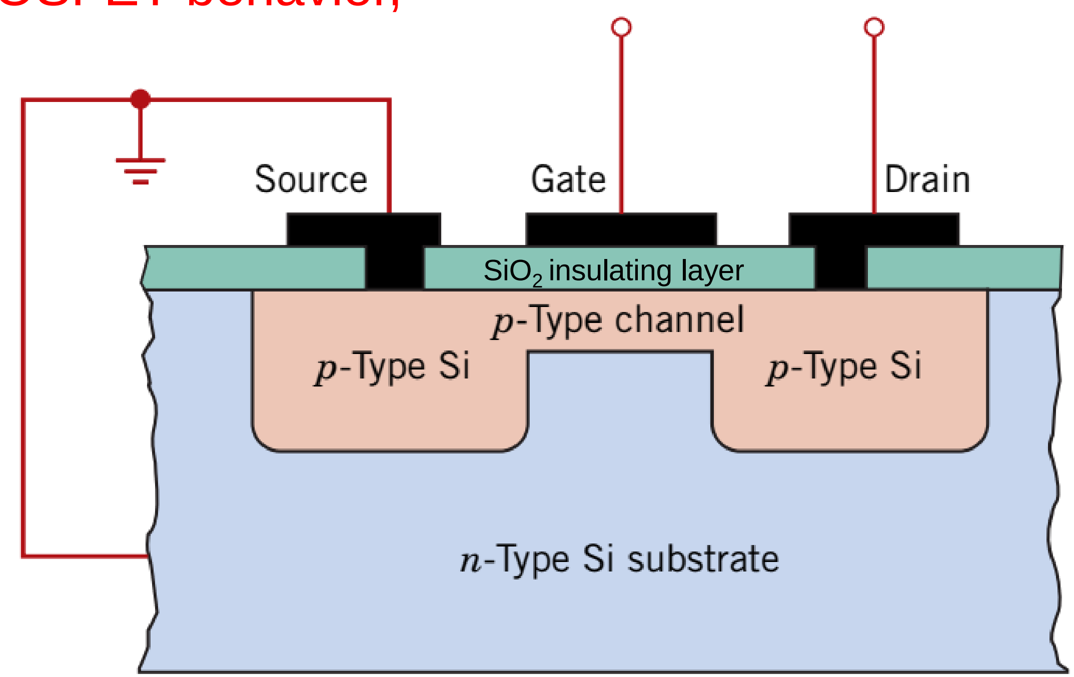
Metal oxide semiconductor field effect transistor (MOSFET)

Physics: conductivity of the channel is varied by the presence of an electrical field on the gate

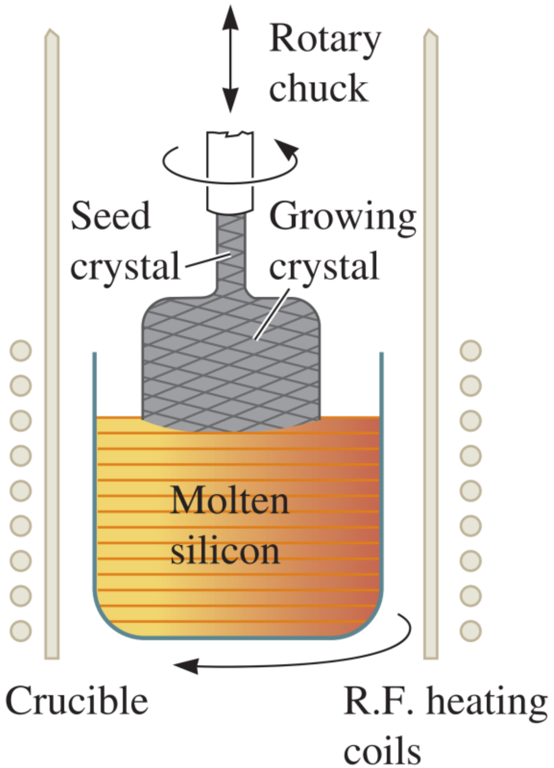
- Impose positive field on gate – drive charge carriers (holes) out of the channel, reducing conductivity
- Small alteration of field at the gate produces a relatively large variation in current between the source and drain
- Key difference with junction transistor – gate current is exceedingly small as compared to the junction transistor
- Majority carrier dominates MOSFET behavior, minority carriers play a role with junction transistors

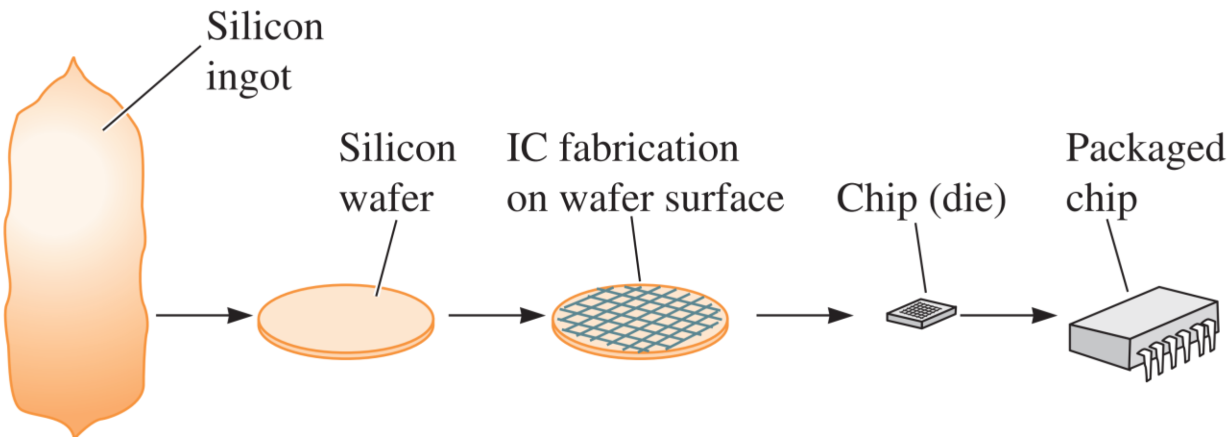
– Two small islands of a *p*-type semiconductor within a substrate of *n*-type silicon. Islands joined by a narrow *p*-type channel

– Have metal connects to islands; form an insulating layer on the surface by oxidizing silicon



Growth of Si crystal

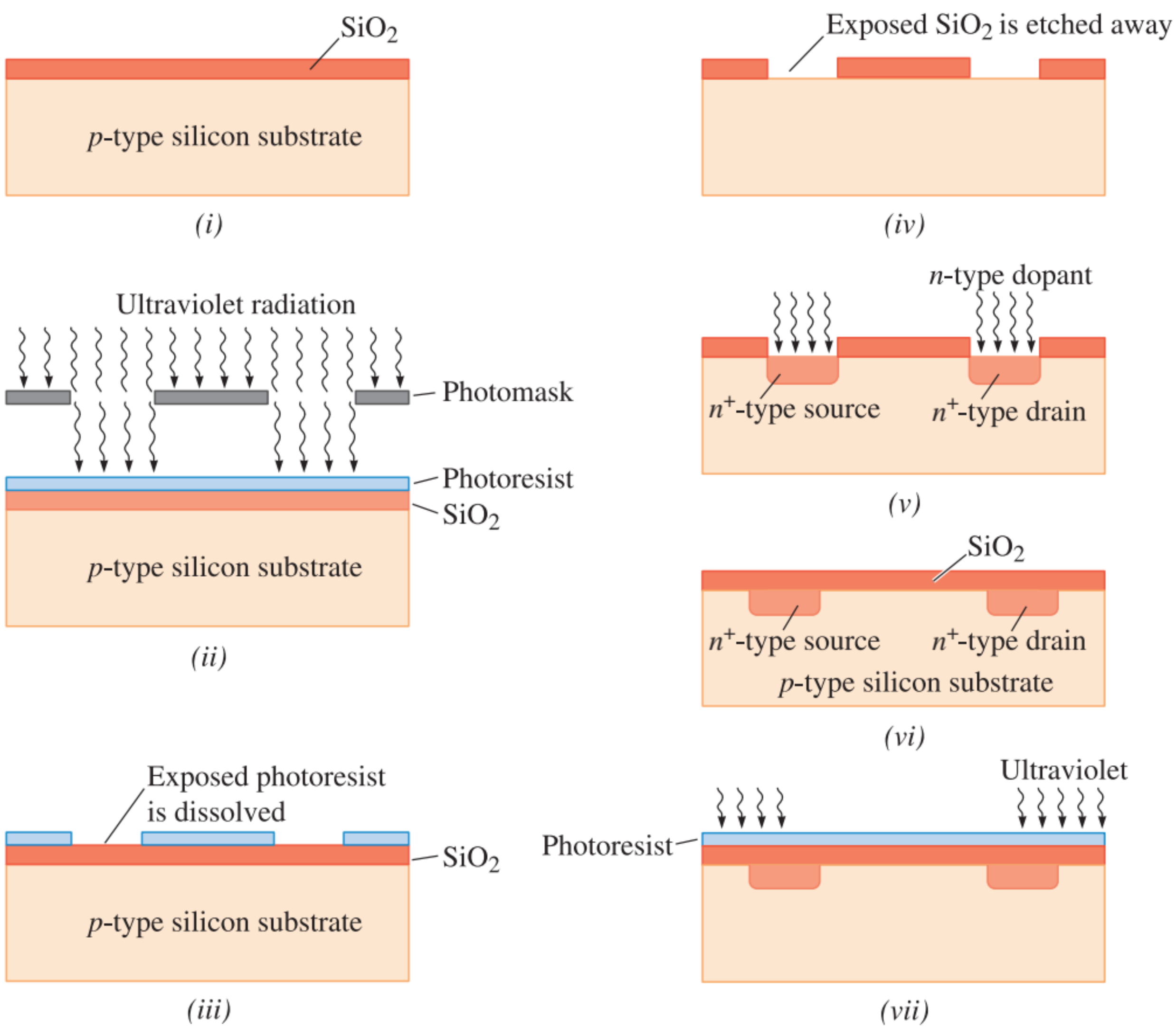




Czochralski growth technique for growing single crystals of silicon

IC Fabrication Process

Overall steps encountered in the processing of semiconductors. Production of a FET semiconductor device:

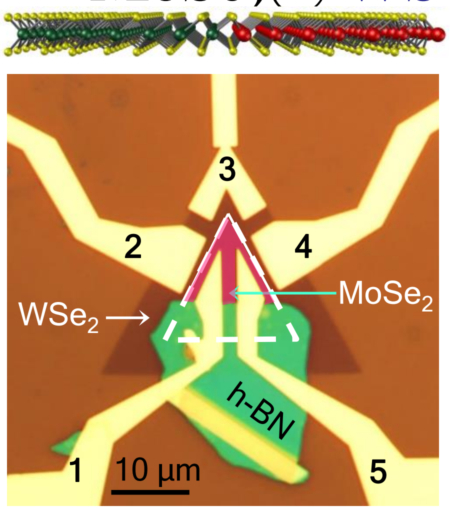


(i) A p-type silicon substrate is oxidized. (ii) In a process known as photolithography, ultraviolet radiation passes through a photomask (which is much like a stencil), thereby exposing a photosensitive material known as photoresist that was previously deposited on the surface. (iii) The exposed photoresist is dissolved. (iv) The exposed silica is removed by etching. (v) An n-type dopant is introduced to produce the source and drain. (vi) The silicon is again oxidized. (vii) Photolithography is repeated to introduce other components, including electrical connections, for the device.

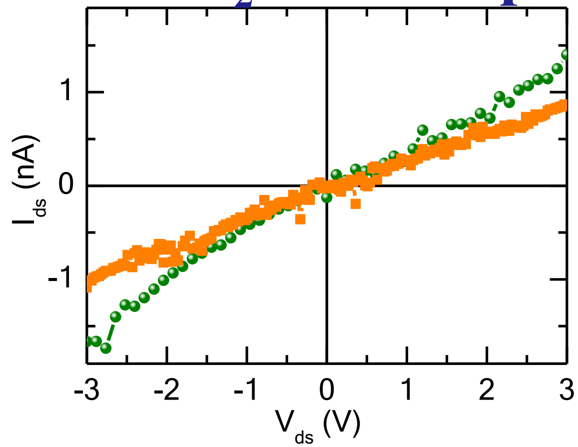
Electrical Transport Measurement: 2D p-n junction

P. Sahoo et al. Nature 2018

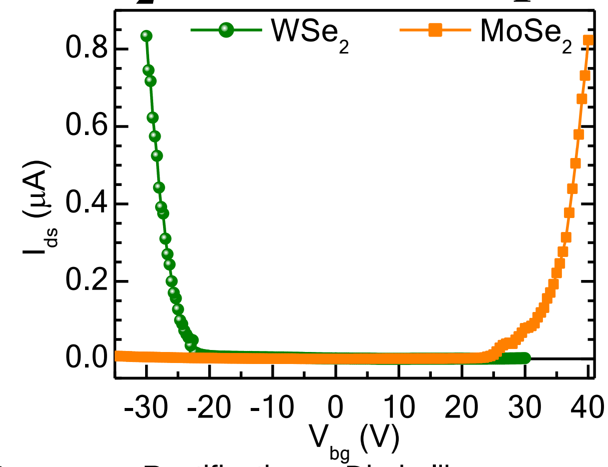
$MoSe_2$@ WSe_2



WSe_2 : hole doped; $MoSe_2$: electron doped



I_{ds} ~V_{ds} is nearly **linear** [V_{bg}=0V] indicating thermionic emission of charge carriers across the Schottky barriers



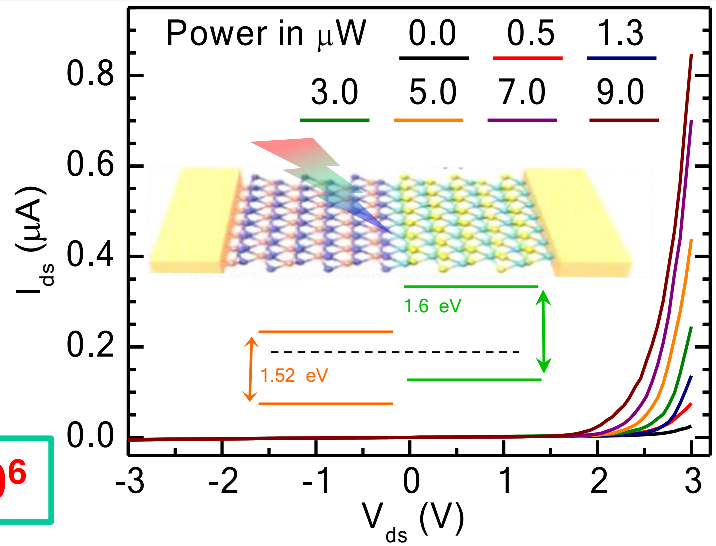
Rectification or Diode-like response indicating PN junction formation

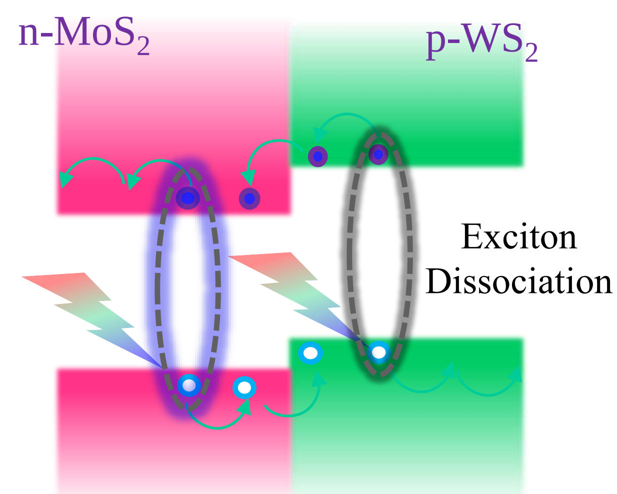
Two Terminal I-V Characteristics : Diode-like response and more prominent under illumination

λ = 532 nm
Mode filed diameter: 10 µm

Photo current
$I_{ph}=I_{ds}-I_{dark}$
at $V_{bg}=0$

I_{on}/I_{off} = ~ 10^5 to 10^6



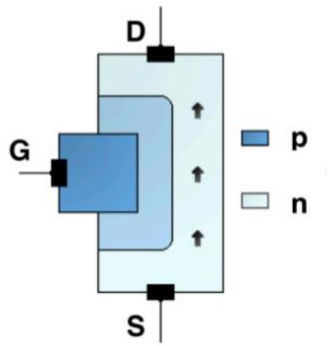


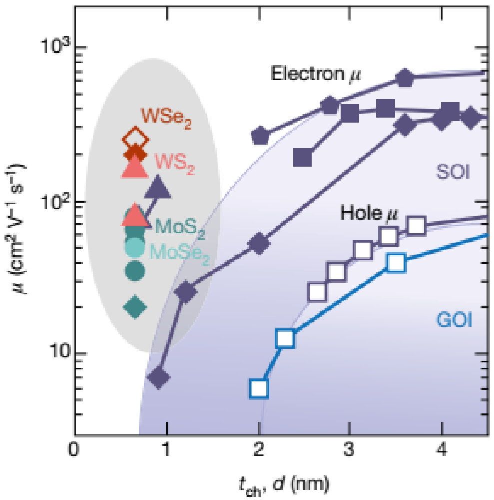
Summary

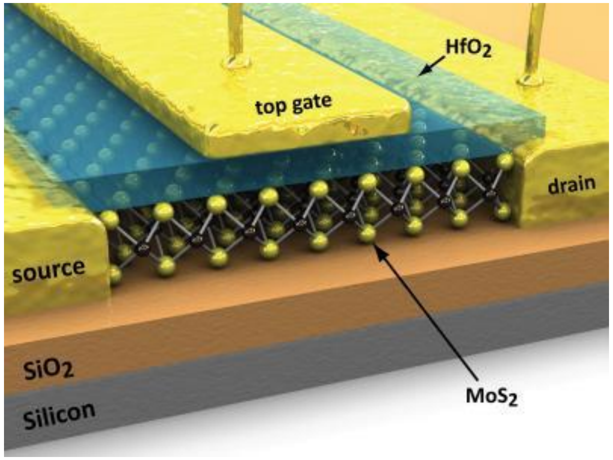
- Conductors, semiconductors, and insulators...
  -- differ in accessibility of energy states for
  conductance electrons.
- For pure semiconductors, conductivity is increased by
  -- increasing temperature
  -- doping (e.g., adding B to Si (*p*-type) or P to Si (*n*-type).
- Energy Band Structures and Bonding (metals, semiconductors, insulators)
- Hall effect to measure carrier concentration and mobility
- Electronic Devices (FET and MOSFET) and their working principles
- 2D materials for future electronics

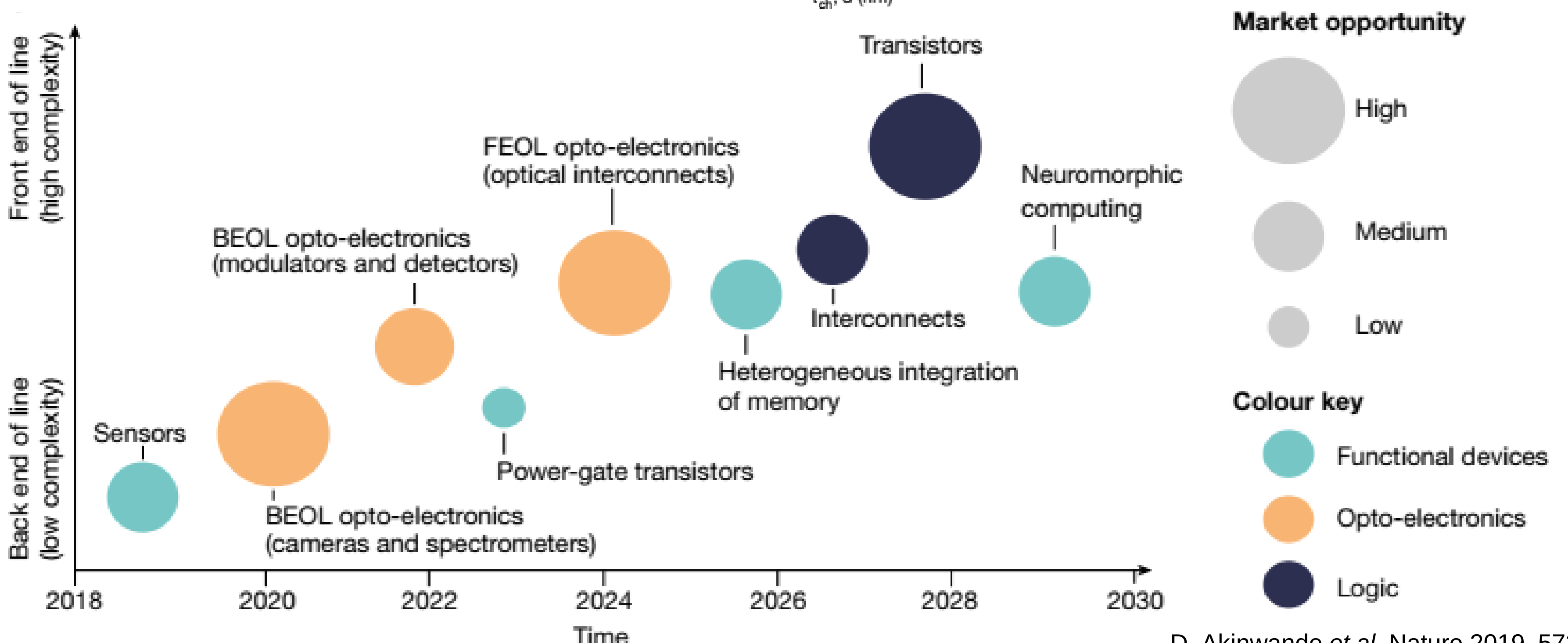
Potential applications of 2D Materials and modern transistor devices

Field Effect Transistors (FET)





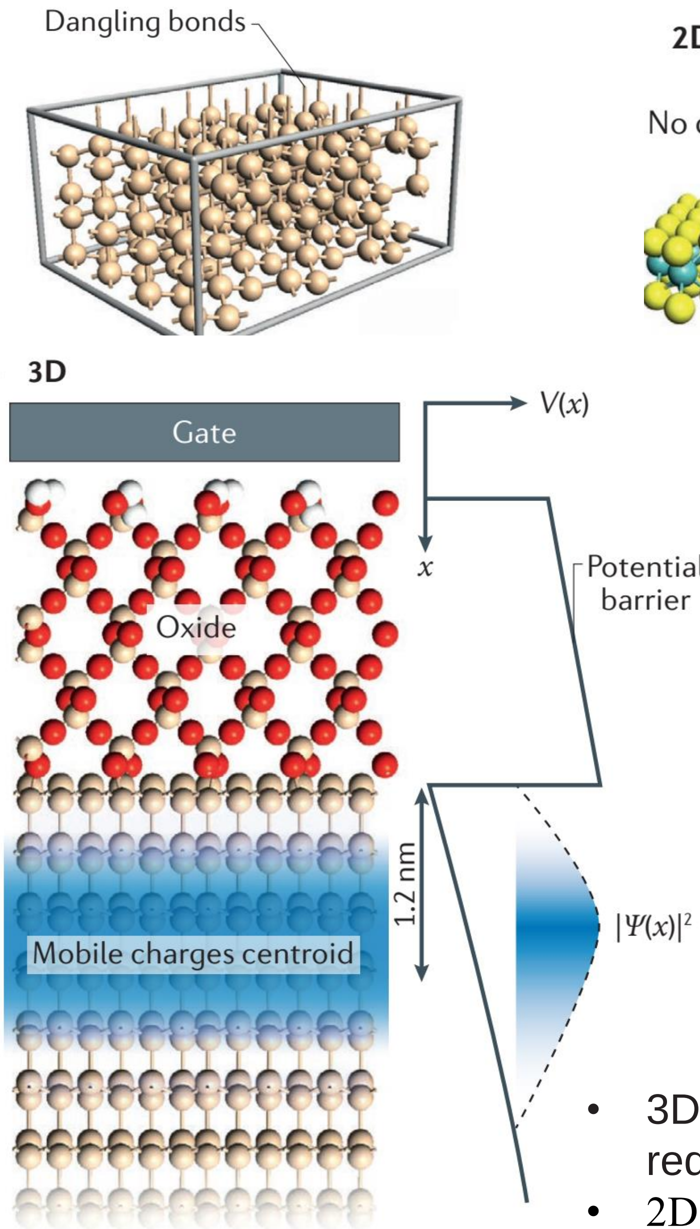


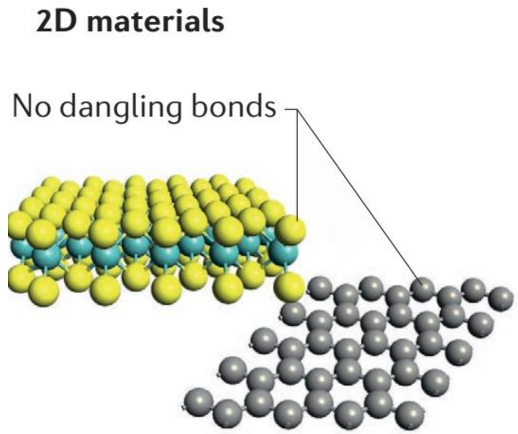


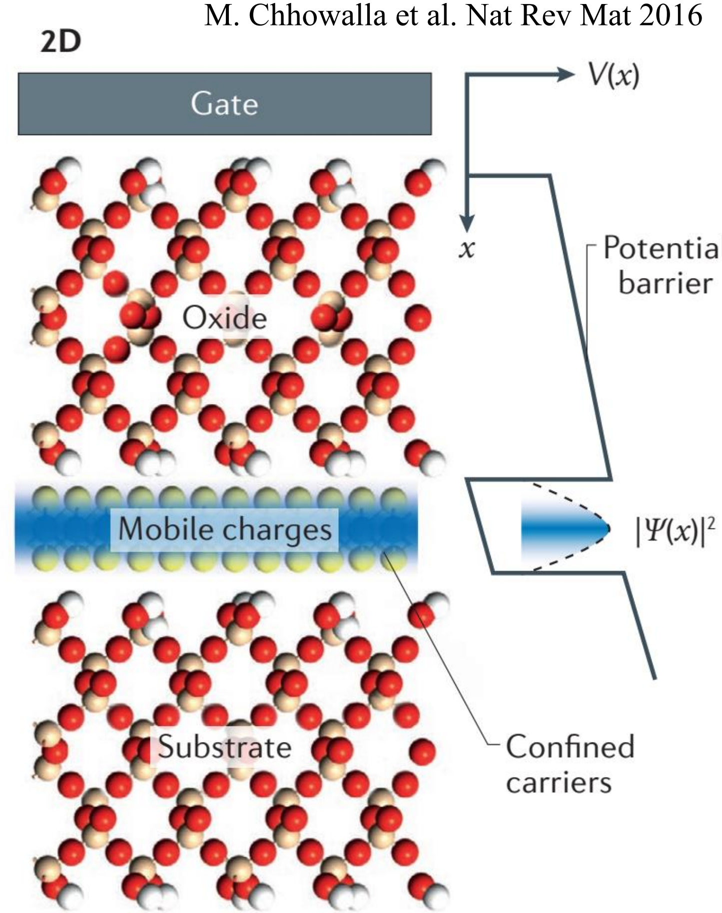
D. Akinwande *et al.* Nature 2019, 573, 507

Advantages of 2D materials compared with 3D materials for FET

M. Chhowalla et al. Nat Rev Mat 2016

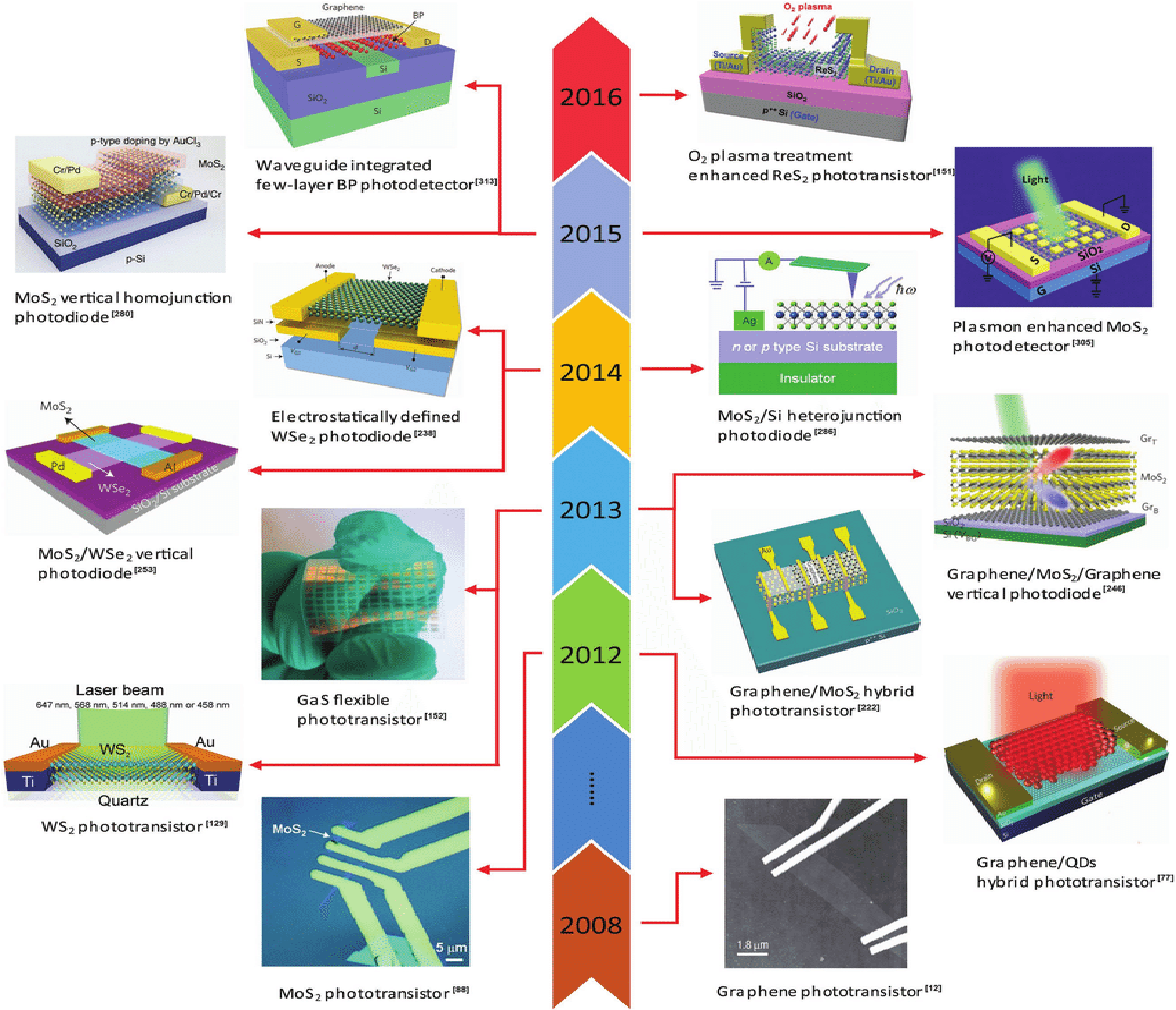






M, decreases with thickness to the sixth power, $\mu \sim t^6$
*E*g, increases by the square of the thickness, $\Delta E_g \sim t^2$

- 3D materials: dangling bonds that form traps for electrons and reduce the performance FETs
- 2D materials: Charge carriers are confined, excellent gate electrostatics



2016
2015
2014
2013
2012
2008
Graphene
BP
Waveguide integrated few-layer BP photodetector[313]
O2 plasma
Source (Ti/Au)
ReS2
Drain (Ti/Au)
p++ Si (Gate)
O2 plasma treatment enhanced ReS2 phototransistor[151]
p-type doping by AuCl3
MoS2
Cr/Pd
Cr/Pd/Cr
p-Si
MoS2 vertical homojunction photodiode[280]
Light
Plasmon enhanced MoS2 photodetector[305]
Anode
WSe2
Cathode
Electrostatically defined WSe2 photodiode[238]
n or p type Si substrate
Insulator
Ag
MoS2/Si heterojunction photodiode[286]
Pd
Au
SiO2/Si substrate
MoS2/WSe2 vertical photodiode[253]
Graphene/MoS2/Graphene vertical photodiode[246]
GaS flexible phototransistor[152]
Graphene/MoS2 hybrid phototransistor[222]
Laser beam
647 nm, 568 nm, 514 nm, 488 nm or 458 nm
WS2
Ti
Quartz
WS2 phototransistor[129]
Source
Drain
Gate
Graphene/QDs hybrid phototransistor[77]
5 μm
MoS2 phototransistor[88]
1.8 μm
Graphene phototransistor[12]

Practice Questions

Q 11.1 For germanium at 25°C, estimate (a) the number of charge carriers, (b) the fraction of the total electrons in the valence band that are excited into the conduction band, and (c) the constant n_0

$$n = n_i = p_i = n_0 \exp\left(\frac{-E_g}{2k_B T}\right)$$

$\rho = 43\ \Omega \cdot \text{cm},\ \therefore \sigma = 0.0233\ \Omega^{-1} \cdot \text{cm}^{-1}$

$E_g = 0.67\,\text{eV},\ \mu_n = 3900\ \frac{\text{cm}^2}{\text{V}\cdot\text{s}},\ \mu_p = 1900\ \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$

Q 11.2 The electrical conductivity and electron mobility for aluminum are 3.8×10^{7} $(\Omega\cdot\text{m})^{-1}$ and 0.0012 $\text{m}^2/\text{V}\cdot\text{s}$, respectively. Calculate the Hall voltage for an aluminum specimen that is 15-mm thick for a current of 25 A and a magnetic field of 0.6 tesla (imposed in a direction perpendicular to the current).

Q 11.3 Design a *p*-type semiconductor based on silicon, which provides a constant conductivity of 100 $\text{ohm}^{-1} \cdot \text{cm}^{-1}$ over a range of temperatures. Compare the required concentration of acceptor atoms in Si with the concentration of Si atoms.

Q 11.4 An extrinsic *p*-type silicon material is desired having a room-temperature conductivity of 50 $(\Omega\cdot\text{m})^{-1}$. Specify an acceptor impurity type that may be used, as well as its concentration in atom percent, to yield these electrical characteristics.

Q 11.5 Assuming that all of the valence electrons contribute to current flow, (a) calculate the mobility of an electron in copper and (b) calculate the average drift velocity for electrons in a 100 cm copper wire when 10 V are applied. $a_{FCC} = 3.6151 \times 10^{-8}$ cm $\quad \sigma = 5.98 \times 10^5\ \Omega^{-1} \cdot \text{cm}^{-1}$

Q 11.6 Consider a parallel-plate capacitor having an area of 6.45×10^{-4} m^2 (1 in.^{2}) and a plate separation of 2×10^{-3} m (0.08 in.) across which a potential of 10 V is applied. If a material having a dielectric constant of 6.0 is positioned within the region between the plates, compute the following:

(a) The capacitance
(b) The magnitude of the charge stored on each plate
(c) The dielectric displacement *D*
(d) The polarization