

Project Report on LNA at 1.575 GHz



Contributors :

22ECB0A13 - Swarup Vikrant Shinde

22ECB0A18 - Manik Sultania

22ECB0A31 - Rohit Raj Gupta

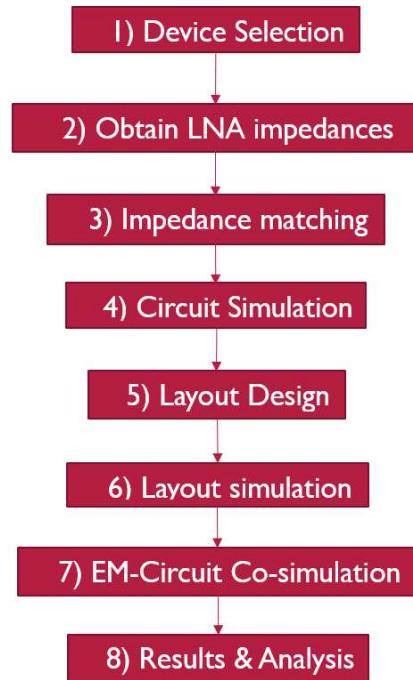
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1.1. Introduction

This report presents a comprehensive step-by-step methodology for designing a Low Noise Amplifier (LNA), specifically targeting the ISM band operating at 1.575 GHz. While the design outlined focuses on this frequency range, the principles and techniques discussed are applicable to LNA design across other frequency bands as well.

The LNA design process consists of eight major steps, as summarized in Table 1.1. The process begins with the selection of a suitable active device, followed by the determination of the LNA's input and output impedances. The next step involves impedance matching, essential for optimal performance. Subsequently, circuit design and simulation are carried out. This is followed by layout design, layout simulation, and EM-circuit co-simulation. Finally, the simulation results are analyzed. It is important to note that this report does not include hardware measurement or correlation between simulated and measured results; these aspects may be considered in future work.



Circuit Flow

1.2. Low Noise Amplifier (LNA): Introduction

This section begins with an overview of the Low Noise Amplifier (LNA) and its role within a typical RF radio system.

As illustrated in **Figure 1.1**, a standard RF radio system comprises several key components, including a baseband processor, up/down-conversion mixers, Voltage-Controlled Oscillator (VCO), Local Oscillator (LO) or Frequency Generating Unit (FGU), pre-driver, driver, power amplifier (PA), coupler, power controller, antenna switch, harmonic filter, antenna, pre-selector and post-selector filters, and the LNA. Each of these elements plays a vital role in enabling efficient wireless transmission and reception of information over long distances.

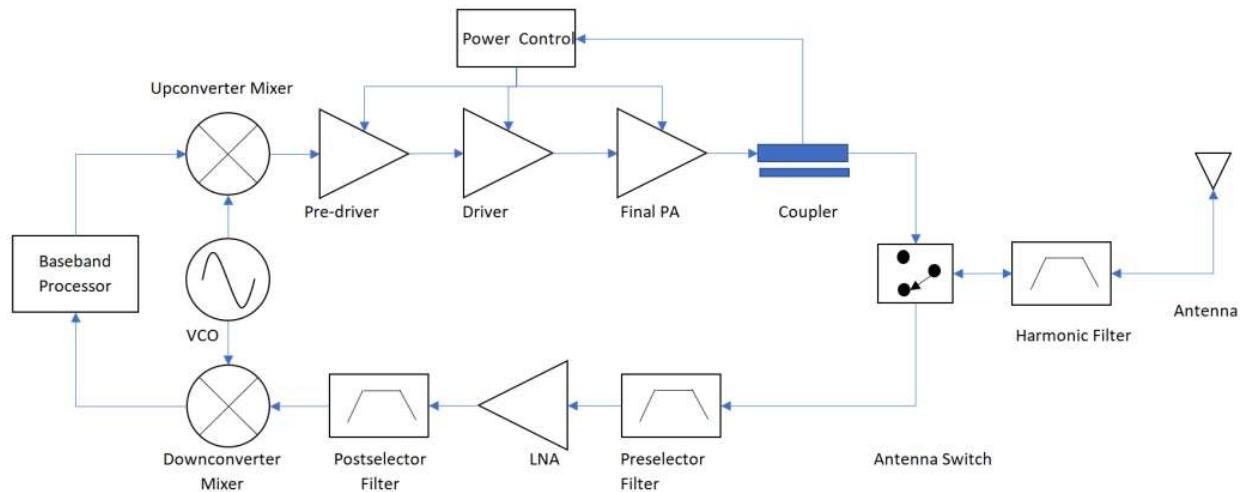


Figure 1.1: Basic RF Radio System Block Diagram

The LNA is positioned at the beginning of the receiver chain, as shown in **Figure 1.2**. The signal captured by the antenna is first directed through an antenna switch to the receiver path. A preselector filter eliminates unwanted out-of-band frequencies before the signal reaches the LNA. The LNA then amplifies the weak incoming signals while introducing minimal additional noise. The amplified signal is further processed by the post-selector filter before being passed to the down-conversion mixer and ultimately to the baseband processor.

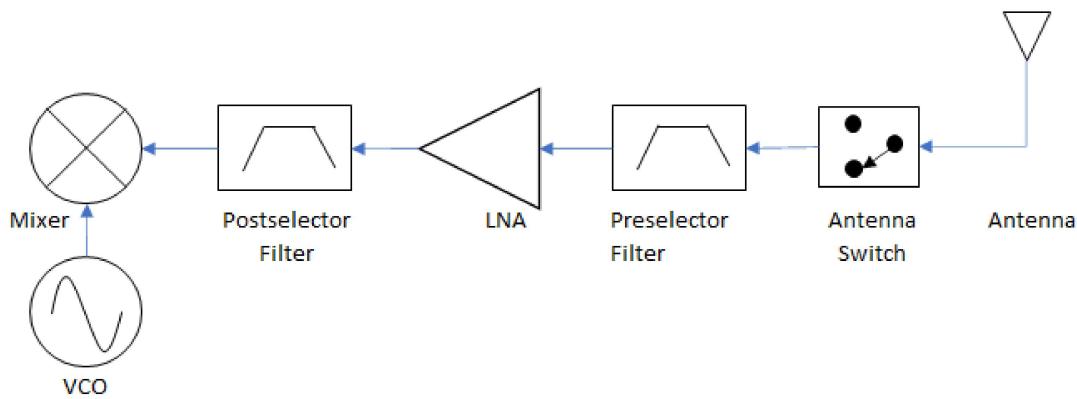


Figure 1.2: Low Noise Amplifier (LNA) within the Receiver Chain

Beyond amplification, the LNA also provides isolation between the mixer and the antenna. However, since the LNA itself contributes a certain level of noise to the system, it directly impacts the receiver's sensitivity and intermodulation distortion. Therefore, a key design challenge is to minimize the noise figure of the LNA while achieving sufficient gain and maintaining overall efficiency.

1.2.1. LNA Implementation Approaches

Two ways of implementing an LNA are Discrete and integrated Circuit Implementation. Each implementation has its advantages and disadvantages. Table 1.2 lists the characteristics of a Discrete LNA vs. an Integrated Circuit LNA, whereas Table 1.3 exhibits the characteristics of an Integrated LNA compared to Discrete LNA.

ADVANTAGE	DISADVANTAGE
Inexpensive implementation	Lower reliability compared to IC
Can be repaired if design not meeting goal during bench testing	Limited bandwidth compared to IC
Low transmission line loss compared to IC	Uncontrolled parasitics
Higher components Q	Large size
Wide variety of components / lumped elements	High assembly cost
	Limited to low frequency

Table 1.2: Characteristics of a Discrete LNA vs. Integrated Circuit (IC) LNA

Next, this table shows the characteristics of an Integrated Circuit LNA vs. Discrete LNA.

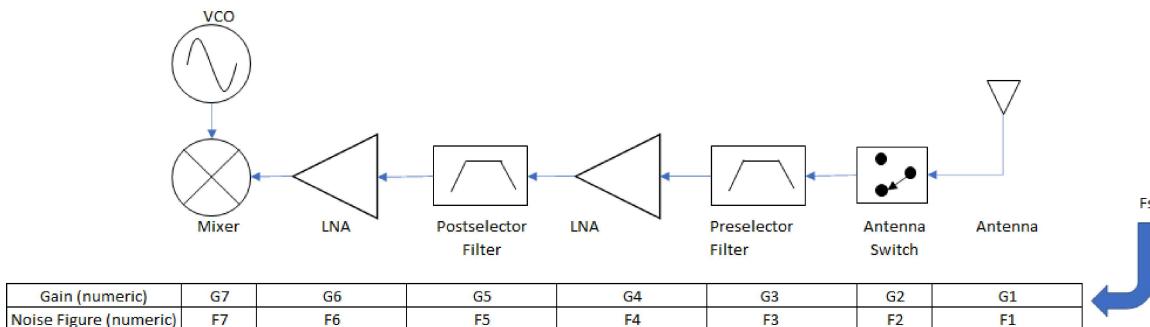
ADVANTAGE	DISADVANTAGE
Small Size and Weight	High cost compared to PCB implementation in small quantities.
Broader bandwidth	No Tuning
Design Flexibility because we can design whatever value of lumped components we want.	Higher transmission line losses
Improved reliability	Undesired RF coupling
Good reproducibility	High Equipment cost
Lower cost in volume	Limited component values are available. Custom components can be designed but at a higher cost.
Very broad Frequency for MMIC	

Table 1.3: Characteristics of an Integrated Circuit (IC) LNA vs. Discrete LNA

Even though there are two ways of implementing LNA, both are relevant. The designer can choose one according to the product specification or application. For our application, we will be moving ahead with Discrete LNA implementation.

1.2.2. Cumulative Noise Figure by Friis's Equation

Friis's equation is an essential formula that enables us to calculate the receiver sensitivity. We can also calculate the IP3 and IP2 of a receiver chain. However, since we are focusing on LNA design only in this training, I will stop at the cumulative noise figure. Figure 1.3 shows the receiver chain. The numeric gain and the noise figure of each component on the receiver chain are below that.



Friis's formula is used to compute the overall noise figure of a cascaded system comprising multiple stages, where each stage contributes its own noise figure and gain. This calculation assumes that the impedance is matched at the input and output of each stage for accurate results.

The equation for the total noise figure F_s is given by:

$$F_s = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \dots + \frac{F_n - 1}{G_1 G_2 \dots G_{n-1}}$$

Equation 1.1

Here, F_1 is the noise figure of the first stage, and G_1, G_2 , etc., represent the power gains of the respective stages. Among all terms, the first stage's noise figure F_1 is the most significant since it is not divided by any gain factor. Consequently, minimizing the noise figure of the initial stage—typically the Low Noise Amplifier (LNA) is critical in optimizing the overall receiver noise performance.

1.2.3. Types of Noise in Receiver Systems

Noise represents a fundamental limitation in receiver design. It is introduced by both passive and active components and can significantly degrade system performance. The six primary types of noise found in electronic receivers are as follows:

1.2.3.1 Thermal Noise

Also known as Johnson–Nyquist noise, thermal noise is inevitable and results from the random thermal motion of electrons in a conductor. It occurs regardless of any applied voltage and has a flat (white) power spectral density across frequencies. Its amplitude follows a Gaussian distribution. Communication systems impacted by thermal noise are typically modeled as **Additive White Gaussian Noise (AWGN)** channels.

1.2.3.2 Shot Noise

Shot noise arises due to statistical fluctuations in electric current as discrete charge carriers (such as electrons) cross a potential barrier, such as in a diode. These carriers arrive randomly, producing current variations. The **Schottky formula** defines the RMS value of shot noise current:

$$i_n = \sqrt{2I_q \Delta B}$$

Equation 1.2

Shot noise is typically absent in resistors, where electron motion is diffusive, but may be observed in mesoscopic resistors under certain conditions.

1.2.3.3 Flicker Noise

Also referred to as **1/f noise**, flicker noise exhibits a power spectral density that inversely varies with frequency. It is prevalent in nearly all active electronic components and is associated with DC current flow.

1.2.3.4 Partition Noise

This type of noise arises when electrical current splits into multiple paths, causing random fluctuations. Transistors exhibit partition noise, which is typically higher than the combined shot noise of their individual PN junctions.

1.2.3.5 Burst Noise

Burst or **popcorn noise** appears as sudden, step-like changes in voltage or current, which persist for milliseconds to seconds. These irregular transitions can produce audible popping sounds in audio circuits.

1.2.3.6 Transit-Time Noise

At very high frequencies (e.g., above VHF), the electron transit time in a transistor becomes comparable to the signal's period. This leads to **transit-time noise**, which increases with frequency and can surpass other noise sources. It also causes the noise input impedance to decrease.

1.2.4 LNA Stage vs. Nonlinear Receiver Line-Up Specifications

The overall receiver architecture, including antenna, filters, LNA, and mixer, is characterized using **nonlinear receiver line-up simulations**, typically performed using **Keysight SystemVue**. These simulations help evaluate:

- Input/output power at each stage
- Gain and noise figure
- Linearity parameters such as IP2 and IP3
- Receiver sensitivity and efficiency

SystemVue allows simulation across multiple power modes and worst-case operating conditions, such as minimum power levels and maximum current consumption, to ensure robust receiver design.

1.2.5 Key Parameters of LNA (Simulated Using Keysight ADS)

The essential LNA parameters evaluated are:

- **Pin_RF**: RF input power to the LNA
- **S(2,1)**: Small-signal gain
- **Noise Figure**: Indicates the noise introduced by the LNA
- **P1dB**: 1-dB compression point, indicating the power level where the amplifier starts to compress and deviate from linearity.
- **S(1,1) & S(2,2)**: Input and output return losses, indicating matching quality
- **S(1,2)**: Reverse isolation, showing the level of feedback from output to input
- **RFfreq**: Operating frequency range

Stability-related parameters include:

- **μload & μsource**: Stability factors
- **Real Part of Driving Point Admittance**
- **True Return Ratio (Loop Gain)**

These parameters collectively evaluate how stable the LNA remains under varying conditions such as temperature, voltage, load mismatch, and input power fluctuations.

1.2.6 Stability Considerations

LNA stability is crucial, as instabilities can cause the circuit to oscillate like an oscillator. Instability typically results from unintended feedback from the output to the input in-phase. Stability is assessed during the design phase by simulating stability factors (μ_{load} and μ_{source}) and performing advanced analyses using the **WS Probe** method.

WS Probe provides:

- **Driving Point Admittance Analysis**
- **Loop Gain (True Return Ratio) Analysis**

Common techniques to enhance stability include:

- Collector/base bypass capacitors
- RC-feedback networks (at the cost of gain at low frequencies)
- Input/output resistive loading (may impact noise figure and gain)
- Emitter feedback resistors (reduce high-frequency gain)

1.3 Device Selection

Device selection is a critical yet often underestimated step in the design process. The choice of device must align with the LNA stage requirements, which are typically derived from the transmitter line-up or overall system specifications.

1.3.1 Design Specifications

Before selecting a suitable device, clear design specifications for the LNA must be established. These specifications are usually defined based on the transmitter line-up, which is generally managed by a technical lead or project manager. Design engineers use these specifications as a reference to implement the LNA stage accordingly.

For this tutorial, the focus is on designing an LNA with the following key specifications:

- **Frequency:** 1.575 GHz
- **Bandwidth:** 25 MHz
- **Noise Figure:** <1.5 dB
- **Gain:** >40 dB
- **Input and Output Return Loss:** >10 dB

- **1 dB Compression point:** >0 dBm

These parameters serve as the foundation for selecting a suitable active device and guiding the design process.

1.3.2 Understanding Device Technology

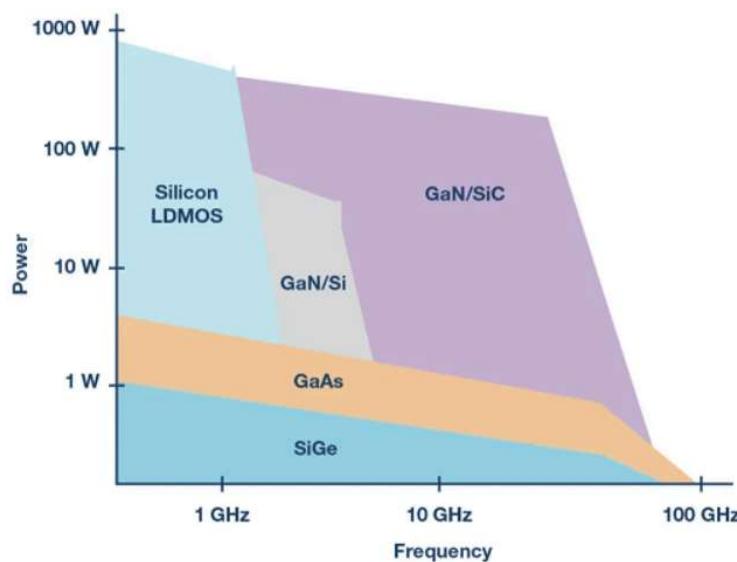
A solid understanding of device technology is essential for selecting the right component for the Driver LNA stage. Since the device selection is one of the most critical steps in the design process, it must align closely with the specifications of the LNA stage.

The graph provided (sourced from Analog Devices) illustrates how device technology varies with power level and operating frequency. For low-power applications (less than 1W), **SiGe** is the most appropriate choice. When operating in the **1W to 6W power range** and at frequencies up to **100 GHz**, **GaAs** is a better fit.

For higher power levels (above 6W), technologies such as **Silicon LDMOS**, **GaN on Silicon (GaN/Si)**, and **GaN on Silicon Carbide (GaN/SiC)** become relevant.

- **Silicon LDMOS** is preferred for high-power, low-frequency applications.
- **GaN/Si** is well-suited for high-power, mid-frequency ranges.
- **GaN/SiC** performs best in high-power, high-frequency scenarios.

Apart from power and frequency, **supply voltage** is another key factor in device selection. Different technologies operate across a wide supply voltage range, typically from **2V to 50V**, which must also be considered during selection.



Got it! Here's the revised version of **Sections 1.3.3 and 1.3.4** with the updated frequency **1.575 GHz** for your selected device **ATF-21170 GaAs FET**:

1.3.3 Parameters of Selected Device

For our Driver LNA design operating at **1.575 GHz**, the **ATF-21170**, a GaAs FET from Avago Technologies (Broadcom), has been selected as the most suitable active device. This choice is based on its excellent performance in terms of low noise, moderate gain, and high linearity—meeting the core specifications required for the LNA stage.

The specifications suggest that the ATF-21170 can deliver the desired performance in terms of noise, gain, and linearity, making it ideal for LNA operation at 1.575 GHz.

1.3.4 Device Model Selection

For simulation and design validation in ADS, it is essential to use a reliable and accurate model of the ATF-21170. The manufacturer provides S-parameters and nonlinear models compatible with ADS, which are necessary for realistic circuit simulation.

To ensure the accuracy of the model, the following validation methods are used:

1. **Impedance Matching** – Comparing the simulated input and output impedance with the values extracted from the S-parameter data.
2. **IV Curve Validation** – Simulating the device's IV characteristics and matching them with the datasheet plots.

1.3.4.IV CURVE SIMULATION IN ADS

In addition to the previously discussed methods, the DC characteristic curve (Ic vs. Vce) serves as a reliable parameter for selecting the most accurate device model.

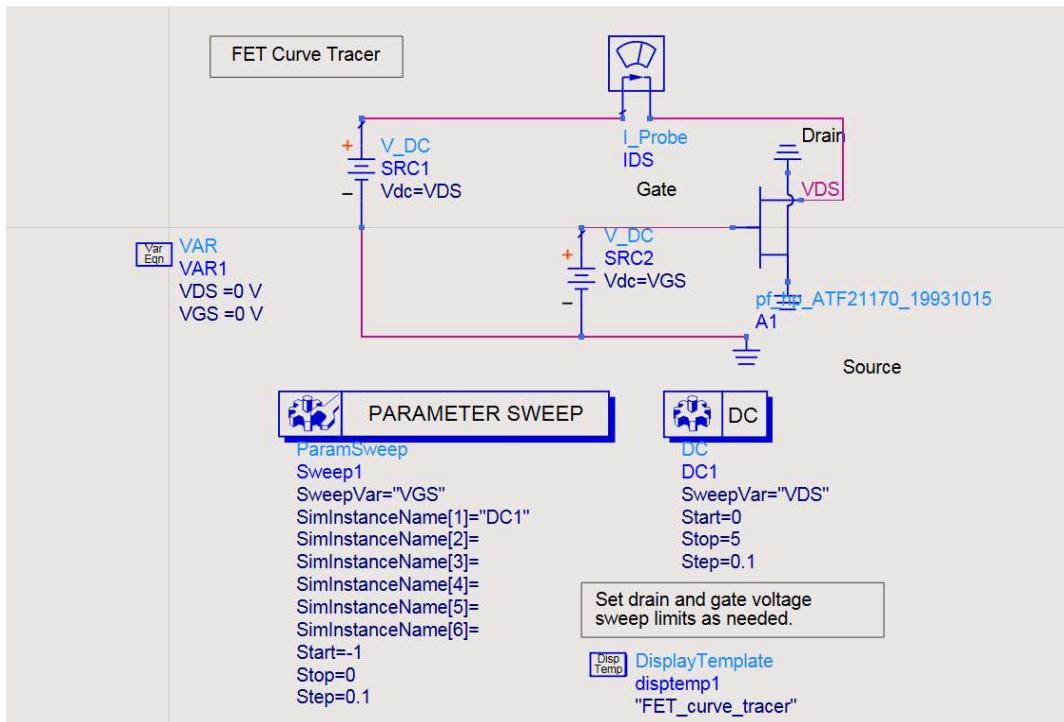


Fig:Circuit Diagram for FET Curve Tracer for ATF21170 FET

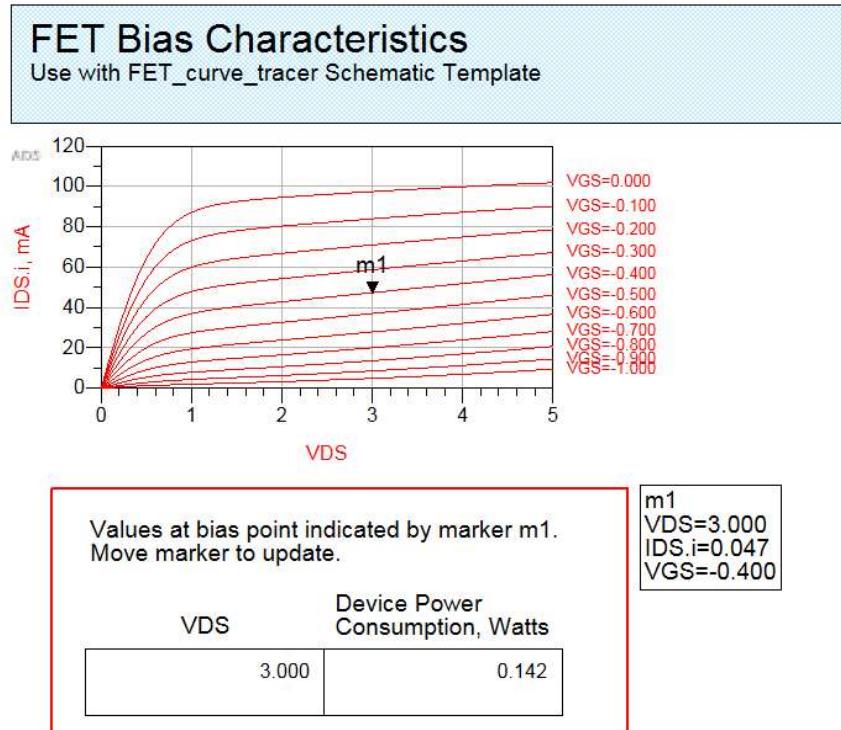


Fig:Simulation for IV Characteristics

1.4 Impedance Matching

After determining the input and output impedances, the next step is to match them to the standard 50-ohm system impedance. This involves matching both the input and output of the LNA to 50 ohms. The impedances obtained from the previous simulation represent the complex conjugates of the actual LNA impedances, denoted as Z_i^* and Z_o^* in Figure 1.18. Therefore, to obtain the true LNA impedances, the sign of the imaginary components must be reversed.

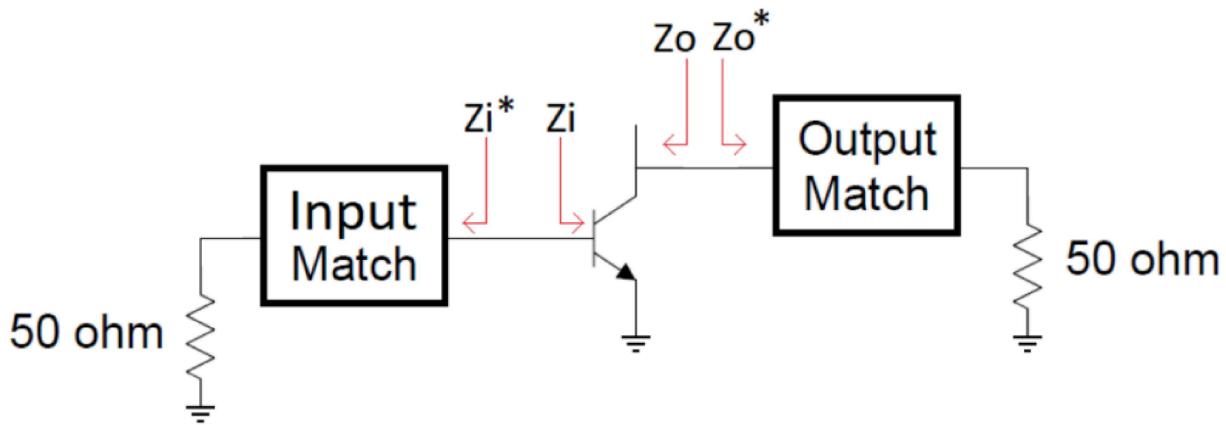


Figure: The LNA impedances matching

Z_o^* – complex conjugate of output impedance

Z_i^* – complex conjugate of input impedance

Z_o – Transistor output impedance

Z_i – Transistor input impedance

1.5 Circuit Simulation

The next step is circuit simulation. Before running the simulation, the LNA circuit must be constructed. The complete LNA schematic is shown in Figure 1.21. The matching component values obtained from Step 3 are used in this schematic to match the input and output to 50 ohms.

In addition to the matching network, the LNA circuit also includes a biasing network. The biasing circuit supplies the required collector-emitter voltage (V_{ce}) and base-emitter current (I_{be}) to properly bias the transistor.

Decoupling capacitors are included to filter out any noise present in the DC supply lines. RF chokes are used to prevent RF signals from leaking into the DC paths. DC-blocking capacitors are added to the input and output matching networks to prevent DC from entering the RF path.

Figure 1.25 shows the LNA IP3 (Third-Order Intercept Point) measurement setup. Two signals with a small frequency separation are injected into the Device Under Test (DUT), which is the LNA, and the output is monitored using a spectrum analyzer.

In this design, we inject two signals at 1.574 GHz and 1.576 GHz, resulting in a fundamental frequency of 1.575 GHz and a separation of 1 MHz. In some industry applications, this frequency gap may be even smaller, sometimes in the kHz range, depending on the radio specification. The input power level is set at -40 dBm for each tone.

The Output IP3 (OIP3) can be calculated using the IP3out component available in ADS. Two such components are used in the simulation to capture both the upper and lower third-order intermodulation products.

1.6 Results and Analysis

(A) Single Stage

The S-parameter and performance simulation results of the LNA circuit are illustrated in Figure 1.30. The design achieves a gain of approximately **11.8 dB at 1.575 GHz**, which falls within the desired operating frequency range of **1.57–1.58 GHz**. The maximum gain reaches **12.35 dB at 1.489 GHz**, and a minimum gain of **8.814 dB** is observed at 1.883 GHz, indicating good mid-band performance with acceptable roll-off outside the target band.

The **input return loss** at 1.489 GHz is **-15.92 dB**, and the **output return loss** at 1.575 GHz is **-11.124 dB**, suggesting that the design achieves effective impedance matching at both ports. An **isolation (S12)** of better than **-29 dB** is also evident, contributing to minimal reverse transmission and strong unidirectional performance.

The **Noise Figure (NF)** analysis shows a **minimum noise figure of 0.318 dB at 1.574 GHz**, and an **NFmin of 0.153 dB**, which is excellent and highly desirable in LNA applications where low noise is critical.

Figure 1.30 also includes the **stability analysis**, where the μ -parameter (Mu1) is **0.998 at 1.575 GHz**, very close to 1, indicating marginal but acceptable stability across the band. Additional simulation or layout tuning may be required for robust unconditional stability.

The **power sweep plot** (bottom right) shows the gain response versus input power (Pin), demonstrating good linearity with moderate gain compression as input power increases. This behavior helps assess the amplifier's dynamic range.

From the analysis, we conclude that the LNA meets essential design requirements, including adequate gain, low noise figure, good isolation, and acceptable input/output matching. Although the stability margin is close to the threshold, it remains within tolerable limits. The overall performance validates the design for use in low-noise applications around the GPS L1 band (~1.575 GHz).

CIRCUIT DIAGRAM

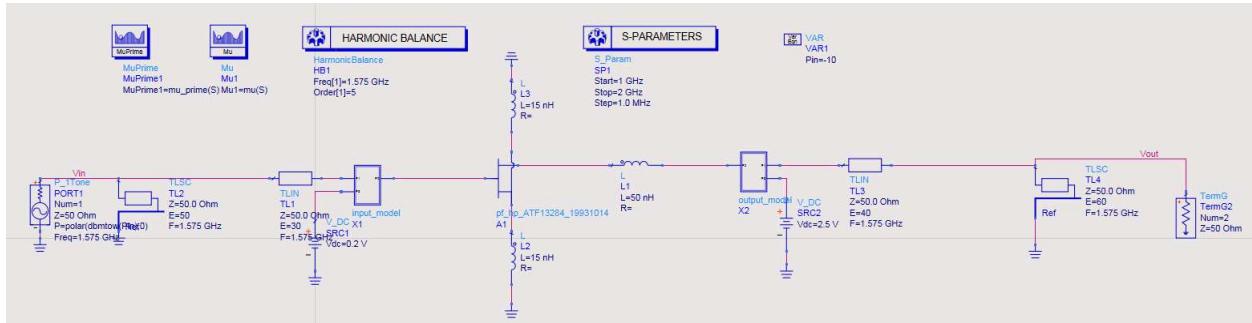


Fig:Circuit Diagram for LNA Design

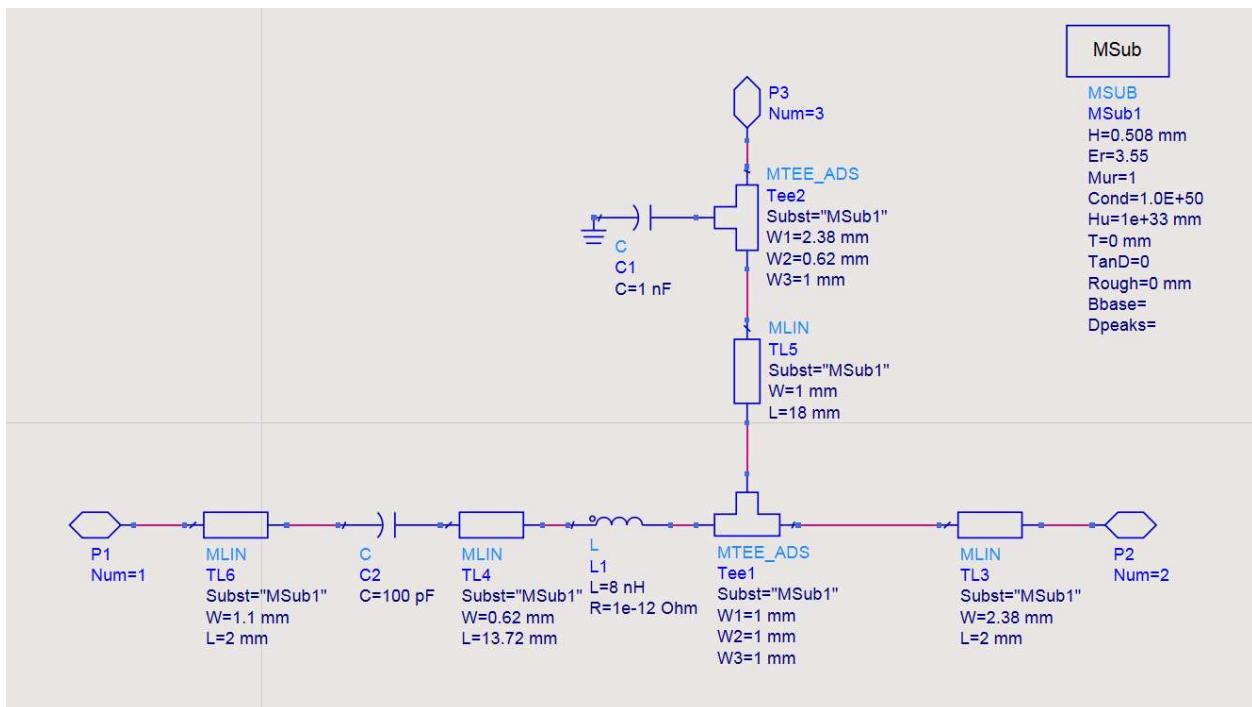


Fig:Circuit Diagram for INPUT Bias Network

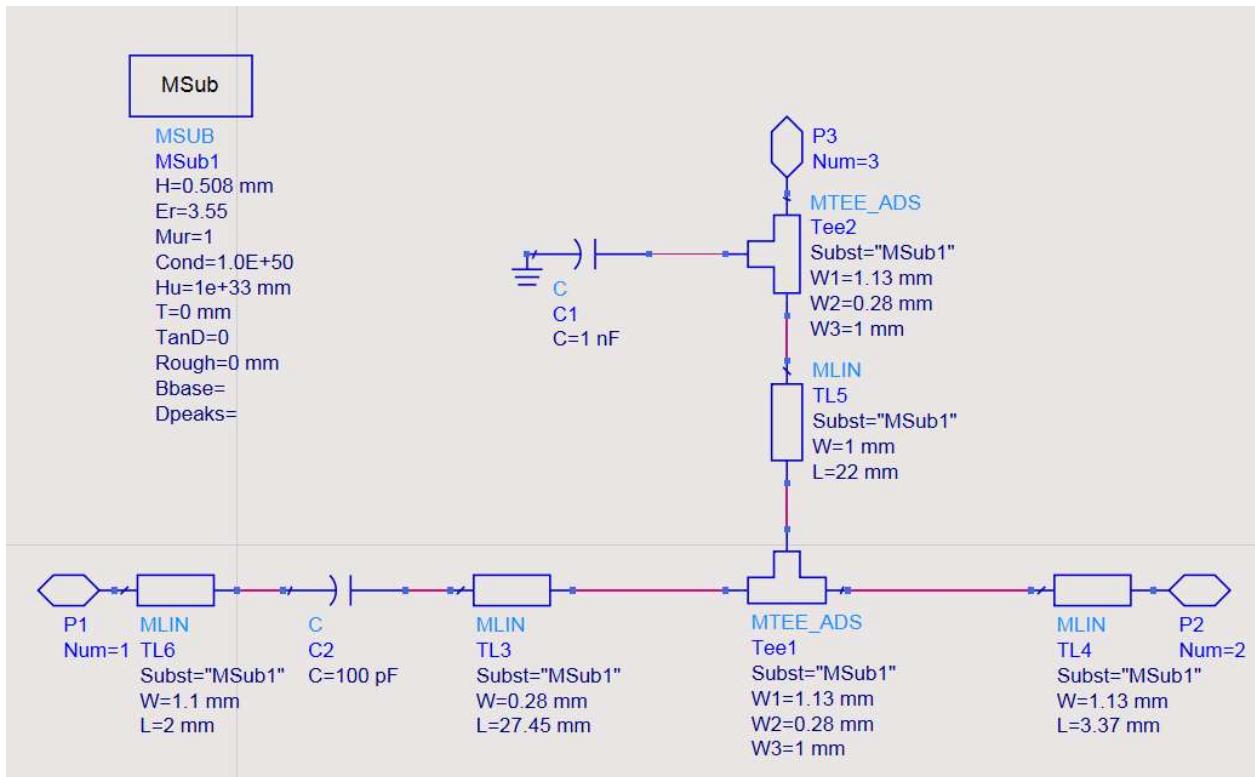


Fig:Circuit Diagram for OUTPUT Bias Network

SIMULATION

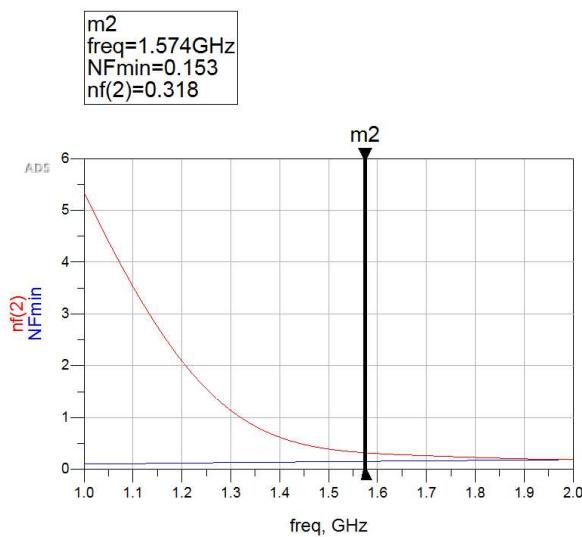


Fig:Noise Figure Simulation

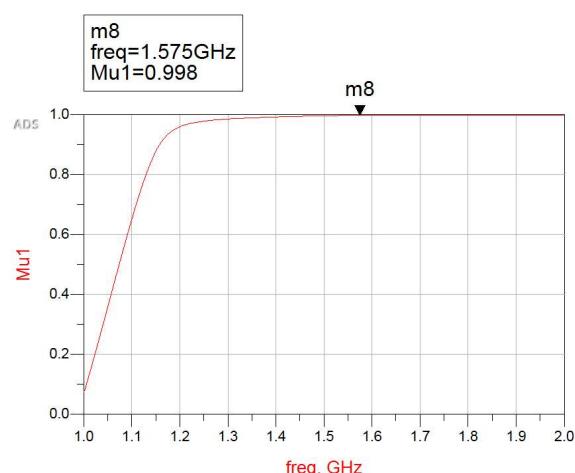


Fig:Stability Factor Simulation

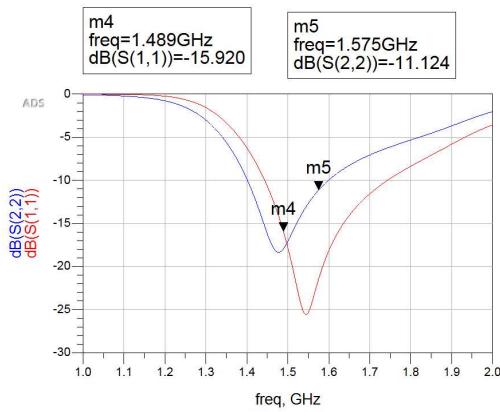


Fig:Input and Output Return Loss

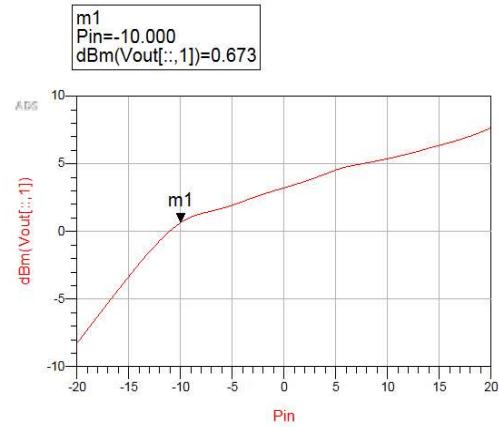


Fig:1 dB Compression Point

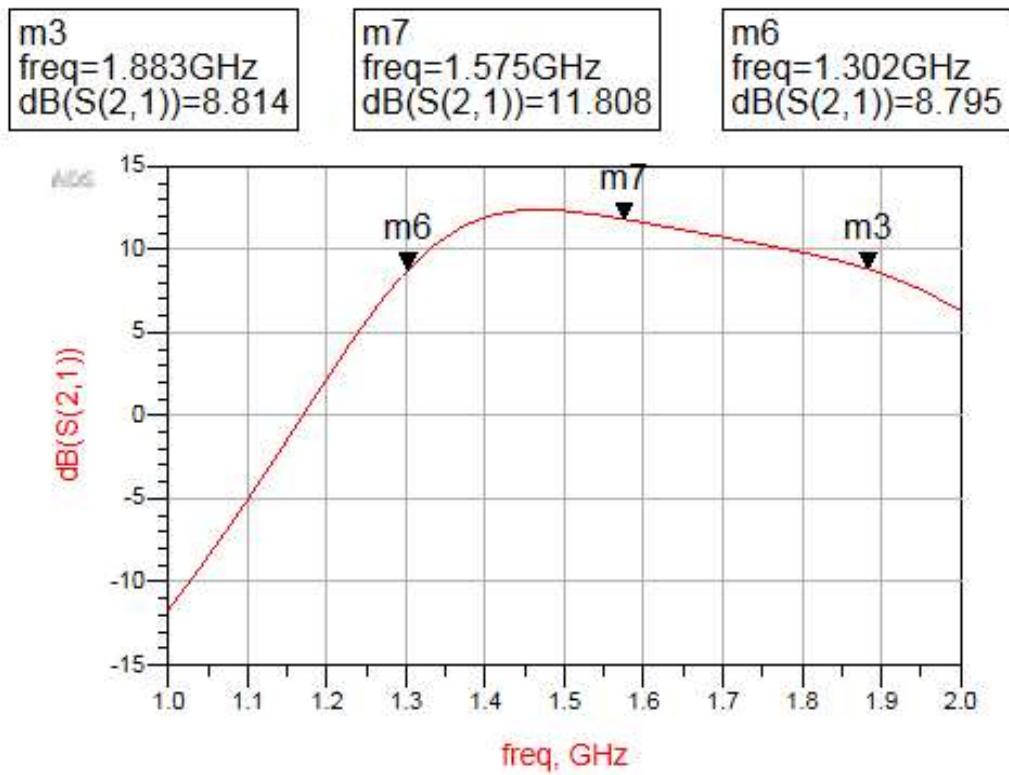


Fig:Power gain Simulation

Lower Cut Off Frequency(f_L):1.302 GHz

HigherCut Off Frequency(f_H):1.883 GHz

Bandwidth(BW)= $f_H-f_L=1.883-1.302=0.581$ GHz

(A) Multi Stage

CIRCUIT DIAGRAM

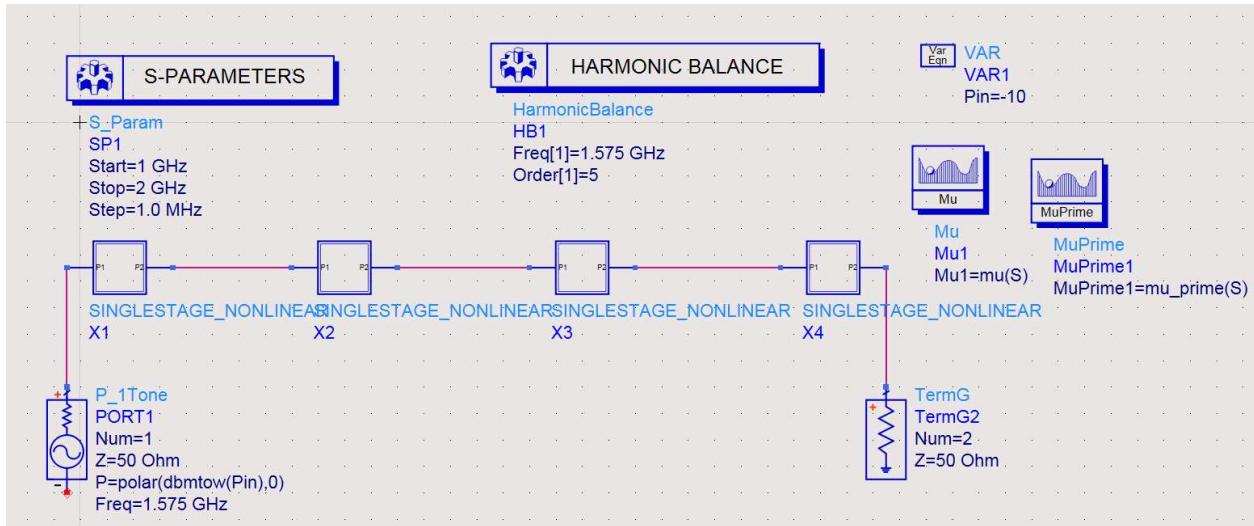


Fig:Circuit Diagram for LNA Design

SIMULATION

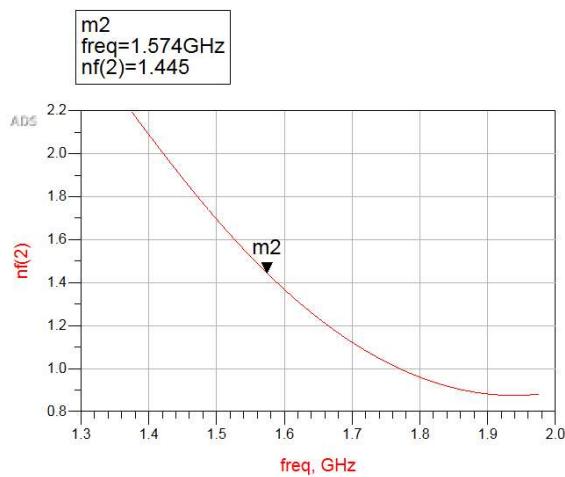


Fig:Noise Figure Simulation

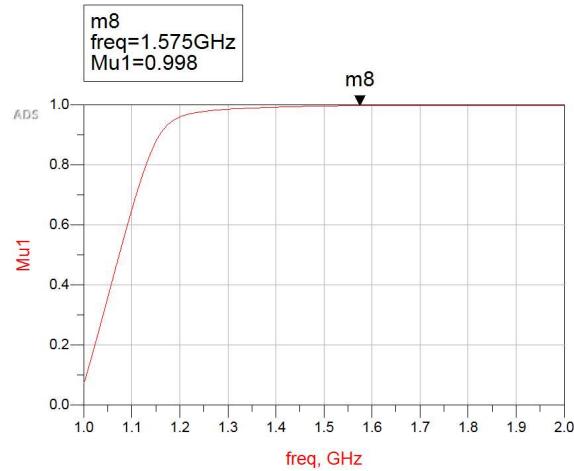


Fig:Stability Factor Simulation

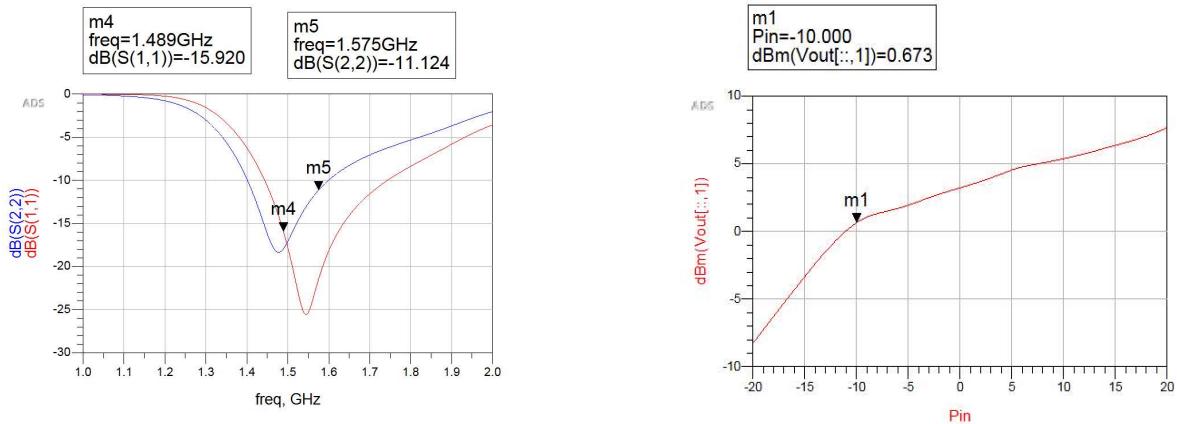


Fig:Input and Output Return Loss

Fig:1 dB Compression Point

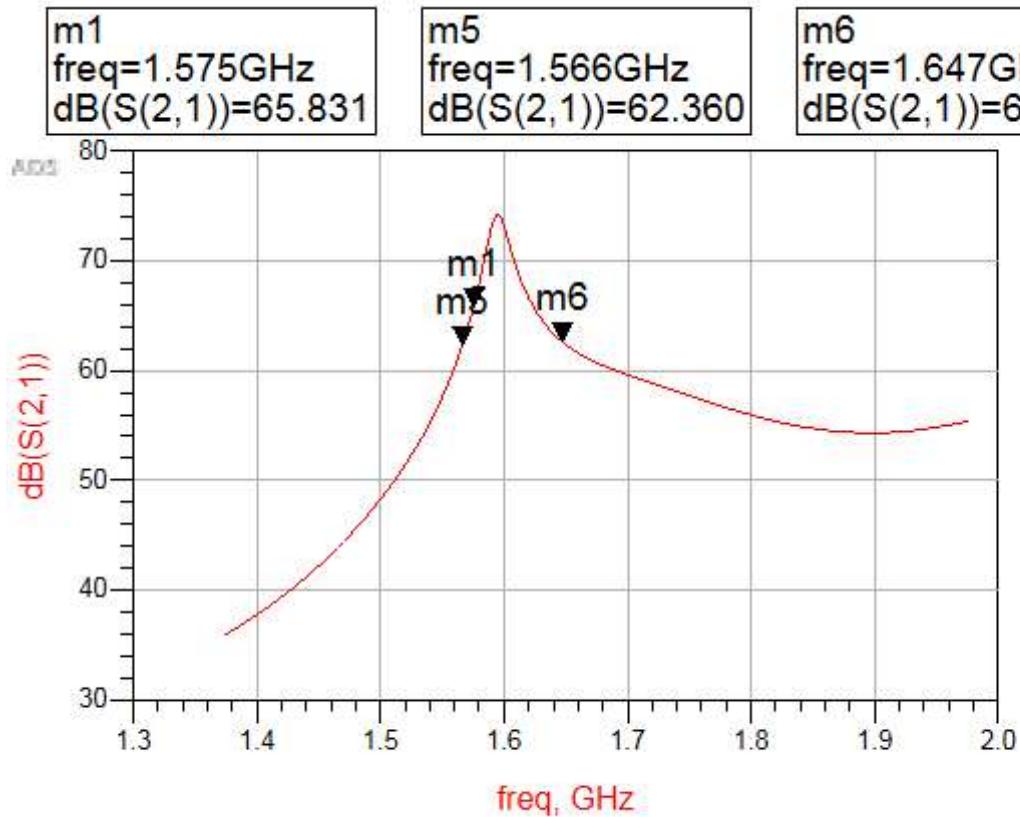


Fig:Power gain Simulation

Lower Cut Off Frequency(f_L): 1.566 GHz

HigherCut Off Frequency(f_H): 1.647 GHz

Bandwidth(BW) = $f_H - f_L = 1.647 - 1.566 = 0.081$ GHz