Design of a Bridge between RIFFA Channel Tester Module and the DDR3 SDRAM in ML605

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Feb 12, 2018

AHIR-MIG Bridge Module

We propose to have a Bridge module between the ahir-system and the memory controller user interface as explained before. The Bridge module will have one 64 bit input pipe called the Request pipe and one 64 bit output pipe called the Response pipe on the AHIR side of the interface.

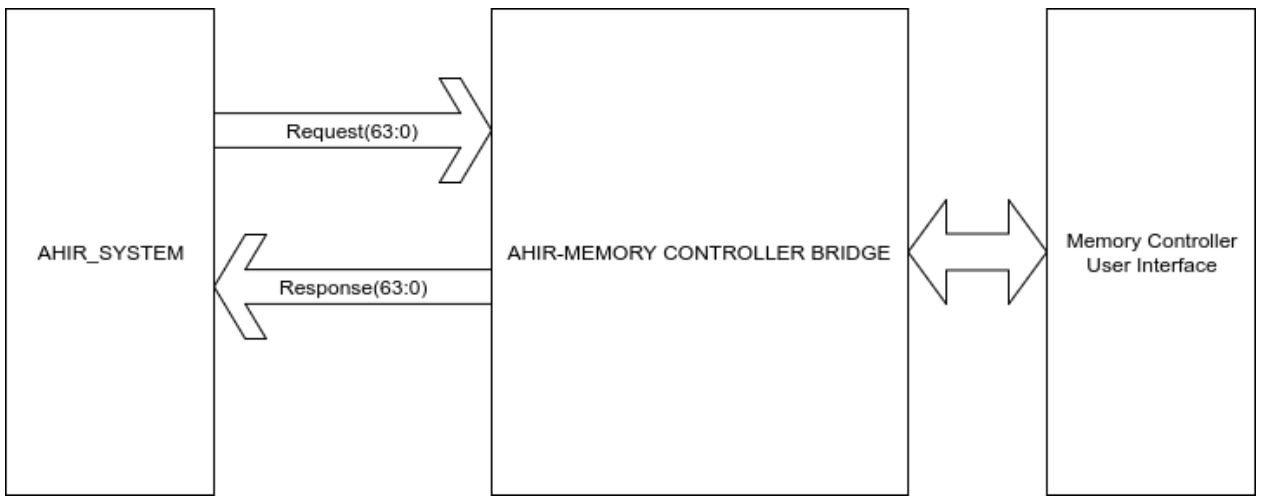

Figure : AHIR-MC Bridge

Parameter Specifications for the Current Design

- For a SODIMM DDR3 SDRAM, the data width is fixed at 64 bits.
- The address width is taken as 32 bits. However, 64 and 128 bit addresses may also be selected.
- The maximum burst length is fixed at 8.

AHIR-MIG Bridge Module

The Bridge interface on the AHIR System side is illustrated in the diagram below:

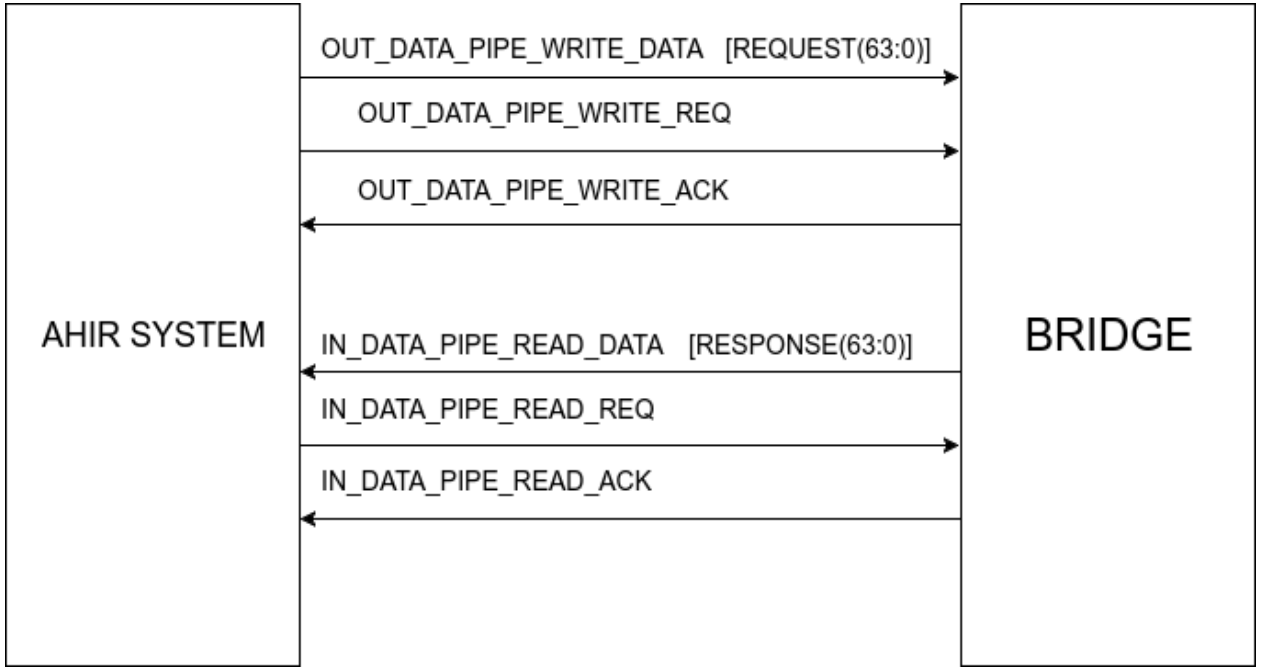

Figure : AHIR-MC Bridge

AHIR-MIG BRIDGE Module

The Bridge Interface on the Memory Controller Top side is showed in the diagram below:

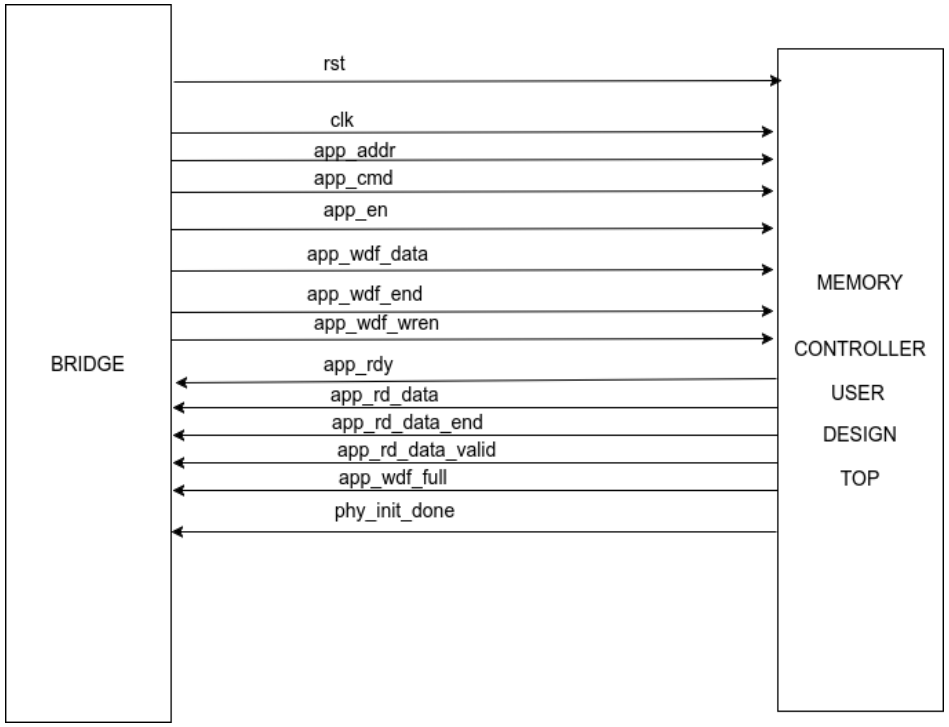

Figure : AHIR-MC Bridge

The Request Packet

The Request packet is a formatted header. Each packet is of 64 bits.

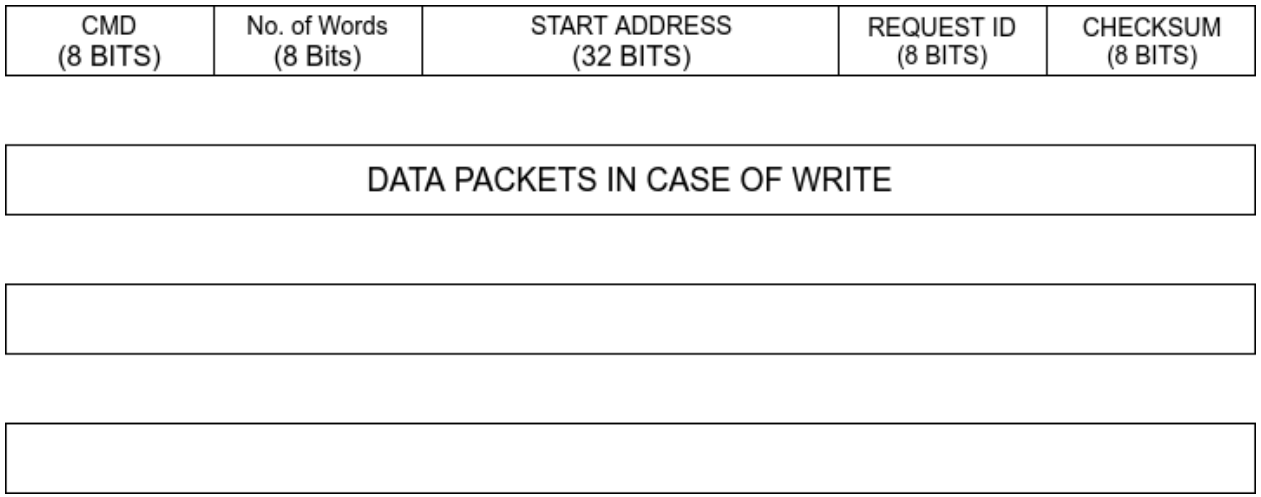

Figure : A Request Packet

Response Packet

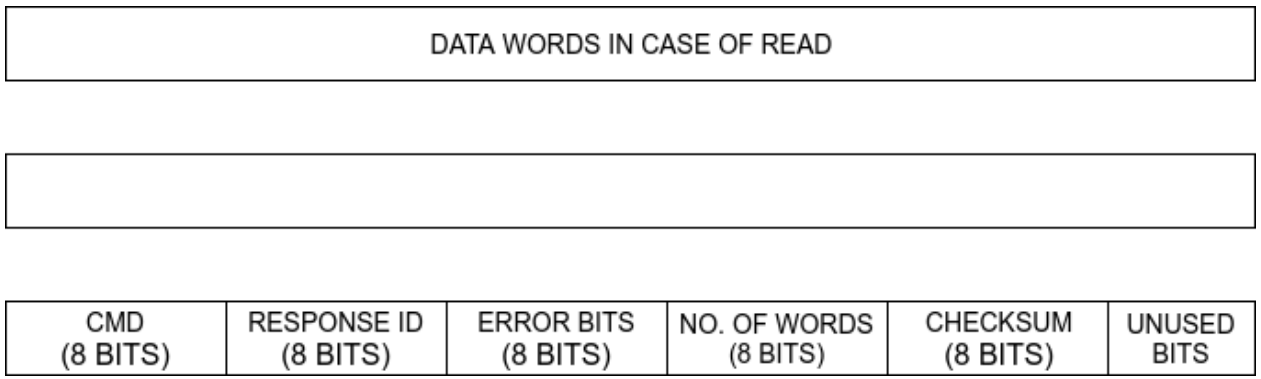

Figure : A Response Packet

Algorithm for the AHIR-System Module

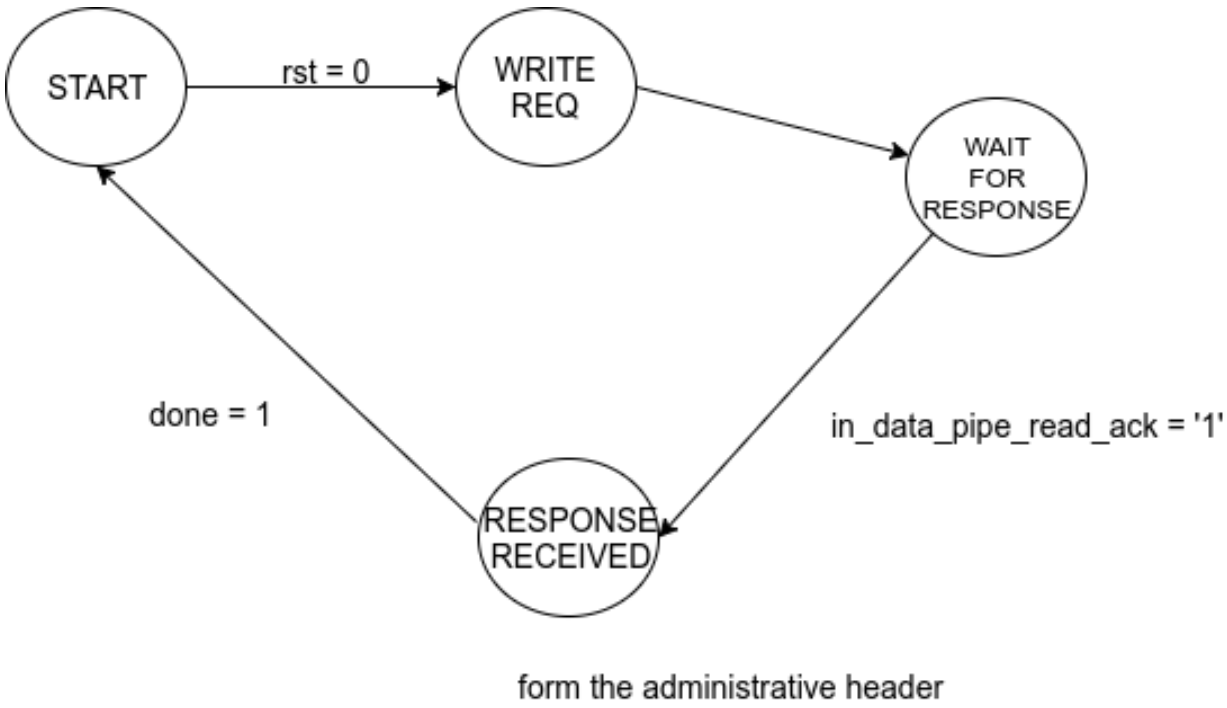

Figure : Ahir System

Algorithm for the Bridge Module

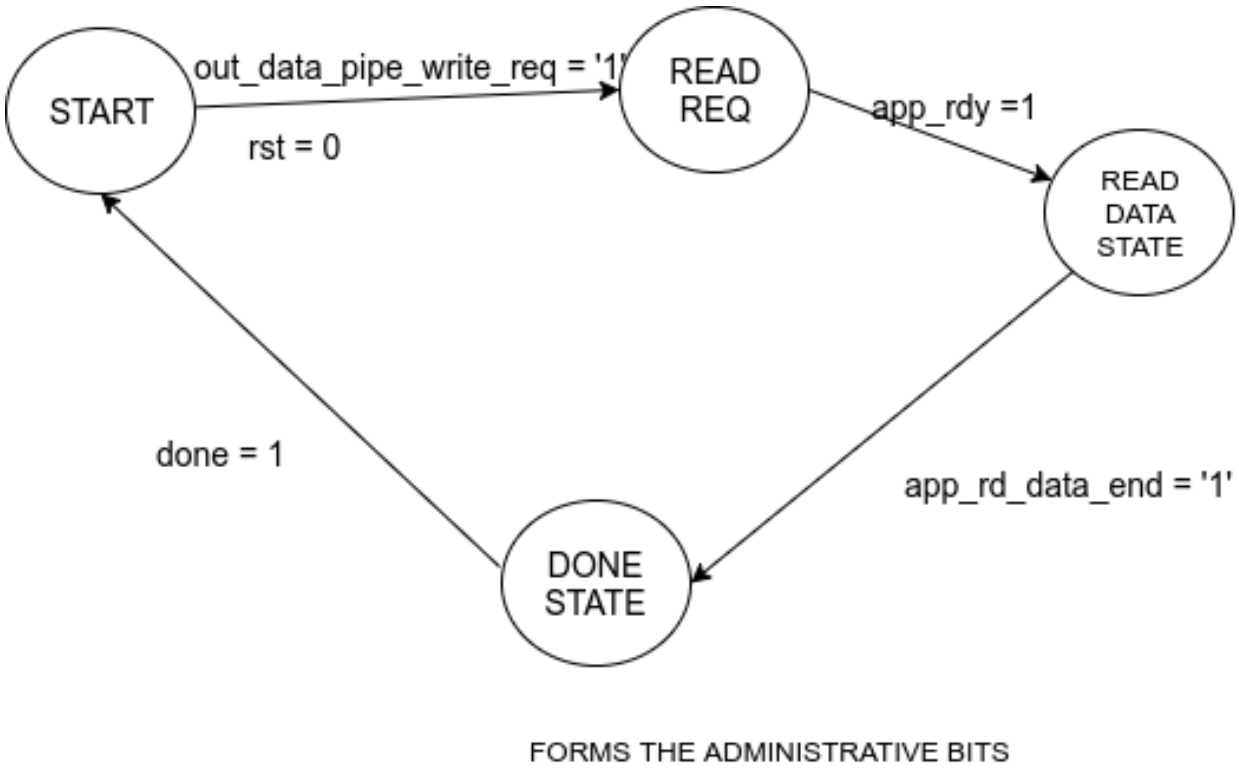

Figure : Ahir-MIG Bridge System

Simulation Results

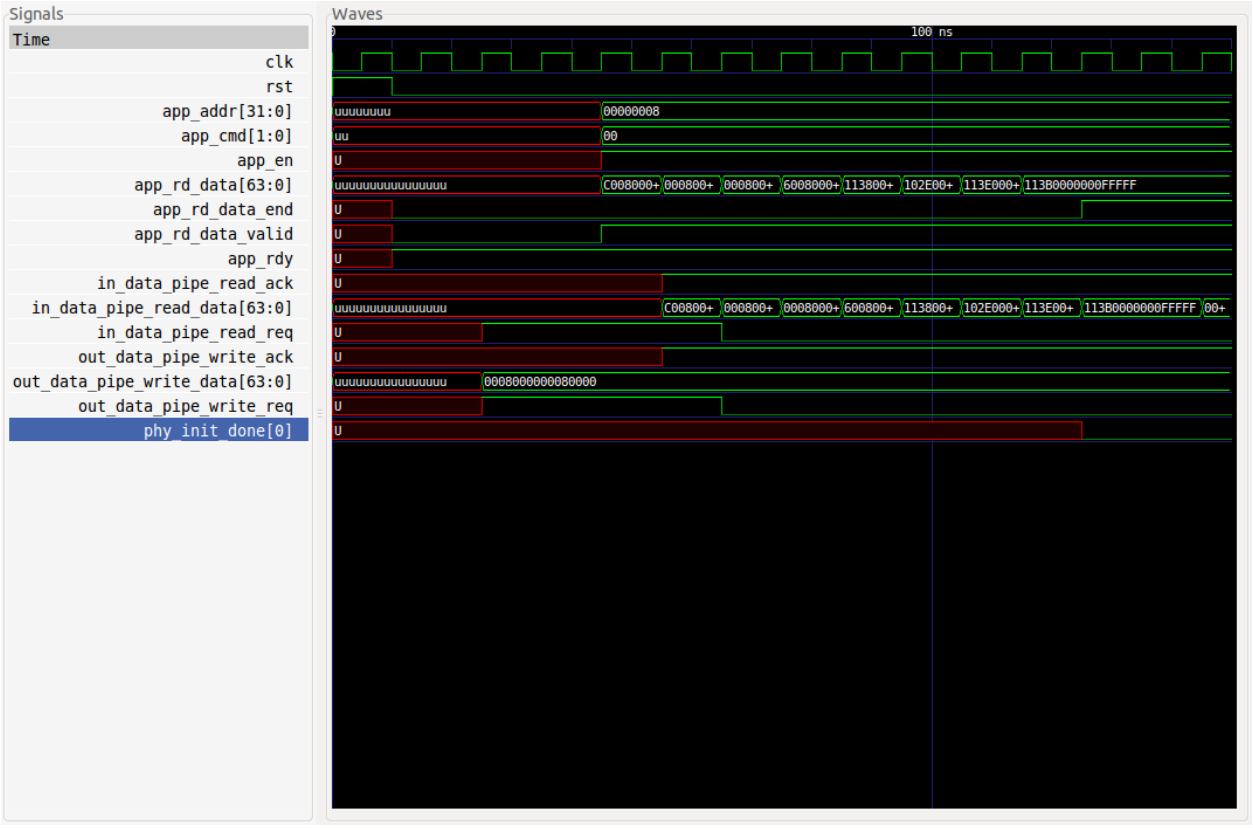

Figure : Ahir-System to Bridge Operation

References

1. https://forums.xilinx.com/t5/Memory-Interfaces/MIG-DDR3-example-design-init-calib-complete-never-goes-high/td-p/721154
2. https://www.xilinx.com/support/answers/34319.html