SRN | | | | | | | | | | | |

PES UNIVERSITY

PES University, Bangalore

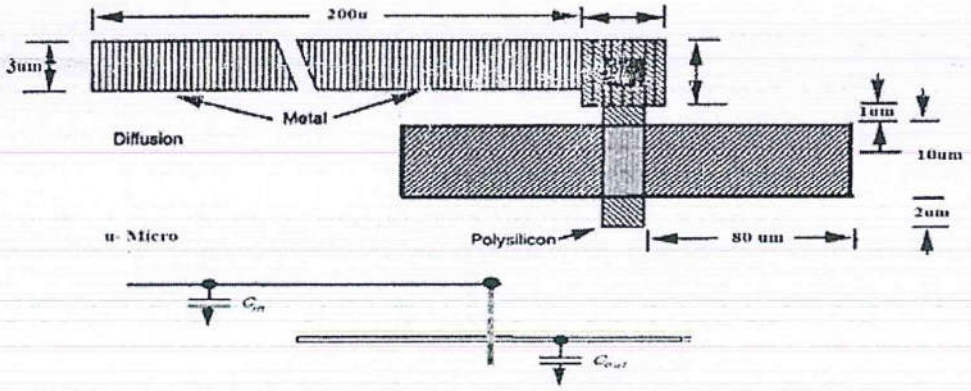
(Established under Karnataka Act No. 16 of 2013)

UE18EC254

DECEMBER 2020: END SEMESTER ASSESSMENT (ESA) B.TECH IV SEMESTER

UE18EC254 –DIGITAL VLSI DESIGN

Time: 3 Hrs | All Questions are Compulsary | Max Marks: 100

1.	a)	Explain the impact of different VLSI design styles upon the design cycle time and the achievable circuit performance.	6
	b)	Explain operation of a CMOS inverter with region of operation with a neat graph and specifying the condition	8
	c)	Derive the expression for critical voltages VIL of depletion load NMOS Inverter	6
2.	a)	Explain the Transistor Design Rules for NMOS,PMOS and CMOS with appropriate diagrams	6
	c)	Realize the Circuit and draw the stick diagram for the following Boolean expression Y= (a+b).c using NMOS & CMOS logic.	8
	d)	Realize the Boolean function $Z=\overline{(D+E+A)(B+C)}$ using CMOS logic and Using the Euler's graph find the Euler's path	6
3.	a)	Calculate the Absolute value of C_{in} and C_{out} for the given Multilayer Layout structure given using orbit 2 μm technologies 	7
	b)	Derive the expression for Number of stages Inverter to be cascaded to drive large capacitive load with minimum delay.	7
	c)	Derive the scaling factor in combined V and D scaling model for the following MOSFET device parameters. i. power-speed product(PT) ii. Maximum operating frequency(f0) iii. Current density(J)	6

Capacitance	*Value in pF × $10^{-4}/\mu m^2$ (Relative values in brackets)*					
	5 μm		*2 μm*		*1.2 μm*	
Gate to channel	4	(1.0)	8	(1.0)	16	(1.0)
Diffusion (active)	1	(0.25)	1.75	(0.22)	3.75	(0.23)
Polysilicon* to substrate	0.4	(0.1)	0.6	(0.075)	0.6	(0.038)
Metal 1 to substrate	0.3	(0.075)	0.33	(0.04)	0.33	(0.02)

Notes: Relative value = specified value/gate to channel value for that technology.

SRN

4.	a)	Explain how Full Adder is realized using TG	7
	b)	What is dynamic logic and what is the drawback of cascading dynamic logic? Explain how it is overcome by domino logic	7
	c)	Realize the following Boolean expression using a) Dynamic b) Pseudo c) C2MOS logic and also draw the stick diagram for C2MOS logic $Y = (ab+cd)'$	6
5.	a)	Explain the design strategy to be used for designing 6T SRAM using Read '0' and Write'0' operation.	8
	b)	Explain with suitable diagram the operation of three transistor DRAM cell.	6
	c)	Suppose one cycle of logic is particularly critical and the next cycle is nearly empty. Determine the maximum amount of time the first cycle can borrow into the second for each of the following sequencing styles. Assume there is zero clock skew and that the cycle time is 500 ps. Use the data given in the table Q5c. a) Flip-flops b) Two-phase transparent latches with 50% duty cycle clocks c) Two-phase transparent latches with 60 ps of nonoverlap between phases d) Pulsed latches with 80 ps pulse width	6

	Setup Time	*clk*-to-*Q* Delay	*D*-to-*Q* Delay	Contamination Delay	Hold Time
Flip-Flops	65 ps	50 ps	n/a	35 ps	30 ps
Latches	25 ps	50 ps	40 ps	35 ps	30 ps

Table Q5c