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**PES University, Bengaluru**
(Established under Karnataka Act No. 16 of 2013)

**UE18EC254**

**DECEMBER 2021: END SEMESTER ASSESSMENT (ESA), B.TECH**
**Digital VLSI Design**

| Time: 3 Hrs | Answer All Questions | Max Marks: 100 |
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|---|---|---|---|
| 1 | a) | Explain VLSI Design flow using design activities on three different domain using Y-Chart | 6 |
| | b) | Mention different regions for CMOS inverter circuit on its voltage-transfer characteristic curve and hence write the expressions for the voltages $V_{IL}, V_{OH}, V_{IH}$ and $V_{OL}$. | 8 |
| | c) | Consider a resistive-load inverter circuit with $V_{DD} = 5V, k_n' = 20\frac{\mu A}{V^2}$, $V_{T0} = 0.8\,V, R_L = 200k\Omega$ and $\frac{W}{L} = 2$. Calculate the critical voltages $(V_{OL}, V_{OH}, V_{IL}, V_{IH})$ on the VTC and find the noise margins of the circuit. | 6 |
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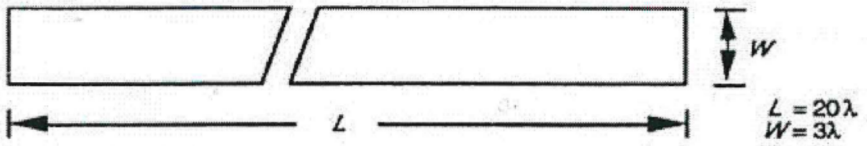
| 2 | a) | Explain with neat diagram, each step of nMOS transistor fabrication. | 10 |
| | b) | Mention the minimum width/size criterion for the following layers with reference to Lambda based design rules.<br>i. p-diffusion<br>ii. Polysilicon<br>iii. Metal1<br>iv. Transistor<br>v. Between two metal1 layers | 5 |
| | c) | Draw the stick diagram and layout diagram of CMOS inverter. | 5 |
| | | | |
| 3 | a) | Consider the area defined in the fig. below. Calculate the area relative to that of a standard gate and the capacitance value for a 5μm technology if the layer given is<br>i) Metal 1<br>ii) Polysilicon<br>iii) n-type diffusion<br>  | 6 |
| | b) | Calculate the inverter pair delay for<br>i. nMOS inverter<br>ii. CMOS inverter | 8 |
| | c) | Calculate the scaling factors for the following<br>i. Gate area<br>ii. Channel resistance<br>iii. Gate delay<br>iv. Gate capacitance | 6 |
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| 4 | a) | Draw the following circuits using CMOS Transmission gates.<br>i. Two-input multiplexor<br>ii. XOR function using 8 transmission gates | 10 |
| | b) | Explain the pre-charge and evaluation phases of domino logic. | 6 |
| | c) | Draw a four – bit adder subtractor circuit | 4 |
| | | | |
| 5 | a) | Explain the working of flip-flop and latch with the help of timing diagram | 8 |
| | b) | Define the following terms:<br>i. Contamination delay<br>ii. Propagation delay<br>iii. Set-up time<br>iv. Hold time | 4 |
| | c) | Explain the Read and Write operations of 3T DRAM cell. | 8 |

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