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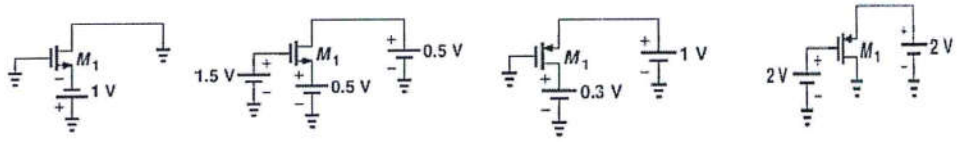
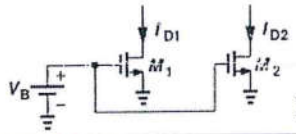
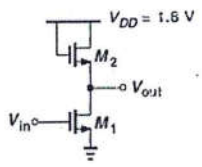
PES University, Bangalore
(Established under Karnataka Act No. 16 of 2013)

UE18EC203

DEC 2019: END SEMESTER ASSESSMENT (ESA) B.Tech III SEMESTER

UE18EC203: CMOS Analog Circuit Design

Time: 3 Hrs | Answer All Questions | Max Marks: 100

1.	a)	From the fundamental concepts of channel charge density, derive an expression for drain current (I_D) of NMOS transistor and also obtain the expression for $I_{D,MAX}$ and R_{ON} from the same.	08
	b)	Determine the region of operation of M_1 in each of the circuits shown in Fig. (1) . Assume V_{TH} = 0.4 V for NMOS and V_{TH} = - 0.4 V for PMOS  Fig(1).	04
	c)	Two current sources realized by identical MOSFETs Fig.(2) match to within 1%, i.e., $0.99\ I_{D2} < I_{D1} < 1.01 I_{D2}$. If V_{DS1} = 0.5 V and V_{DS2} = 1 V, what is the maximum tolerable value of λ? Assume $\mu_n C_{ox}$ = 200 $\mu A/V^2$, V_{TH} = 0.4 V  Fig(2)	04
	d)	An NMOS current source with I_D = 0.5mA must operate with drain – source voltage of 0.4V. If the output impedance is 20K ohms , determine the (W/L) ratio and gate voltage of the device. Assume $\mu_n .C_{ox}$ = 134μA/ V^2 , V_{th}= 0.7V	04
2.	a)	Design CS stage with resistive load to provide an output swing from 1V to 2.5V. Assume (W/L) = 50/0.5 , R_D = 2K ohms, λ= 0, V_{DD}= 3V, $\mu_n .C_{ox}$ = 134μA/ V^2 , V_{th}= 0.7V 1. Calculate the input voltages that yield desired output swing. 2. Calculate the drain current and the transconductance of the MOS device for both cases.	06
	b)	In the circuit shown below Fig.(3), $(W/L)_1$ = 10/0.18 and I_{D1} = 0.5 mA.(a) If λ = 0, determine $(W/L)_2$ such that M_1 operates at the edge of saturation.(b) Now calculate the voltage gain. (c) Explain why this choice of $(W/L)_2$ yields the maximum gain. Assume $\mu_n .C_{ox}$ = 200 $\mu A/V^2$, V_{TH}= 0.4 V  Fig.(3)	04

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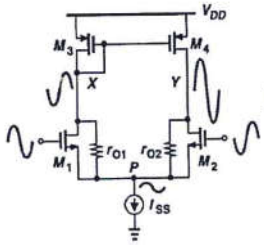
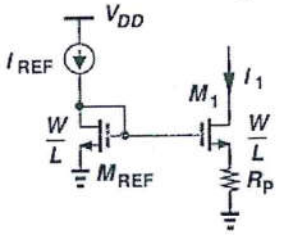
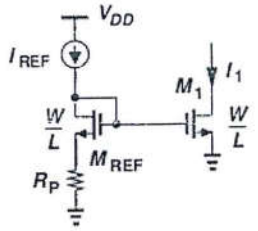
	c)	Show that in the case of CS stage with source degeneration, A_V equation becomes weaker function of g_m, and also drain current is "linearized" function of input voltage.	06
	d)	Derive an expression for voltage gain of a source follower with the aid of a small signal circuit taking body effect into account and $\lambda = 0$.	04
3.	a)	Obtain the relationship between I_{out} and I_{ref} in case of basic current mirror circuit .What is the effect of channel length modulation on output current I_{out} ? How can the effect of channel length modulation on output current can be suppressed? Redraw the modified current mirror circuit and explain how the effect of channel length modulation is minimized.	06
	b)	In the circuit shown below Fig.(4), does virtual ground exist at node 'P'? Explain the reason. Further, calculate G_M, R_{out} and small-signal voltage gain A_V of the circuit.  Fig.(4)	06
	c)	1.Determine the value of R_P in the circuit of Fig.(5) such that $I_1 = I_{REF}/2$.  Fig.(5)  Fig.(6) 2.Determine the value of R_P in the circuit of Fig.(6) such that $I_1 = 2I_{REF}$.	08
4.	a)	Why differential paths are important for sensitive and noisy signals? Also explain the effect of differential signal on output voltage swings.	06
	b)	Obtain the expression for common mode to differential mode conversion of an differential amplifier owing to device dimension and threshold voltage mismatch.	07
	c)	Design differential pair with PMOS Loads for a voltage gain of 20 and a power budget of 1 mW with $V_{DD} = 1.8$ V. Find g_{mN}, (W/L) ratio of both NMOS and PMOS devices. Assume ,input common-mode level is 1 V, $\mu_n.C_{ox} = 2\mu_p.C_{ox} = 100\ \mu A/V^2$, $V_{TH,n} = 0.5$ V, $V_{TH,p} = -0.4$ V, $\lambda_n = 0.5\lambda_p = 0.1\ V^{-1}$.	07

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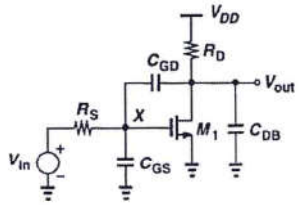
5.	a)	For the following circuit Fig.(7),find ω_{in} and ω_{out} using Miller's Theorem. Using these two poles obtain the transfer function of the circuit. Also explain what will be the error and possible concern in estimation of the transfer function with this approach.  Fig.(7)	06
	b)	With suitable examples explain the effect of negative feedback on Gain desensitization and Bandwidth modification.	06
	c)	Derive an expression for the transfer function of Voltage- Current feedback system and also obtain the expression for R_{out} and R_{in} with negative feedback.	08