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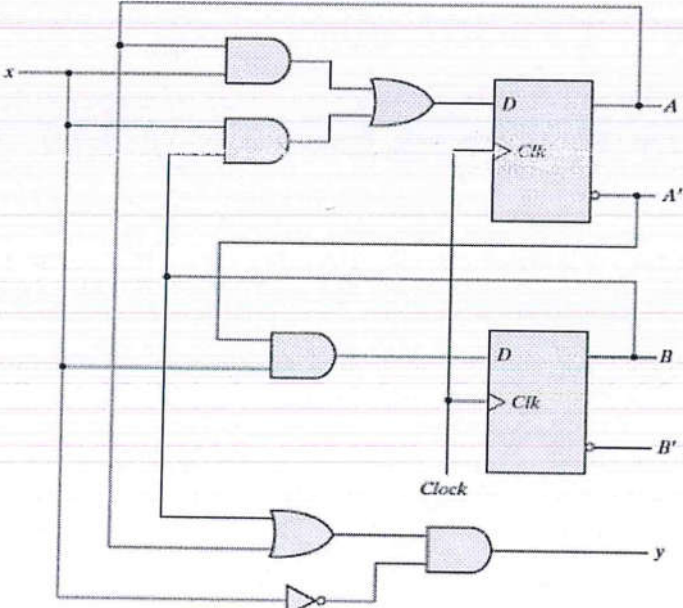
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PES University, Bengaluru
(Established under Karnataka Act No. 16 of 2013)

UE19EC205**DECEMBER 2020: END SEMESTER ASSESSMENT (ESA) B TECH 3rd SEMESTER****UE19EC205-Computer Organization and Digital Design**

Time: 3 Hrs	Answer All Questions	Max Marks: 100
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1	a)	Convert $(41.6875)_{10} = ()_2$.	3
	b)	Simplify the Boolean function, $F(w,x,y,z) = \sum(0,1,2,4,5,6,8,9,12,13,14)$ using four variable K-Map.	7
	c)	Explain 3-to-8-line Decoder with a neat diagram and Truth table. Construct 4X16 decoder with two 3X8 decoders.	10
2	a)	Write the steps involved in flip flop conversions. Convert D Flip-flop into JK Flip-flop.	7
	b)	Analyze the following given clocked sequential circuit and answer the questions given below.  <ol style="list-style-type: none">1. Identify the model of given sequential circuit2. Write the state equations for the next state3. Write the state table4. Draw the state diagram	8
	c)	Write a HDL model for 4-bit universal shift register using behavioral modeling	5

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3	a)	With the help of a neat diagram and relevant equations explain 4-bit Carry-Lookahead adder. Construct a 16-bit Carry-Lookahead adder using 4-bit adders.	10
	b)	Perform Bit pair recoding multiplication of (13) X (-6).	5
	c)	Subtract the floating point numbers, $F_2 = (100001110.11)_2$ from $F_1 = (11100000)_2$. Also represent the result in equivalent binary value with mantissa and exponent.	5
4	a)	Explain the following a. Byte addressability b. Big endian c. Little endian	6
	b)	Explain about a straight-line sequencing for $C = [A] + [B]$ with a neat diagram.	7
	c)	Differentiate between Von-Neumann and Harvard Architecture.	7
5	a)	Explain about connection of the memory to the processor and show how data transfer takes place between memory and a processor with a neat diagram.	8
	b)	Explain the direct mapped cache in mapping function with a neat diagram.	8
	c)	Give a brief note on Write-through protocol & Write-back protocol.	4