



**DECEMBER 2021: END SEMESTER ASSESSMENT (ESA) B. TECH
 3rd SEMESTER**

UE20EC205 - Computer Aided Digital Design

Time: 3 Hrs		Answer All Questions	Max Marks: 100																																																																																					
1	a)	With neat diagram explain the different levels of abstraction for an electronic computer system along with typical building blocks at each level.	8																																																																																					
	b)	Compare the range of N-bit numbers in unsigned, sign/magnitude and two's complement binary number systems. Also write a number line indicating the values of 4-bit numbers in each of these binary number systems.	8																																																																																					
	c)	Simplify the following Boolean equation. Sketch a reasonably simple combinational circuit implementing the simplified equation. $Y = \overline{A + \overline{AB} + \overline{A}\overline{B}} + \overline{A + \overline{B}}$	4																																																																																					
2	a)	Using De Morgan equivalent gates and bubble pushing methods redraw the circuit shown in the following Figure so that you can find the Boolean equation by inspection. Write the Boolean equation.	6																																																																																					
	b)	Find a minimal Boolean equation using K-map for the function given in the following truth table. Remember to take advantage of the don't care entries. Also sketch a circuit for the simplified function.	8																																																																																					
		<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>C</th> <th>D</th> <th>Y</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>X</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>X</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>X</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>X</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>X</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>X</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	C	D	Y	0	0	0	0	0	0	0	0	1	1	0	0	1	0	X	0	0	1	1	X	0	1	0	0	0	0	1	0	1	X	0	1	1	0	X	0	1	1	1	X	1	0	0	0	1	1	0	0	1	0	1	0	1	0	0	1	0	1	1	1	1	1	0	0	0	1	1	0	1	1	1	1	1	0	X	1	1	1	1	1	
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	c)	Write system verilog code for the following function using data flow modeling style. Here assume that inverters have a delay of 2 ns, three-input AND gates have a delay of 4 ns, and three-input OR gates have a delay of 6 ns. $Y = \bar{a}bc + a\bar{b}c + ab\bar{c}$	6
3	a)	With neat block diagram explain the working of D flip-flop. Also write the logic symbol for D flip-flop.	6
	b)	Write the waveform and state transition diagram for a divide-by-3 counter. With the help of this state transition diagram design the FSM using one-hot encoding.	9
	c)	Assume that you have designed the circuit shown in the following Figure. According to the data sheets for the components, flip-flops have a clock-to-Q contamination delay of 30 ps and a propagation delay of 80 ps. They have a setup time of 50 ps and a hold time of 60 ps. Each logic gate has a propagation delay of 40 ps and a contamination delay of 25 ps. Determine the maximum clock frequency and check whether any hold time violations could occur. If so, provide the solution to overcome hold time violations.	5
4	a)	Write system verilog programs for a 3:8 decoder using case statements and parameterized module separately. Among these two methods which one is preferred? Justify your statement.	8
	b)	Write state transition diagram and system verilog code using Mealy module to implement the following problem statement. Use binary encoding. Alyssa P. Hacker owns a pet robotic snail with an FSM brain. The snail crawls from left to right along a paper tape containing a sequence of 1's and 0's. On each clock cycle, the snail crawls to the next bit. The snail smiles when the last two bits that it has crawled over are 01. The input A is the bit underneath the snail's antennae. The output Y is TRUE when the snail smiles.	6
	c)	Write a self-checking testbench for the following function: Insert a delay of 20 time units for each input combination. $y = \bar{a}\bar{b}\bar{c} + a\bar{b}\bar{c} + ab\bar{c}.$	6
5	a)	Mention the steps for adding floating-point numbers with the same sign. With the help of these steps find the floating-point addition of 7.875 and 0.1875 using IEEE 754 single precision floating-point format.	8
	b)	With neat diagram explain the working of a 4-bit shift register with parallel load also explain how it can be used as a parallel to serial converter. Write system verilog code to implement this register.	8
	c)	Write neat diagram for the internal organization of 4X3 memory array.	4