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PES University, Bengaluru

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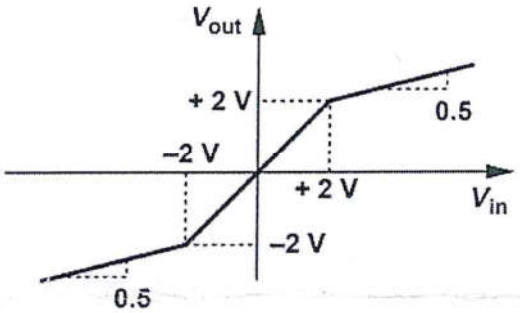
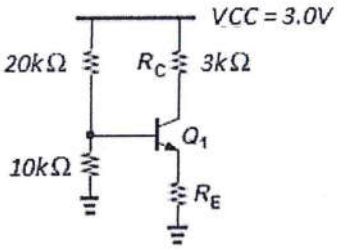
UE19EC204

December 2020: END SEMESTER ASSESSMENT B Tech III SEMESTER

UE19EC204 - ANALOG CIRCUIT DESIGN

Time: 3 Hrs	Answer All Questions	Max Marks: 100

1.	a)	With neat circuit diagram obtain an expression to avoid saturation region operation of transistor in simple biasing technique. Further, also specify any one limitation of this technique.	4
	b)	We wish to design a circuit that exhibits the input/output characteristic shown in Figure 1. Using 1kΩ resistors, ideal diodes, and other components, construct the circuit.  Figure 1	5
	c)	With relevant waveforms, explain emitter follower circuit as a power amplifier.	5
	d)	In the circuit of Figure 2, determine the required value of R_E Assume collector current equal to 0.5mA, $\beta = 100$ and $I_S = 5*10^{-15}$ A.  Figure 2	6
2.	a)	Write a short note on CMOS technology	4
	b)	From the fundamentals of channel charge density derive an expression for drain current in the MOSFET	6
	c)	Write importance differences between NMOS and PMOS transistors	4
	d)	A MOSFET is biased at a drain current of 0.5 mA. If $\mu_n C_{ox} = 100\ \mu A/V^2$, $W/L = 10$, and $\lambda = 0.1V^{-1}$, $\eta = 0.1$, calculate its small-signal parameters.	6

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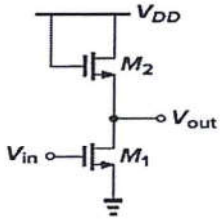
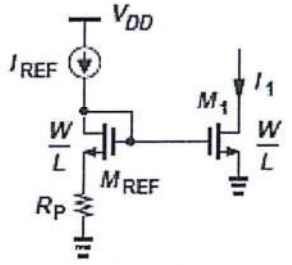
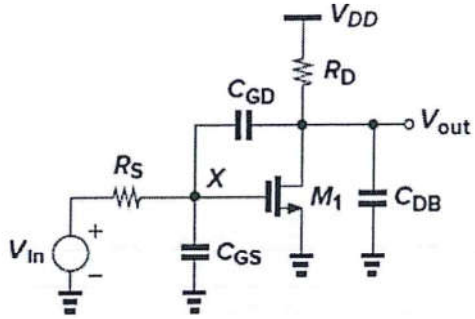
3.	a)	Derive expression for voltage gain in a source follower circuit.	7
	b)	Explain Cascode amplifier and its voltage head room issue.	6
	c)	Consider the circuit shown in Figure 3 with $(W/L)_1 = 50/0.5$ and $(W/L)_2 = 10/0.5$. Assume $V_{DD} = 3.0V$, $V_{TH} = 0.7V$ and $\lambda = \gamma = 0$. At what input voltage M_1 is at the edge of saturation region? What is the small signal gain under this condition?  Figure 3	7
4.	a)	Derive expression for the small signal voltage gain of MOS Differential pair using half circuit analysis.	7
	b)	Write a note on Differential pair with MOS loads.	6
	c)	Write the expression for the resistor R_P in the circuit of Figure 4 such that $I_1 = 2I_{REF}$. If $V_{GS2} = 1.5V$, $V_{th} = 0.5V$ and $I_{REF} = 1.2mA$, what is the value of required R_P to meet the condition?  Figure 4	7
5.	a)	Discuss different types amplifiers with their idealized models.	5
	b)	Explain the non-linearity reduction feature of the feedback amplifier.	5
	c)	Derive the expression for input impedance and output impedance of voltage-voltage feedback topology.	5
	d)	The CS stage of Figure 5 is designed with $(W/L)_1 = 50/0.5$, $R_S = 1k\Omega$, and $R_D = 2k\Omega$. If $I_{D1} = 1$ mA, determine the poles of the circuit. Assume $C_{gs} = 75fF$, $C_{gd} = 0.2fF$, $C_{db} = 27fF$ and $\mu_n C_{ox} = 135\mu A/V^2$.  Figure 5	5