PES UNIVERSITY

PES University, Bengaluru

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UE18EC204

DECEMBER 2020: END SEMESTER ASSESSMENT (ESA) B TECH

UE18EC204 – Digital Design Using HDL

Time: 3 Hrs	Answer All Questions	Max Marks: 100

1	a)	Find all the prime implicants of the following function using K-map: $f(a,b,c,d)=\sum m(0,2,4,5,6,7,8,10,13,15)$	5
	b)	Simplify the logic function given below, using Quine-McCluskey method and get the minimal SOP expression: $f(a,b,c,d)=\sum m(0,1,3,7,8,9,11,15)$	8
	c)	Explain the HDL design flow with a diagram	7
2	a)	Consider the values A = 0101 and B = 1010, Perform the 4-bit addition operation using 4-bit adder - subtractor circuit with XOR gate. Explain with a neat diagram.	5
	b)	Explain Implementation of a full adder with a Decoder with a neat diagram	5
	c)	List and explain the three different modellings in HDL with an example code	10
3	a)	What is the significance of edge triggering? Explain the working of D-type positive edge triggered Flip-flop with a neat circuit diagram.	6
	b)	Write a HDL model for 2 to 1 multiplexer using dataflow modelling	4
	c)	Convert JK Flip-flop into D Flip-flop.	5
	d)	Write a HDL model for JK Flip-Flop using case statement.	5
4	a)	With the help of a neat diagram, explain the four bit register with parallel load.	5
	b)	Design a 4-bit Universal shift register using positive edge triggered D Flip-flops and explain its operation.	7
	c)	Write a HDL model in structural description for a ripple counter with D Flip-Flop as its component.	8

5	a)	A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is 000011101010	5
	b)	Implement the following two Boolean functions with a PLA: $F_1(A, B, C) = \sum(0, 1, 2, 4)$ $F_2(A, B, C) = \sum(0, 5, 6, 7)$	10
	c)	List and explain the types of ROMs	5