SRN | | | | | | | | | | | |

PES University, Bangalore

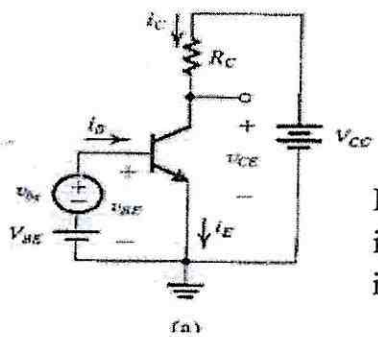
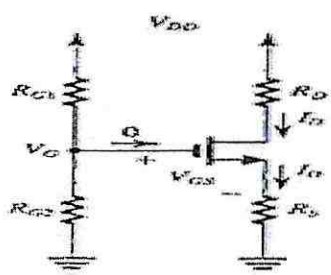
(Established under Karnataka Act No. 16 of 2013)

DEC 2018: END SEMESTER ASSESSMENT (ESA) B.TECH. III SEMESTER

UE17EC202- ANALOG CIRCUIT DESIGN

Time: 3 Hrs | Answer All Questions | Max Marks: 100

Note :- Write the equations while solving mathematical problems

1.	a)	Design the DC biasing and resistor value of a clamper circuit to shift the output waveform 5V above the input waveform. Input signal is 7V peak 1000 Hz sinusoidal. Discharge time constant is around five times of one cycle time. Capacitor value is 0.47uF. Draw the circuit diagram, input and output waveforms with values. Assume Silicon diode.	7M
	b)	Briefly explain "reverse recovery time" in diode with its significance.	3M
	c)	 For the given circuit, derive the expressions for i) small signal collector current i_c ii) small signal voltage gain Av	5M
	d)	Classify the amplifiers based on the type of input and output signals. Write the ideal input and output resistance for each. Draw the small signal ac equivalent model for amplifier in which input signal is voltage and output signal is current .	5M
2	a)	Draw the cross section view of enhancement type N channel MOSFET for $V_{GS}>Vt$ and $(V_{GS}-Vt)>V_{DS} >> 0$. Briefly explain the operation of MOSFET with the drain current equation for the above condition.	5M
	b)	With R_{G1} =1MΩ, design all the remaining resistor values of the given MOSFET amplifier to operate DC drain current of 0.5 mA in saturating region. Also find the value of V_{GS}. DC drain voltage V_D =4V , Source voltage Vs =2V, DC Power supply voltage V_{DD}=10V, The MOSFET device has i) threshold voltage Vt=1V ii) k'_nW/L =1mA/V^2 Neglect channel length modulation effect. 	5M
	c)	With regard to the MOSFET, define process transconductance parameter and aspect ratio. Consider an n-channel MOSFET with t_{ox} =20nm μ_n =650 cm^2/V, Vt=1V , W/L =10 permittivity of Silicon oxide ϵ_{ox} = 3.45x 10^{-11}F/m. Find the drain current when V_{GS} =3V and V_{DS} =2.5V	5M

PTO

SRN | | | | | | | | | | |

	d)	Calculate the input resistance, output resistance and overall voltage gain Gv of common source amplifier if g_m = 2 mA/V, r_o = 50kΩ , R_D =10kΩ R_L =20kΩ , R_G = 10MΩ, Rsig= 500kΩ . Draw the small signal ac equivalent circuit for this amplifier with values.	5M
3	a)	An CS amplifier has R_G =4.7MΩ, R_D=R_L = 20kΩ, Rsig= 100 kΩ Coupling capacitors C_{C1}=C_{C2} = 1uF, bypass capacitor Cs =2uF MOSFET has internal capacitances Cgs=1.5pF Cgd =0.5pF, output resistance ro = 150kΩ, If midband gain with load A_M is -18, g_m =1.92mA/V, Calculate i)lower cutoff frequencies due to coupling capacitors and bypass capacitor & lower 3-dB frequency f_L of amplifier iii)upper 3-dB frequency f_H iii) the frequency at which the short circuit current gain is unity.	10M
	b)	Draw the collector current waveforms for transistors operating in class A and class C amplifiers. Derive the maximum power conversion efficiency for class A amplifier.	5M
	c)	A class B output stage is required to deliver an average power of 50W into a 8 Ω load. The power supply should be 4 V greater than the corresponding peak sine-wave output voltage. Determine the power-supply voltages required (PS+ and PS-), the peak current from each supply, the total supply power, the power-conversion efficiency and max power dissipated.	5M
4	a)	Briefly explain the negative feedback with block/signal flow diagram and derive the gain equation with feedback. List the properties of negative feedback amplifier.	5M
	b)	Draw the block diagram of negative feedback amplifier where input is current and output is voltage. Name the type of feedback topology. Derive the equation for input resistance and output resistance with feedback.	5M
	c)	Define Barkhausen criteria for oscillator. If negative feedback resistor of Wien bridge oscillator is 33kΩ, design all other resistor values to get 700 Hz output frequency. Consider C=0.01uF. Draw the circuit diagram with values.	5M
	d)	With diagrams, briefly explain how to ensure the stability of the amplifier using i) Bode plots ii) Nyquist plot.	5M
5.	a)	With a neat diagram, briefly explain the operation of instrumentation amplifier circuit using op-amps. Write the gain equation of the amplifier for differential input.	5M
	b)	For inverting amplifier using op amp, derive the corner frequency (3-dB frequency) in terms of unity gain frequency(w_t) using closed loop gain and open loop gain equations . Draw the frequency response for the same.	5M
	c)	With respect to opamp , define i) input bias current ii) input offset current iii)slew rate iv) full power bandwidth v)input offset voltage.	5M
	d)	Draw the circuit diagram of astable multivibrator using op-amp. Derive the equations for time duration of output high (T_{HIGH}) and frequency of output.	5M

********** **********

SRN

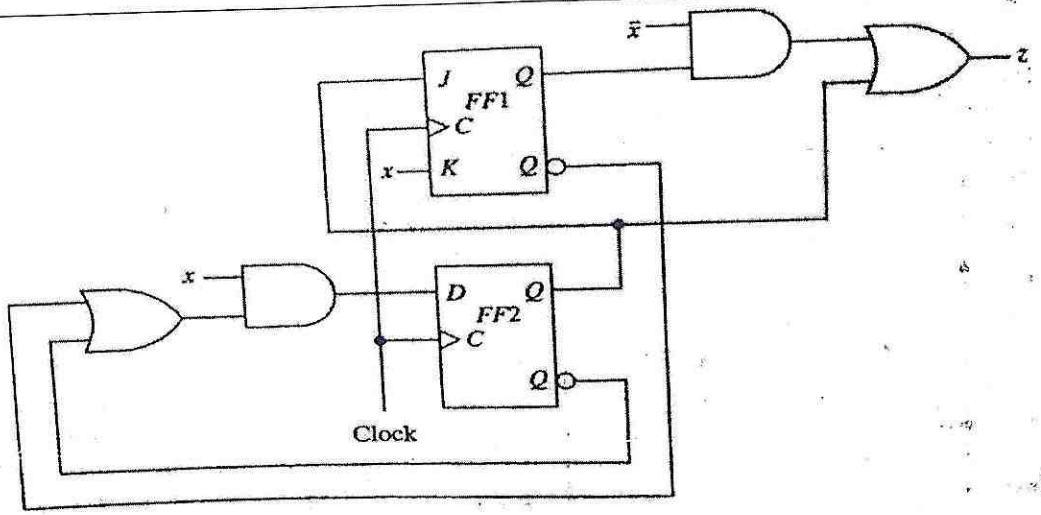


fig. Q4(a)

5	a)	Write the terminal voltage conditions for different regions of operation of the NMOSFET enhancement mode device, draw the circuit diagram of CMOS inverter, and define Noise margins w.r.t. digital logic circuit.	6
	b)	Draw the circuit diagram of 3-input CMOS NAND gate.	3
	c)	Design a Multiplier that can multiply 4-bit multiplicand and 3-bit multiplier using 4-bit binary adder component and additional logic gates.	7
	d)	Obtain a minimal state FSM for a clocked synchronous sequential network having a single input line x, in which the symbols 0 and 1 are applied, and a single output line z. An output of 1 is to be produced for each consecutive 1 input if the group of consecutive 1 inputs is preceded by exactly one 0 input. At all other times the network is to produce 0 outputs. An example of input/output sequences that satisfy the conditions of the network specification is: x = 1 1 0 1 1 0 0 0 1 1 1 1 0 1 0 1 1 1 z = 0 0 0 1 1 0 0 0 0 0 0 0 0 1 0 1 1 1	4