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PES UNIVERSITY

PES University, Bangalore

(Established under Karnataka Act No. 16 of 2013)

UE18EC204

DEC 2019: END SEMESTER ASSESSMENT- B.TECH. III SEMESTER

UE18EC204 – DIGITAL DESIGN USING HDL (DDHDL)

Time: 180 mins | Answer All Questions | Max Marks: 100

1.	a)	The following Boolean expression: $F = \bar{a}b + ad + a\bar{b}c$ OR $F = \bar{a}b + \bar{c}d + a\bar{b}c$ Is a simplified version of the expression: $F = \bar{a}bc\bar{d} + \bar{a}bcd + a\bar{b}\bar{c}d + a\bar{b}cd + ab\bar{c}d$ Are there any don't care terms? If so, which are they?	05
	b)	Find all the prime implicants and the minimal SOP expression for the following function using Quine-McCluskey Binary method. $F(v,w,x,y,z) = \sum m(1,9,10,11) + d(0,3,14,25,27)$	10
	c)	Draw the logic diagram of the digital circuit specified by the following Verilog description: module circuit1(A,B,C,D,F); input A,B,C,D; output F; wire u,v,w,x,y,z; or (x,B,C,u); and (y,v,C); and (w,B,z); and (z,y,A); or (F,x,w); not (u,D); not (v,A); endmodule	05
2.	a)	An 8:1 Multiplexer has inputs a, b and c connected to the select lines s_2, s_1 and s_0 respectively. The data inputs I_0 to I_7 are as follows: $I_1 = I_2 = 0;\ I_3 = I_5 = I_7 = 1;\ I_0 = I_4 = d$ and $I_6 = \bar{d}$ Determine the Boolean function that the Multiplexer implements.	05

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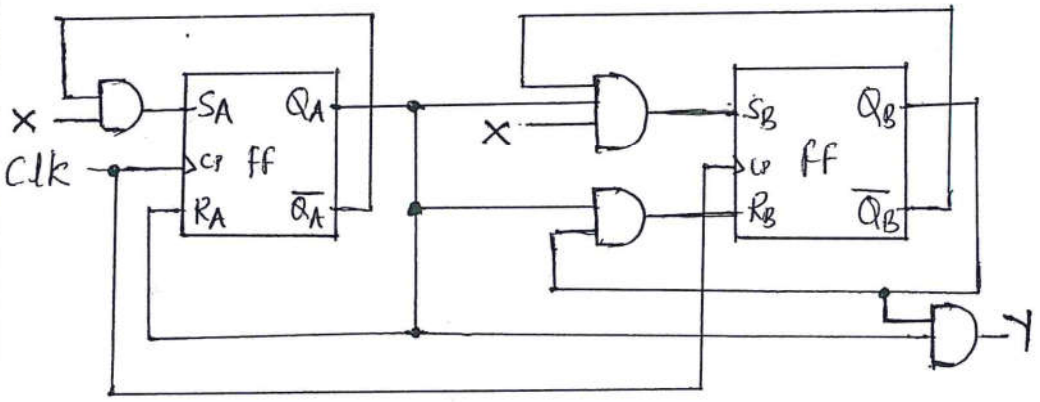
	b)	Using the Decoder with active low outputs, design the combinational circuit defined by the following functions: $f_1(x,y,z) = \bar{x}\bar{y}\bar{z} + xz + yz$ $f_2(x,y,z) = x\bar{y}\bar{z} + \bar{x}y$ $f_3(x,y,z) = \bar{x}\bar{y}z + xy$	05
	c)	Design a 4-bit BCD Adder circuit using 7483 IC chip, with self correcting circuit, that is, a provision has to be made in the circuit, in case if the sum of the BCD numbers exceeds 9.	05
	d)	Construct a 2:1 Multiplexer with three state buffers and write a Verilog HDL code for the same using three state gates.	05
3.	a)	Write the characteristic table of a JK Flip-flop and derive the characteristic equation for its complement output.	04
	b)	Give the output function, state table and state diagram by analyzing the sequential circuit shown in the figure below: 	10

	c)	i) Draw the logic diagram for the sequential circuit described by the following HDL module:
		`module seq_ckt(input A,B,C, output reg Q,input clk);`
		`reg E;`
		`always @ (posedge clk)`
		`begin`
		`E<=A||B;`
		`Q<=E&&C;`
		`end`
		`endmodule`
			06

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		ii) Draw the logic diagram for the same HDL module to have the same behavior when the assignments are made with = instead of with <=	
4.	a)	Draw the logic diagram of a 4-bit bidirectional Universal shift register with four D flip-flops and four 4:1 Multiplexers with mode selection inputs s_1 *and* s_0. Also write the verilog HDL code for the same using Behavioral modeling.	**10**
	b)	Design a Synchronous counter using positive edge triggered JK flip-flops whose counting sequence : $Q_2Q_1Q_0$ is : 000, 001, 100, 110, 111, 101, 000, ...	**10**
5.	a)	It is necessary to formulate the Hamming code for four data bits D_3, D_5, D_6 *and* D_7 together with three parity bits P_1, P_2 *and* P_4. i) Evaluate the 7-bit composite code word for the data word 0010. ii) Evaluate three check bits C_4, C_2 *and* C_1 iii) Assume an error in bit D_5 during writing into memory. Show how the error in the bit is detected and corrected. iv) Add parity bit P_8 to include double-error detection in the code. Determine the Hamming code word for double-error detection.	**06**
	b)	Which are the three fundamental types of standard PLDs. How do you differentiate them?	**04**
	c)	Realize the following given functions with a 3x4x2 PLA device, with both true and complemented outputs. $f_1(x,y,z) = \sum m(1,2,3,7)$ $f_2(x,y,z) = \sum m(0,1,2,6)$	**10**