Section 20. Comparator Voltage Reference

HIGHLIGHTS

This section of the manual contains the following major topics:

Note: This family reference manual section is meant to serve as a complement to device data sheets. Depending on the device variant, this manual section may not apply to all PIC32MX devices.

Please consult the note at the beginning of the **"Comparator Voltage Reference"** chapter in the current device data sheet to check whether this document supports the device you are using.

Device data sheets and family reference manual sections are available for download from the Microchip Worldwide Web site at: http://www.microchip.com

20.1 INTRODUCTION

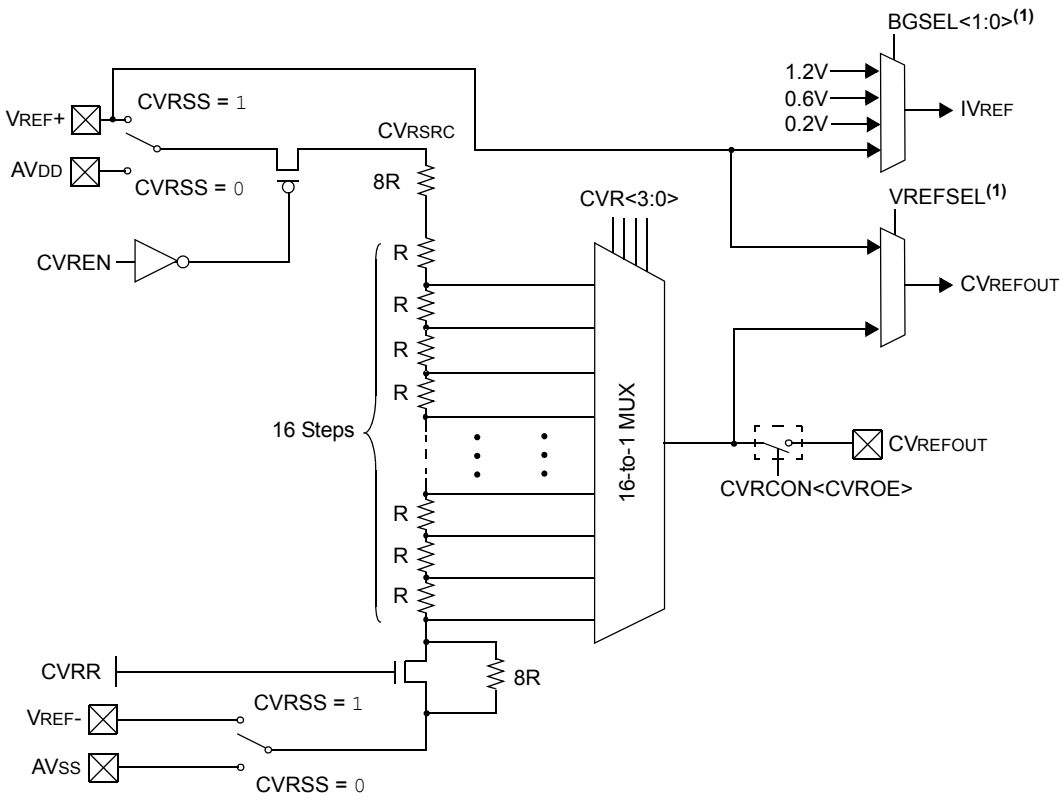
The Comparator Voltage Reference module is a 16-tap, resistor ladder network that provides a selectable reference voltage. Although its primary purpose is to provide a reference for the analog comparators, it also may be used independently of them.

A block diagram of the module is illustrated in Figure 20-1. The resistor ladder is segmented to provide two ranges of voltage reference values and has a power-down function to conserve power when the reference is not used. The module's supply reference can be provided from either device VDD/VSS or an external voltage reference. The module output is available for the comparators and typically available for pin output. For more information, refer to the specific device data sheet.

The Comparator Voltage Reference has the following features:

- High and low range selection
- Sixteen output levels available for each range
- Internally connected to comparators to conserve device pins
- Output can be connected to a pin

Figure 20-1: Comparator Voltage Reference Block Diagram



Note 1: These bits are not available on all devices. On such devices, CVREF is generated by the resistor network and IVREF is connected to 1.2V. Refer to the specific device data sheet for availability.

20.2 COMPARATOR VOLTAGE REFERENCE CONTROL REGISTERS

The Comparator Voltage Reference module consists of the following Special Function Registers (SFR):

CVRCON: Comparator Voltage Reference Control Register

The following table provides a brief summary of the register related to the Comparator Voltage Reference module. The corresponding register appears after the summary, followed by a detailed bit description.

Table 20-1: Comparator Voltage Reference SFR Summary

Name	Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
CVRCON(1,2,3)	31:24	—	—	—	—	—	—	—	—
	23:16	—	—	—	—	—	—	—	—
	15:8	ON	—	—	—	—	VREFSEL(4)	BGSEL<1:0>(4)	
	7:0	—	CVROE	CVRR	CVRSS	CVR<3:0>			

Note 1: This register has an associated Clear register at an offset of 0x4 bytes. These registers have the same name with CLR appended to the end of the register name (e.g., CVRCONCLR). Writing a '1' to any bit position in the Clear register will clear valid bits in the associated register. Reads from the Clear register should be ignored.

2: This register has an associated Set register at an offset of 0x8 bytes. These registers have the same name with SET appended to the end of the register name (e.g., CVRCONSET). Writing a '1' to any bit position in the Set register will set valid bits in the associated register. Reads from the Set register should be ignored.

3: This register has an associated Invert register at an offset of 0xC bytes. These registers have the same name with INV appended to the end of the register name (e.g., CVRCONINV). Writing a '1' to any bit position in the Invert register will invert valid bits in the associated register. Reads from the Invert register should be ignored.

4: These bits are not available on all devices. Refer to the specific device data sheet for availability.

Register 20-1: CVRCON: Comparator Voltage Reference Control Register

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 23							bit 16

R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-1(1)
ON	—	—	—	—	VREFSEL(1)	BGSEL<1:0>(1)	
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CVROE	CVRR	CVRSS	CVR<3:0>			
bit 7							bit 0

Legend:			
R = readable bit	W = writable bit	P = programmable	r = reserved bit
U = unimplemented bit, read as '0'		-n = bit value at POR: ('0', '1', x = unknown)	

bit 31-16 **Reserved:** Write '0'; ignore read

bit 15 **ON:** Comparator Voltage Reference On bit

1 = Module is enabled, setting this bit does not affect other bits in the register.
0 = Module is disabled and does not consume current. Clearing this bit does not affect the other bits in the register.

Note: When using 1:1 PBCLK divisor, the user's software should not read/write the peripheral's SFRs in the SYSCLK cycle immediately following the instruction that clears the module's ON bit.

bit 14-11 **Reserved:** Write '0'; ignore read

bit 10 **VREFSEL:** Voltage Reference Select bit(1)

1 = CVREF = VREF+
0 = CVREF is generated by the resistor network

bit 9-8 **BGSEL<1:0>:** Band Gap Reference Source bits(1)

11 = IVREF = VREF+
10 = IVREF = 0.2V (nominal)
01 = IVREF = 0.6V (nominal, default)
00 = IVREF = 1.2V (nominal)

bit 7 **Reserved:** Write '0'; ignore read

bit 6 **CVROE:** CVREFOUT Enable bit

1 = Voltage level is output on CVREFOUT pin
0 = Voltage level is disconnected from CVREFOUT pin

bit 5 **CVRR:** CVREF Range Selection bit

1 = 0 to 0.67 CVRSRC, with CVRSRC/24 step size
0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size

Note 1: These bits are not available on all devices and the reset value is '0' for devices without these bits. Refer to the specific device data sheet for availability.

Register 20-1: CVRCON: Comparator Voltage Reference Control Register (Continued)

bit 4 **CVRSS:** CV_{REF} Source Selection bit
1 = Comparator voltage reference source, $CV_{RSRC} = (V_{REF}+) – (V_{REF}-)$
0 = Comparator voltage reference source, $CV_{RSRC} = AV_{DD} – AV_{SS}$

bit 3-0 **CVR<3:0>:** CV_{REF} Value Selection $0 \leq CVR<3:0> \leq 15$ bits
When CVRR = 1:
$CV_{REF} = (CVR<3:0>/24) \bullet (CV_{RSRC})$
When CVRR = 0:
$CV_{REF} = 1/4 \bullet (CV_{RSRC}) + (CVR<3:0>/32) \bullet (CV_{RSRC})$

Note 1: These bits are not available on all devices and the reset value is '0' for devices without these bits. Refer to the specific device data sheet for availability.

20.3 OPERATION

20.3.1 CVREF Output

The Comparator Voltage Reference module is controlled through the CVRCON register (Register 20-1). This module provides two ranges of output voltage, each with 16 distinct levels. The range to be used is selected by the CVRR bit (CVRCON<5>). The primary difference between the ranges is the size of the steps selected by the CVREF value selection bits, CVR<3:0>, with one range offering finer resolution and the other offering a wider range of output voltage. The typical output voltages are listed in Table 20-2.

The equations used to calculate the CVREF output are as follows:

If CVRR = 1:
Voltage Reference = ((CVR<3:0>)/24) x (CVRSRC)

If CVRR = 0:
Voltage Reference = (CVRSRC/4) + ((CVR<3:0>)/32) x (CVRSRC)

The CVREF Source Voltage (CVRSRC) can come from either VDD and VSS, or the external VREF+ and VREF- pins that are multiplexed with I/O pins. The voltage source is selected by the CVRSS bit (CVRCON<4>). The voltage reference is output to the CVREFOUT pin by setting the CVROE bit (CVRCON<6>); this overrides the corresponding TRIS bit setting.

The settling time of the Comparator Voltage Reference module must be considered when changing the CVREF output. For more information, refer to the specific device data sheet.

Table 20-2: Typical Voltage Reference in Volts (CVRSRC = 3.3)

CVR<3:0>	Voltage Reference	
	CVRR = 0 (CVRCON<5>)	CVRR = 1 (CVRCON<5>)
0	0.83V	0.00V
1	0.93V	0.14V
2	1.03V	0.28V
3	1.13V	0.41V
4	1.24V	0.55V
5	1.34V	0.69V
6	1.44V	0.83V
7	1.55V	0.96V
8	1.65V	1.10V
9	1.75V	1.24V
10	1.86V	1.38V
11	1.96V	1.51V
12	2.06V	1.65V
13	2.17V	1.79V
14	2.27V	1.93V
15	2.37V	2.06V

20.3.2 CVREF Output Considerations

The full range of voltage reference cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 20-1) keep the voltage reference from approaching the reference source rails. The voltage reference is derived from the reference source. Therefore, the voltage reference output changes with fluctuations in that source. Refer to the product data sheet for the electrical specifications. Table 20-3 contains the typical output impedances for the Comparator Voltage Reference module.

Table 20-3: Typical CVREF Output Impedance in kilohms

CVR<3:0>	Voltage Reference	
	CVRR = 0 (CVRCON<5>)	CVRR = 1 (CVRCON<5>)
0	12k	0.5k
1	13k	1.9k
2	13.8k	3.7k
3	14.4k	5.3k
4	15k	6.7k
5	15.4k	7.9k
6	15.8k	9k
7	15.9k	9.9k
8	16k	10.7k
9	15.9k	11.3k
10	15.8k	11.7k
11	15.4k	11.9k
12	15k	12k
13	14.4k	11.9k
14	13.8k	11.7k
15	12.9k	11.3k

20.3.3 IVREF Output

The Comparator Voltage Reference module provides selection for the internal voltage reference. The Band Gap Reference Source Select bits (BGSEL<1:0>) allow voltage selection of 1.2V, 0.6V, or 0.2V, which is generated internally. Refer to the specific device data sheet for the IVREF specifications.

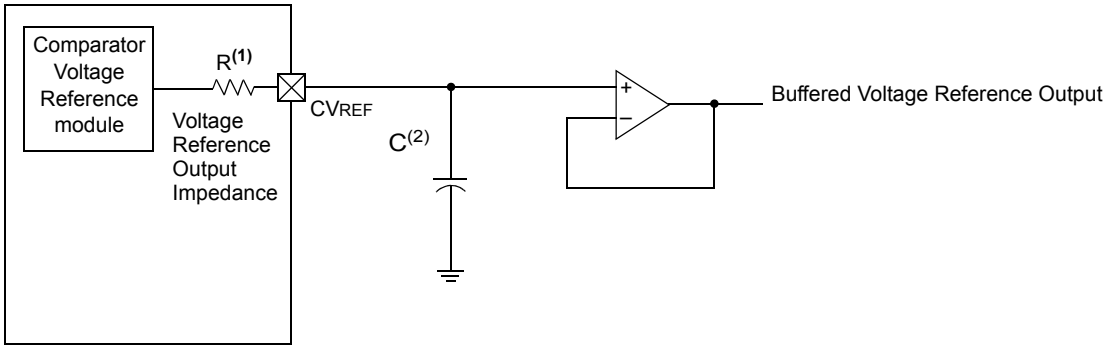
20.4 INTERRUPTS

There are no Interrupt configuration registers or bits for the Comparator Voltage Reference module. The module does not generate interrupts.

20.5 I/O PIN CONTROL

The Comparator Voltage Reference module can output to a pin. When the module is enabled and CVROE (CVRCON<6>) is '1', the output driver for the CVREFOUT pin is disabled and the CVREF voltage is available at the pin. For operation, the TRIS bit corresponding to the CVREFOUT pin must be a '1'. This disables the digital Input mode for the pin and prevents undesired current draw resulting from applying an analog voltage to a digital input pin. The output buffer has very limited drive capability. An external buffer amplifier is recommended for any application that uses the CVREF voltage externally. An output capacitor may be used to reduce output noise. Use of an output capacitor will increase settling time (see Figure 20-2).

Figure 20-2: Comparator Voltage Reference Output Buffer Example



Note 1: R is dependent on the Comparator Voltage Reference Control bits CVRR (CVRCON<5>) and CVR<3:0> (CVRCON<3:0>). For more information, see Table 20-3.

2: Use of an output capacitor will increase settling time. Capacitor value selection is dependent on the CVR<3:0> and CVRR settings, and the frequency to be attenuated.

20.6 OPERATION IN POWER-SAVING AND DEBUG MODES

20.6.1 Operation in Sleep Mode

The Comparator Voltage Reference module continues to operate in Sleep mode. The CVRCON register is not affected when the device enters or wakes from Sleep mode. If the CVREF voltage is not used in Sleep mode, the module can be disabled by clearing the ON bit (CVRCON<15>) prior to entering Sleep mode to save power.

20.6.2 Operation in Idle Mode

The Comparator Voltage Reference module continues to operate in Idle mode. The CVRCON register is not affected when the device enters or exits Idle mode. There is no provision to automatically disable the module in Idle mode. If the CVREF voltage is not used in Idle mode, the module can be disabled by clearing the ON bit (CVRCON<15>) prior to entering Idle mode to save power.

20.6.3 Operation in Debug Mode

The Comparator Voltage Reference module continues to operate while the device is in Debug mode. The module doesn't support Freeze mode.

20.7 EFFECTS OF RESETS

All Resets disable the voltage reference by forcing all bits in the CVRCON register to '0'.

20.8 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC32MX family device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Comparator Voltage Reference module are:

Title	Application Note #
Related application notes are not available.	N/A

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC32MX family of devices.

20.9 REVISION HISTORY

Revision A (October 2007)

This is the initial released version of this document.

Revision B (October 2007)

Updated document to remove Confidential status.

Revision C (April 2008)

Revised status to Preliminary; Revised U-0 to r-x.

Revision D (June 2008)

Revised Figure 20-1; Change Reserved bits from “Maintain as” to “Write”; Added Note to ON bit (CVRCON Register).

Revision E (August 2010)

This revision includes the following updates:

- Updated the Comparator Voltage Reference Block Diagram (see Figure 20-1)
- Added notes regarding the INV, SET, and CLR registers to the Oscillators SFR Summary (see Table 20-1)
- Updated the Comparator Voltage Reference Control Register (see Register 20-1)
- Removed the CVRCONINV, CVRCONSET, and CVRCONCLR registers
- Removed 20.3.3 “Initialization”
- Added new section **20.3.3 “IVREF Output”**
- Removed Table 20-4: Pins Associated with a Comparator
- Removed 20.8 “Design Tips”
- Minor corrections to formatting and text were incorporated throughout the document

NOTES:

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